

Modeling, Analysis, Simulation and Control of Semiconductor Manufacturing Systems: A Generalized Stochastic Colored Timed Petri Net Approach

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ABSTRACT

In this paper, a generalized stochastic colored timed Petri net(GSCTPN) is used to model an IC wafer fabrication system. There are two major sub-models: Process-Flow Model and Transportation Model. There are two different automated guided vehicle systems, namely, Interbay system and Intrabay system. For multiple-load and variable-speed AGV system, we embed a simple motion-planning rule and introduce a collision avoidance strategy in model to solve the variable speed and traffic jam problems of vehicles. The simple control policies for AGV's visiting and AGV's routing are discussed. The heuristic rules for lot release and lot scheduling are also studied. To obtain performance measures, simulation is used. To show the promising potential of the proposed work, a real-word IC wafer fabrication system is used as a target plant layout for implementation.

1 Introduction

The previous works in applying Petri nets to IC wafer fabrication are discussed below. Modeling, analysis, simulation, scheduling, and control of semiconductor manufacturing systems was performed by using Petri nets in [1]. It also serves as a good tutorial paper. Janneck [2] presents the modeling a die bonder with Petri nets. Xiong *et al.*[3] propose and evaluate two Petri-net based hybrid heuristic search strategies and their applications to semiconductor test facility scheduling. In [4], hybrid Petri nets are presented as tools for modeling and simulation of semiconductor manufacturing systems. The colored timed Petri net(CTPN) is used to model the furnace in IC wafer fabrication, based on CTPN, the dynamic behaviors of the furnace can be emulated [5]. Jeng *et al.*[6] report a project of applying Petri net methodologies to detailed modeling, qualitative analysis, and performance evaluation of the etching area in an IC wafer fabrication system located in Taiwan's Hsinchu Science Based Industrial Park.

In this paper, a generalized stochastic colored timed Petri net(GSCTPN) model is built to model the detailed behaviors of an IC wafer fabrication system. Some control policies generated based on that GSCTPN model are to optimize some a priori assigned performance criterion. The plant layout and process-

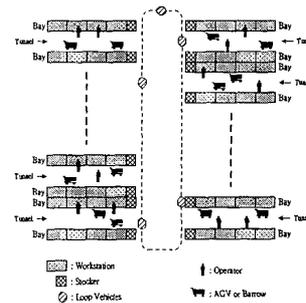


Figure 1: Physical Layout

ing steps are similar to that in [1, 6]. Different from the model proposed in [1, 6], the present work introduces a GSCTPN modeling of a general IC wafer fabrication system. The result net model solves the "long" net modeling of reentrant processing problem and contains fewer of places and transitions; especially, including two different multiple-load and variable-speed AGV transportation systems. Although the AGV transportation system provides us flexibility and economy, it leaves us numerous ways of routing which unfortunately gives the control problem a combinatorial flavor. The organization of this paper is as follows. Section 2 describes the overview of IC manufacturing process and the IC plant layout. Section 3 introduces a GSCTPN Modeling of system. Section 4 describes a performance analysis based on simulation. Section 5 is conclusion.

2 System Description

In general, the machines in an IC wafer fabrication system are grouped into four functional sections: the *photolithography area*, the *diffusion area*, the *etching area*, and the *thin film area*. A processing unit of wafers is called a *lot* in an IC wafer fabrication. When *lots* arrive at the IC factory, they are processed in the previously mentioned four areas. As shown in Fig. 1, an IC plant is a base of *tunnels*. Machines are placed beside the tunnels, they are grouped into a *bay*. In the Interbay system, The corresponding AGV stops are arranged in location 25-35 as shown in Fig. 2. There is only one single-loop track in the Interbay system. In the In-

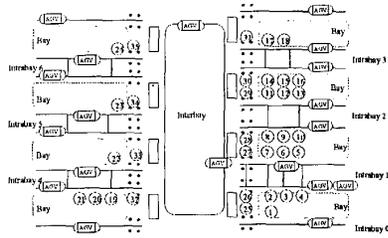


Figure 2: Plant Layout

terbay system, AGV that are called *loop vehicles* can move to any stop in unidirectional. Each stop in Interbay system is used as a transit station that transports lots between different bays. We denote the transit station as *Interbay station/stoker*. There are 24 stations divided into 6 types, each of multi-server stations consists of several identical pieces of equipment. There are two types of lots associated with different wafer processing flows. One consists of 172 operations. The other consists of 148 operations.

3 Generalized Stochastic Colored Timed Petri Net Modeling

The proposed generalized stochastic colored timed Petri-Net (GSCTPN) extends the framework of the original PN by adding color, time and modular attributes to the net. The GSCTPN model contains two major sub-models. One is called Transportation Model, and the other is called Process-Flow Model.

3.1 Modeling for Process Flow

The Process Flow Model can be decomposed into two micro-models, each with different characteristics. One is Process Routing Module and the other is Process Elementary Module. The following are detailed descriptions of each of these micro-models.

Process Routing Module

The GSCTPN model we proposed to illustrate the processing flow of each lot type is Process Flow Model. It models the technological precedence constraints for processing lots and provides normally more than one alternative routes to accomplish the operation processing. The essential idea is that, the number of color set is equal to sum of adding total processing-steps for each type of lot. This means that the processing-steps attribute is embedded as colors to the model. For example, the number of processing steps for type 1 is 172 and that of type 2 is 148. Then, the number of color is 320. Token in color set k represents that a lot is currently processing at the k -th step. Moreover, the number of tokens in color set k represents the how many lots currently is at the k -th step.

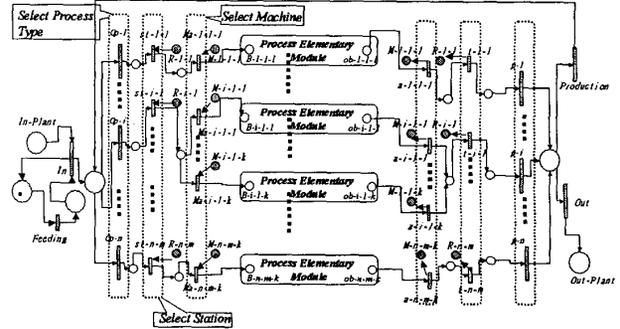


Figure 3: Process Routing Module

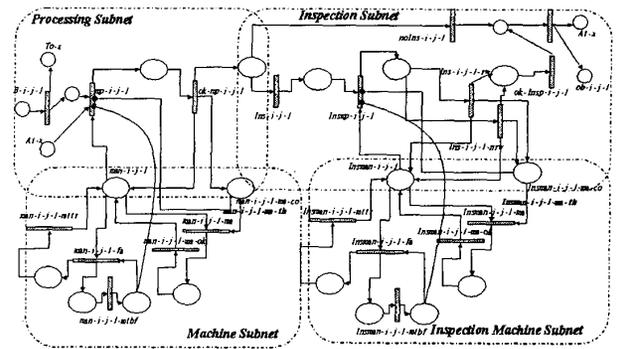


Figure 4: Process Elementary Module

Process Elementary Module

The Process Elementary Module can be composed of four subnets as shown in Fig. 4, each with different characteristics. They are, namely, Processing Subnet, Inspection Subnet, Machine Subnet, and Inspection Machine Subnet. However, the Inspection Subnet and Inspection Machine Subnet has to be additionally included if wafers need to be inspected. The following are detailed descriptions of each of these subnets.

The essential idea of modeling Processing Subnet is that, before a lot can take up any resource, it must acquire its control right in terms of a token. For example as shown in Fig. 4, if a lot wants to move to the machine $Mac-i-j-l$ located at the stop x , it must get the token of resource place $man-i-j-l$. Moreover, if the current location where the wafer resides is not the same with that of machine $Mac-i-j-l$, it is need to send a signal in the communication place $To-x$. It invokes an AGV to come to the place where the wafer resides. When the AGV arrives, it proceeds to load the wafer. The AGV starts to move to the destination place.

Machines may fail, it is very common in IC fabrication. In Machine Subnet which is shown in Fig. 4, an operation transition $man-i-j-l-mtb$ will be fired periodically according to the fabrication statistics. It is called *mean time between failure*(MTBF). If transition

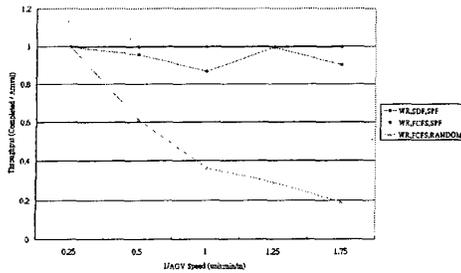


Figure 17: The relationship between speed of AGV and routing rule

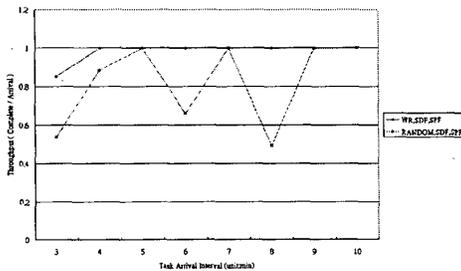


Figure 18: The relationship between visiting rule and task arrival interval

AGV Routing and AGV Visiting

In Intrabay 1, there are three multiple-load AGVs. There are three rule combinations. (WR(*workload regulating*),SDF(*shortest distance first*),SPF(*shortest path first*)) denotes that the AGV dispatching rule is WR, visiting rule is SDF, and routing rule is SPF. (WR,FCFS,SPF) presents that the dispatching rule is WR, visiting rule is FCFS(*first come first serve*), and routing rule is SPF. (WR,FCFS,RANDOM) presents that the dispatching rule is WR, visiting rule is FCFS(*first come first serve*), and routing rule is RANDOM. Moreover, there are five runs in this simulation. The AGV's speed of the first run is 1/0.25 m/min and 1/1.75 m/min for the last run. In Fig. 17, we can see that the gap among three different combinations is increased according to 1/(speed of AGV). This phenomenon indicates that increasing the speed of AGV can increase performance. The Fig. 17 also shows that the routing rule has more impact on performance than the visiting rule in this simulation experiment.

AGV Dispatching

There are two combinations, (WR,SDF,SPF), (RANDOM,SDF,SPF) to be implemented. (WR,SDF,SPF) denotes that the AGV dispatching rule is WR, visiting rule is SDF, and routing rule is SPF. (RANDOM,SDF,SPF) presents that the

dispatching rule is RANDOM, visiting rule is SDF, and routing rule is SPF. The loading and storing tasks are fed into the Interbay 1. The task arrival is DETERMIN. Moreover, there are eight runs in this simulation. The task arrival interval of the first run is 3 minutes and that of the last is 10 minutes. The Fig. 18 shows the results. The cycle time is increased according to the rate of task arrival. In this simulation experiment, dispatching rule RANDOM and WR are little difference in performance due to only three AGVs. If the number of AGVs is large, we can predict that RANDOM and WR are much different in performance. The Fig. 18 also shows that WR has stable performance than RANDOM.

5 CONCLUSION

The present work introduces a GSCTPN modeling of a general IC wafer fabrication system, the result net model solves the "long" net modeling of reentrant processing problem. The validated model can be used to answer many "what-if" questions, such as predicting the throughput.

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