行政院國家科學委員會專題研究計畫　期中進度報告

子計畫一：極大型混合尺寸模組的平面規劃與擺置(2/3)

計畫類別：整合型計畫
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執行期間：93 年 08 月 01 日至 94 年 07 月 31 日
執行單位：國立臺灣大學資訊工程學系暨研究所

計畫主持人：楊佳玲
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行政院國家科學委員會補助專題研究計畫成果報告

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執行單位：台灣大學資訊工程學系

中　華　民　國　94　年 5　月 28 日

行政院國家科學委員會專題研究計畫成果報告

先進電子設計自動化技術研發

子計畫一：極大型混和尺寸模組的平面規劃與擺置 (2/3)

計畫編號：NSC-93-2220-E-002-001
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計畫主持人：楊佳玲　　台灣大學資訊工程系
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一、中文摘要

在本計劃第二年，我們提出了一以階層比例分割(hierarchical ratio partition)為基礎的擺置演算法來處理極大型混和尺寸的設計。這個擺置演算法包含了三個步驟：全域擺置(global placement)，合法化(legalization)和詳細擺置(detailed placement)。和傳統以分割為基礎的方法不一樣的地方是我們在每一層都採用比例分割。另外，藉由在每一層使用事先觀察(look-ahead)的技術，我們可以更精確的檢驗某擺置的合理性。

此計劃第二年之另一成果是我们提出一個結構層(Architecture Level)考量溫度之平面規劃工具。隨著晶片電晶體密度提高，溫度將是未來設計上之主要考量。此平面規劃工具，能協助設計者在溫度的限制下 找到最佳 performance 之結構及平面規劃。

關鍵詞：奈米科技，平面規劃，擺置，溫度限制，模擬退火法

Abstract

In the second year of this project, we develop a hierarchical ratio partitioning based placement algorithm for large-scale mixed-size designs. The placement algorithm consists of three steps: global placement, legalization, and detailed placement. Unlike the traditional partition-based technique that is based on balanced partitioning, we apply ratio partitioning in each level. Further, by applying the look-ahead bipartitioning technique in each level, we can evaluate the feasibility of the placement for sub-partitions more accurately.

The other accomplishment in this year is that we develop a thermal-aware architectural floorplanner. As the transistor density continues to grow, thermal will become the main design issue. With the aid of this tool, an architect can explore both physical and architectural design spaces simultaneously to find an architecture and the corresponding chip layout that maximizes performance under a thermal limitation.

Keyword: nanometer technology, floorplaning, placement, temperature constraint, simulated annealing

二、Introduction & Objective

As the process technology advances, the feature size is getting smaller and smaller, which makes it possible to integrate an entire system with one billion transistors on a single chip. At the same time, the Intellectual Property (IP) modules and pre-designed macro blocks (such as embedded memories, analog block, pre-designed datapaths, etc.) are often reused, and thus many IC designs contain hundreds of thousands of modules with different sizes. Hence, we need an efficient algorithm to solve such a placement problem with a large number and hybrid sizes of modules and cells.

Traditional standard cell placement techniques assume that cells have the same sizes. Thus, they cannot handle problems with different sizes well. Many researchers have presented to handle such a mixed-size placement problem, including the analytical-based approach [5], the simulated annealing-based approach [3], and the partition-based approach [1].

In this report, we present a **hierarchical ratio partitioning based placement algorithm** for large-scale mixed-size designs. The placement algorithm consists of three steps: global placement, legalization, and detailed placement. It works in a hierarchical manner and integrates net-weighting partitioning, white space management, look-ahead bipartitioning, and fast legalization to handle the large-scale mixed-size placement problems.

As the technology continues to improve, power density within a single chip increases steadily. High die temperatures reduce device reliability and cause timing error. Moreover, transistor speed is slower at higher temperatures, and leakage power grows exponentially as temperature increase. Thus, the heat is a critical design consideration for large-scaled mixed-size designs. Therefore, to handle the thermal stress in large-scale mixed-size designs, we propose a **thermal-aware architectural floorplanner** that can optimize performance while satisfying a given temperature constraint. The floorplanner consists of three main approaches for consideration temperature constraint: the adaptive cost function, the heuristic-based perturbation, and the configuration selection

三、Research Techniques

3.1 Hierarchical Ratio Partition Algorithm

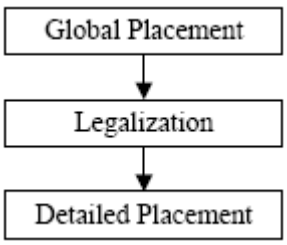

Figure 1. The flow of our placement algorithm

Our placement algorithm consists of three steps: global placement, legalization, and detailed placement as shown in Figure 1. We apply three techniques, the net-weighting partitioning, the whitespace distribution, and the look-ahead bipartitioning for the global placement stage and the fast legalization for the legalization stage. We will introduce each technique at the following subsections.

Net-Weighting Partitioning

We recursively partition a block into two set of sub-regions. The block-location determination problem can be formulated as a hypergraph partitioning problem. Then, the hypergraph is partitioned using a weighted-net, min-cut bipartitioner to obtain the minimum half perimeter wirelength (HFWL). Each node in the hypergraph represents a block inside the region, with the node weight begin set to the area of the corresponding block. Each edge corresponds to a multi-terminal net in the circuit, with the hyperedge weight being set to the value of the HPWL contribution if the hyperedge is cut.

Whitespace Distribution

If a large block exists in the region, we cannot always use a balanced region bipartition, or the block may not fit into any sub-region. In this case, we perform the ratio partitioning. We add a dummy node connecting to the node corresponding to the large block , and set the net-weight to a large negative value.

Traditional min-cut based placers uniformly distribute whitespace in the chip, producing excessive wirelength when large amount white spaces are present. We control the imbalance factor to allocate the whitespace.

Look-Ahead Bipartitioning

The look-ahead bipartitioning concept is proposed in [4] to solve floorplanning problem. It integrates the cutsize-driven bipartitioning and the area-driven floorplanning. Before each application of cutsize-driven bipartitioning, area-driven floorplanner is used to check whether the given sub-problem can be legalized.

For our look-ahead bipartitioning, we resort to a first-fit bin-packing heuristic to check if the subproblem can be legalized. If such a legalization solution exists, the cutsize-driven bipartitioning continues like [4]. If not, we move the cut-line toward the partition with a smaller utilization ratio. Then, we redo the ratio partitioning by modifying the imbalance factor. Again, we check for the existence of a legalization solution, and the ratio partitioning is repeated until we find a legalization solution.

Fast Legalization

In this step, all cells are moved into rows and all overlaps are removed. To legalize a large-scale global placement solution effectively

and efficiently, we propose a fast three-stage legalization algorithm: (1) place cells into their nearest rows (legalize the *y*-coordinates of all cells), (2) sort all standard cells according to their sizes, from the largest to the smallest, and (3) assign the *x*-coordinates for all cells according to the sorted order. If no overlap occurs, the resulting *x*-coordinate of the cell is kept; otherwise, we will find a nearest empty slot to place the cell.

3.2 Thermal-aware Architecture Floorplanning

The goal of thermal-driven floorplanning is to optimize performance with an architectural template and set of architectural configurations under a given temperature constraint. The performance is defined as instruction per cycle (IPC) times the cycle time. Figure 2 shows our framework for thermal-driven floorplanning. Below we detail the methods used in our thermal-driven floorplanner.

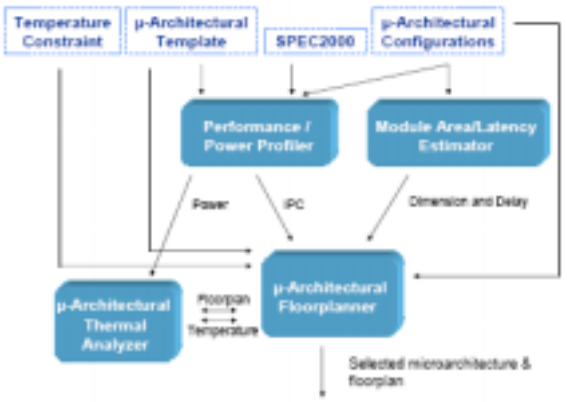

Figure 2. Framework overview of thermal-driven floorplanning

Adaptive Cost Function

The cost function Φ used in our cost function is defined as:

$$\Phi = \alpha \frac{CT_p}{IPC(c)} + \beta T ,$$

where CT_p is the estimated cycle time for the floorplan *P*, IPC(c) is the estimated IPC of the configuration c, and T is the maximum temperature of *P*. We estimate the wirelength according to the half perimeter measure and use IPEM [2] to estimate the interconnect delay. The parameter α is always equal to 1 while β is changed adaptively as followings:

$$\beta = 0, \text{ if } T \le T_{max}$$

$$\beta = T - T_{max} + \varepsilon$$

where T_{max} is the temperature constraint, and ε is a constant between 0 and 1.

Heuristic-Based Perturbation

We introduce two types of operations: Critical-Module-Swap and Hot-Cold-Mix. The Critical-Module-Swap operation swaps Module-X with a neighbor of Module-Y, where Module-X and Module-Y are both in the critical path. The Hot-Cold-Mix operation places the hottest module around the coldest one. When the temperature is not violated, we focus on performance optimization, so Critical-Module-Swap is considered. When the temperature is violated, Hot-Cold-Mix is considered.

Configuration Selection

Unlike [3] that randomly choose a module to perform configuration selection, we evaluate the cost of all configurations under the current layout, and choose the first three configurations in the increasing order of their cost as our configuration alternatives. We also choose configurations that violate the temperature constraint as our configuration alternatives. Our approach can generate better results than the random approach since our SA engine converges faster.

四、Conclusions and Discussions

In this report, we proposed a hierarchical ratio partitioning based algorithm that can efficiently and effectively handle the large-scaled mixed-size designs. There are four major techniques for our placement algorithm: net-weighting algorithm, whitespace distribution, look-ahead bipartitioning, and fast legalization. Furthermore, due to the integration of large-scale cells with one single chip, thermal issue will be a critical problem. We also propose a architectural-level thermal-driven floorplanner that can optimize performance with an architectural template and set of architectural configurations under a given temperature constraint.

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