# 行政院國家科學委員會補助專題研究計畫成果報告

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※「K-頻段無線收發關鍵元組件之研究」子計畫三：※

※ 升降頻器之研製（2/3） ※

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計畫類別：☐個別型計畫 ☑整合型計畫

計畫編號：NSC 88-2219-E-002-020

執行期間：88 年 8 月 1 日至 89 年 7 月 31 日

計畫主持人：王 暉

共同主持人：

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☐赴國外出差或研習心得報告一份

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執行單位：

中 華 民 國 89 年 8 月 30 日

「K-頻段無線收發關鍵元組件之研究」子計畫三：

升降頻器之研製（2/3）

Research and Development of Down- and Up-Converters（2/3）

計畫編號：NSC 88-2219-E-002-020

執行期限：88 年 8 月 1 日至 89 年 7 月 31 日

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## 一. 中文摘要（關鍵詞：K-頻段，單晶微波積體電路、降頻器、升頻器、收發機。）

本計畫預備研究及設計 K-頻段(21-26 GHz)之降頻器與升頻器元組件。該元組件係應用於微波電信機之傳送接收器。製作此微波電路晶片，將使用國外之砷化鎵單晶微波電路之代工之高速場效電晶體製程與異質接面雙極性電晶體製程。此升降頻器中之電路將包含低雜訊放大器、混波器及中頻放大器等。

在此三年計畫中，元件模型、電路設計及佈局、晶片製作與測試均將進行。在電路設計方面，我們使用國科會晶片中心所提供之高速場效電晶體與異質接面雙極性電晶體代工製程為主。第一年計畫中，已完成製作第一循環之單一功能電路之晶片，同時並完成部分電路之測試。本年度除繼續進行電路量測工作外，並利用 0.15 微米高速場效電晶體以及異質接面雙極性電晶體的製程，進一步設計各項單一及多功能晶片。

**Abstract**（Keywords：K-band, MMIC, Downconverter, Upconverter, Transceiver.）

This project is aimed at the development and the design of K-band (21-26 GHz) downconverter and upconverter components for microwave radio transceiver applications using commercial foundry GaAs MMIC process technologies. The components will include low noise amplifiers, mixers and IF amplifiers.

In this 3-year project, device modeling, MMIC design, chip layout, fabrication and chip evaluation will all be exercised. In the MMIC design portion, we use the HEMT and HBT foundry service provided by CIC. In the first year, we have completed individual single-function components based on existing models. Part of the circuits have been measured. In this year, in addition to the on going chip measurement effort, we used the 0.15-μm PHEMT and HBT MMIC processes to further develop the various single- and multi-functional MMIC chips.

## 二. 計畫緣由與目的

There has been some research and development effort devoted in low microwave frequency range ( < 10 GHz) MMIC frequency converters in Taiwan. The goal of this project is to push the MMIC frequency converters design technology to K-band (20-30 GHz) and demonstrate the up- and down-converters implemented in MMIC chips. Since the GaAs

HEMT and HBT MMIC process technologies are available through commercial foundries, we used of the accessible MMIC processes to develop learn the MMIC design and modeling techniques.

This project provided a starting point of frequency converter MMIC development to K-band frequency in Taiwan and also established the infrastructure in our institute. The importance of this step-stone for future wireless MMIC technology development is obvious.

## 三. 研究方法與結果

In the first year, we have designed the LNAs, driver amplifiers, mixers and IF amplifiers fabricated using Philips, France 0.2-μm PHEMT process. Part of these circuits have been measured. The results are presented in [7], [8]. In this year, in addition to the on going chip measurement effort, we used the 0.15-μm PHEMT and HBT MMIC processes to further develop the various single- and multi-functional MMIC chips.

### LNA

The low noise amplifier was designed using four-finger 120-μm PHEMT to operate at 21 to 26 GHz [3]. Inductive T transformers were used to match the device impedance to 50 Ω input and output. MIM capacitors were used for dc block and RF bypass. Fig. 1(a) and 1(b) show the chip photo and the measured small-signal gain and return loss of two-stage LNA. At 24 GHz, the small signal gain is 16.4 dB and input/output return losses are 7.5/11.6 dB.

### Driver Amplifier

The driver amplifier was designed using 120-μm PHEMT to drive 300-μm PHEMT. Inductive T transformers were used to match the device impedance to 50-ohm input and output [4]. The 90° hybrid, Lange coupler, and the single-end design are used as the balanced amplifier. MIM capacitors were used for DC blocking and RF bypassing. Fig. 2(a) and 2(b) show the chip photo and the measured small-signal gain of two-stage single-ended PA, the single-end amplifier demonstrated a small signal gain of 19 dB at 24 GHz. The power performance of the single-ended one is shown in Fig. 2(c). It has a 1-dB compressed power point ($P_{1dB}$) of 14.6 dBm at 22 GHz.

### Mixer

The subharmonically pumped mixer used two anti-parallel diodes each with four gate finger of 40 μm width to operate from 21 to 26 GHz of RF frequency. This circuit is suitable for both frequency upconversion and downconversion. Fig. 3(a) and 3(b) show the chip photo and the measured results of the subharmonically pumped mixer. The measured conversion loss is 12 dB for up conversion and 14 dB for down conversion.

### IF Amplifier

Five PHEMTs with a total gate periphery of 660 μm were used as the active devices for these amplifiers [5], [6]. Both microstrip line and GCPW are used to form the artificial gate and drain transmission lines. They are periodically loaded with the capacitive gate and drain impedance of the FET's forming lossy transmission line structures of different characteristic impedance and propagation constant. The resultant effective input and output propagation structures acted as gate and drain lines. An RF signal applied at the input end of the gate line travels down the line to the other end, where it is absorbed by the terminating impedance. The chip photos are shown in Fig. 4(a) and 4(c). Fig. 4(b) and Fig. 4(d) show the measured small-signal gain and return loss via on-wafer probing. The microstrip-line design demonstrated a small signal gain of 12±2.5 dB, and the GCPW design has a small-signal gain of 10±0.5 dB.

In addition, we also complete the circuit designs using the GCS HBT process and TRW 0.15-μm PHEMT process. Table 1 lists the results of these circuits.

## 四. 參考文獻


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| 0.15-μm PHEMT Process | | |
|---|---|---|
| Name | Description | Simulated Results |
| FIL001 | ◆Active filter<br>◆4-finger, 120-μm PHEMT<br>◆microstrip line design | G = 7 dB<br>@19 GHz |
| LNA | ◆4-finger, 120-μm PHEMT<br>◆microstrip line design | G=21 dB,<br>NF=1.7 dB<br>@ 24 GHz |
| Mixer | ◆4-finger, 40-μm gate-PHEMT diode<br>◆singly balanced design with a Lange coupler | Conversion loss < 10 dB<br>Return loss > 10 dB |
| HBT Process | | |
| Name | Description | Measured Results |
| VCO | ◆12-μm² emitter area HBT<br>◆microstrip line design | Frequency : 29 GHz<br>Power : -5 dBm |

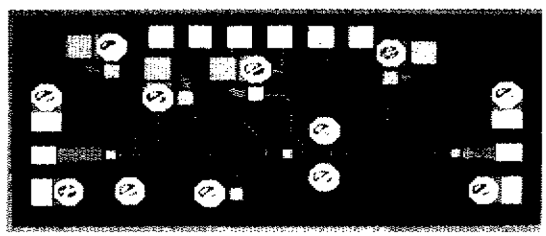

Fig. 1(a) The chip photo of two-stage LNA.

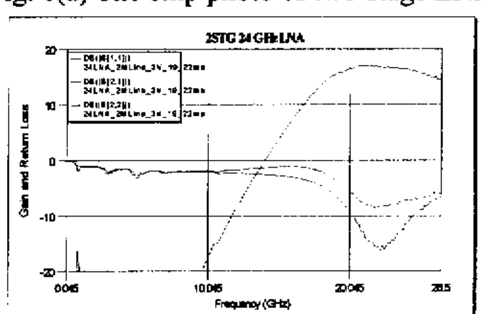


Fig. 1(b) Measured small-signal gain and return loss of two-stage LNA.

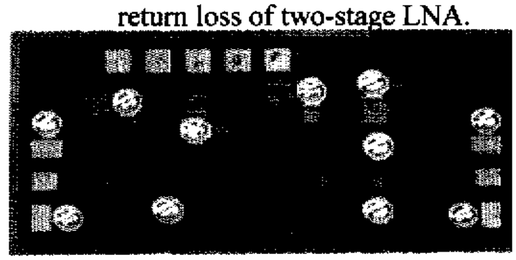

Fig. 2(a) The chip photo of two-stage PA

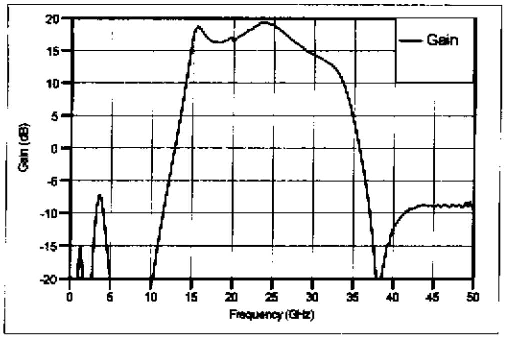


Fig. 2(b) Measured small-signal gain of two-stage single-ended PA.

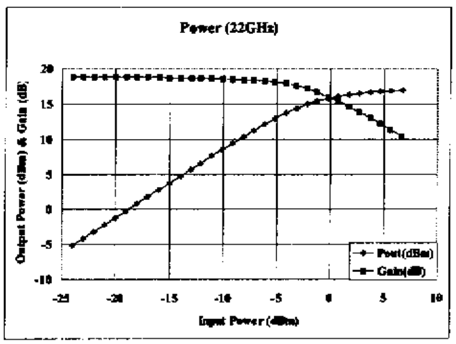


Fig. 2(b) Measured power performance of two-stage single-ended PA.

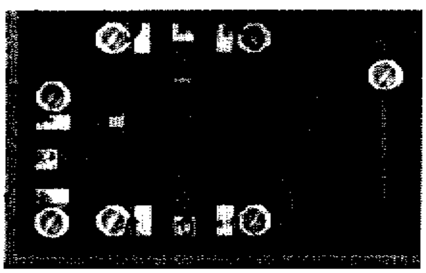

Fig. 3(a) Chip photo of the subharmonically pumped mixer.

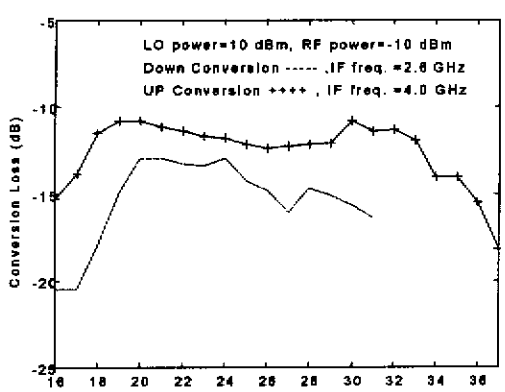


Fig. 3(b) Measured conversion of the subharmonically pumped mixer.

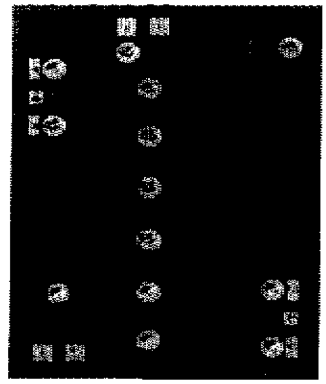

Fig. 4(a) The chip photo of the microstrip-line DA.

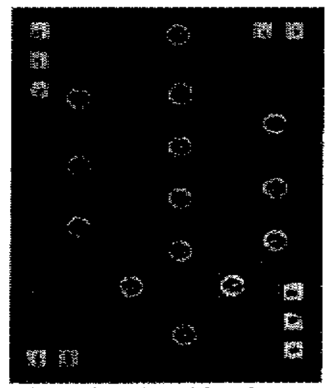

Fig. 4(b) The chip photo of the GCPW DA.

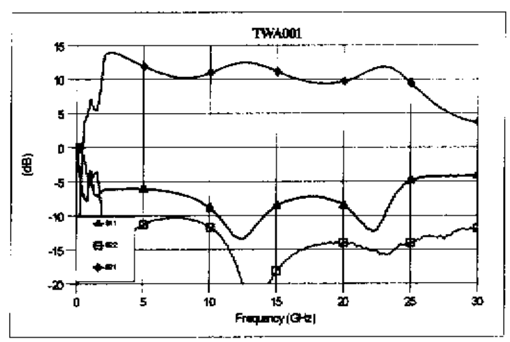


Fig. 4(c) Measured small-signal gain and return loss of microstrip-line DA.

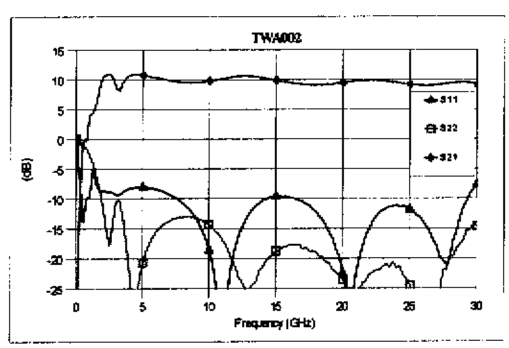


Fig. 4(d) Measured small-signal gain and return loss of GCPW DA.