Throughput of ATM cell over Wireless Rayliegh Channel

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Abstract

In this paper, an error correction scheme employing side information is proposed first time to improve the throughput of the Asynchronous Transfer Mode (ATM) transmission over Rayleigh fading channel using the binary phase shift keying (BPSK) modulation. With the combinations of the Selective Repeat protocol (SR) in the link layer and the error correction scheme, the throughput of the ATM cell is improved significantly. The numerical examples show that at high bit error rate the throughput gain is enormous.

1. Introduction

The demand of multimedia communications over the wireless system increases rapidly. The ATM, which is very flexible for various services, is widely used for multimedia communications. On the other hand, The wireless communication possesses very attractive mobile property. The cellular and trunking radios become very popular. So the ATM over wireless is very desirable.

In the wireless channel, the noise, fading, and interference effect the transmission tremendously. The bit error rate (BER) usually is very high. However, the conventional computer communication Automatic Repeat Request protocols (ARQ) such as Stop-and-wait, Go-back-N, and Selective Repeat (SR), are designed mainly for the telecommunication transmission environment which is built on the copper and fiber technologies. The transmission of ATM cell over wireless using the conventional ARQ protocol is very inefficient especially when the BER is high. There are some techniques proposed to reduce the bit error rate in the Rayleigh fading channel [1]-[4]. In [5], Shu Lin and Philip S. Yu proposed a hybrid ARQ scheme to increase the throughput efficiency using the forward-error-correction (FEC) codes.

In this paper, we propose a new scheme, which combines the ARQ protocol and the error correction scheme with side information, to improve the ATM cell throughput. In a conventional binary receiver, a single threshold is used to make decision. However, the difference between the threshold and the signal value bears some information. Here we propose a generator to generate the side information. When the output value of the correlator is in a certain region, the bit is marked. It is more likely that wrong decision is made in the marked bit than the other. So these bits can be used to correct the erroneous ATM cell. The numerical examples show that the throughput gain can be enormous at high bit error rate.

2. Binary Phase Shift Keying Receiver with Side Information Generation

As shown in Fig 1, the proposed BPSK receiver with side information generation consists of two parts. The first one consists of a correlator and a maximum likelihood decoder to produce an estimated digital signal. The second one, which is connected to the output of the correlator, includes a comparator and a decision circuit to generate side information. The only difference between the conventional PSK receiver and our receiver is the side information generator that is designed to extract the side information of the input signal by marking the possible error bits. In the

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Fig 1: receiver diagram

first branch, the output value of the correlator is greater than the threshold level, the decision is made in favor of "1". Otherwise, the decision is made in favor of "0". If "1" is transmitted, the probability distribution of the correlator output is shown in Fig 2, where T is the bit duration, A_s and A_L are the amplitudes of the received signal and the local oscillator.



Fig 2: the distribution of the output value of correlator when "1" is sent by transmitter.

Now we consider the side information generation. It is obvious, if the output value of the correlator is larger than r, the transmitted signal has very high probability to be "1". If the output value of the correlator is fallen in the region (0, r), the signal will still be determined as "1" with slightly higher possibility of wrong decision. Similarly, if the output value of the correlator is fallen in the region (0, -r), the bit will also have higher error probability. So all the received signals in the regions (r, ∞), (0, r), (-r, 0), and (-r, - ∞) will be recorded and denote as Conditions I, II, III and IV for further processing. The bits in Conditions II and III will be specially marked. Obviously most error bits should be in the marked bits if we set the threshold r properly. When cells are transmitted, the receiver uses the CRC checksum to detect erroneous cells. With the aid of side information the receiver may locate the erroneous bits and correct them.

3. Error Correction Scheme with Side Information

In this paper, we assume that the channel is Rayleigh fading channel and the SR ARQ protocol is employed. For simplicity, the buffer is assumed to be infinite and the effect of erroneous acknowledgement (ACK) and negative

acknowledgement (NAK) is ignored. The length of packet is 53 bytes including 2 bytes CRC checksum. The format of packet is defined as shown in Fig 3.



Fig 3: the format of packet

The side-information error correction scheme consists of n-bits-marked error correction and two-packet error correction. The protocol is described as below. If a packet is sent by the transmitter and received without error, the receiver will deliver it to the higher layer and send an ACK to the transmitter. If the packet is erroneous, n-bits-marked error correction will be employed. For example, if n bits of Conditions II and III in an erroneous packet and the error bits occur in the n marked bits. The sum of all combinations of the error bits is:

Therefore, we can correct the packet by alternating the n marked bits n_c times at most. If the number of marked bits is larger than the maximum number of marked bits, a NAK will be sent to the sender immediately.

b1 b2	I	II	III	IV
Ι	1	1	1	0
II	1	1	0	0
ш	1	1	0	0
IV	1	0	0	0

Table1: error correction table of two-packet error correction

After the n-bits-marked error correction process, if the erroneous packet can be corrected, the receiver delivers it to the higher layer and sends an ACK back. Otherwise, the receiver saves the packet and sends a NAK to the transmitter to request for a retransmission. The receiver will process the retransmitted packet as the previous one, but it will not send the NAK back if it can't be corrected immediately. The receiver will further process the packet by employing two-packet error correction which compares these two erroneous packets bit by bit. Table1 is the decision table of this process. b1 and b2 denote the same position bits in the first packet and the retransmitted packet. For example, if the bit in the first packet was fallen in Condition IV, this bit will be determined as "1".

If the packet still can not be corrected, the receiver will save the first retransmitted packet, discard the first transmitted one and send a NAK to the transmitter. When the receiver received the second retransmitted packed, it will

treat the packet as the first retransmitted one. This procedure will continue until the packet is received successfully. After some tedious derivation, we can express the throughput of this scheme as follows:

$$\begin{aligned} Throughput &= 1/E_{s}, \dots, \dots, (2) \\ E_{s} &= 1 + (1 - P_{f})/(P_{f} + P_{EEC}), \dots, \dots, \dots, (3) \\ P_{f} &= P_{c} + P_{n}, \dots, \dots, (4) \\ P_{c} &= (1 - P_{e})^{8}, \dots, \dots, (5) \\ P_{n} &= \sum_{i=1}^{n} C_{i}^{8} [(P_{2} + P_{3})^{i} P_{1}^{8-i} - P_{2}^{n} P_{1}^{8-i}], \dots, (6) \\ P_{EEC} &= P_{all} - P_{c1} - P_{c2} - P_{n1} - P_{n2} + P_{c12} + P_{c1n2} + P_{c2n1} + P_{n12}, \dots, (7) \\ P_{all} &= (1 - P_{e} - P_{24} + P_{31})^{8}, \dots, \dots, (9) \\ P_{c2} &= ((1 - P_{e})^{2} + P_{31})^{8}, \dots, \dots, (9) \\ P_{c2} &= ((1 - P_{e})^{2} + P_{31})^{8}, \dots, \dots, (10) \\ P_{n1} &= \sum_{i=1}^{n} C_{i}^{8} [(P_{11} + P_{12} + P_{13} + P_{14})^{8-i} (P_{21} + P_{22} + P_{23} + P_{31})^{i} \\ &- (P_{11} + P_{12} + P_{13} + P_{14})^{8-i} (P_{21} + P_{22} + P_{23})^{i}], \dots, \dots, (11) \\ P_{n2} &= \sum_{i=1}^{n} C_{i}^{8} [(P_{11} + P_{21} + P_{31})^{8-i} (P_{12} + P_{13} + P_{22} + P_{23})^{i} \\ &- (P_{11} + P_{21} + P_{31})^{8-i} (P_{12} + P_{13} + P_{22} + P_{23})^{i} \\ &- (P_{11} + P_{21} + P_{31})^{8-i} (P_{12} + P_{13} + P_{22} + P_{23})^{i} \\ &- (P_{11} + P_{21} + P_{31})^{8-i} (P_{12} + P_{13} + P_{22} + P_{23})^{i} \\ P_{c12} &= (1 - P_{e})^{28} \\ \dots, \dots, (12) \\ P_{c12} &= \sum_{i=1}^{n} C_{i}^{8} [(P_{11} + P_{21})^{8-i} (P_{12} + P_{13} + P_{22} + P_{23})^{i} - (P_{11} + P_{21})^{8-i} (P_{12} + P_{22})^{i}], \dots, (14) \\ P_{c2n1} &= \sum_{i=1}^{n} C_{i}^{8} [(P_{11} + P_{21})^{8-i} (P_{21} + P_{22} + P_{23})^{i} - (P_{11} + P_{21})^{8-i} (P_{12} + P_{22})^{i}], \dots, (14) \\ P_{c2n1} &= \sum_{i=1}^{n} C_{i}^{8} [(P_{11} + P_{21})^{8-i} (P_{21} + P_{22} + P_{23})^{i} - (P_{11} + P_{21})^{8-i} (P_{21} + P_{22})^{i}], \dots, (15) \\ P_{n22} &= \sum_{i=1}^{n-1} \sum_{i=1}^{n} \sum_{i=1}^{n} A_{i}^{8} + e_{i=i} e_{i} P_{i}^{8-m_{1}-m_{2}+k} / k! (m_{1} - k)! (m_{1} - k)! \bullet \end{aligned}$$

and

$$A_{y}^{x} \stackrel{\Delta}{=} x!/(x-y)! , x \ge y....(17)$$

$$C_{y}^{x} \stackrel{\Delta}{=} x!/[(x-y)!y!] , x \ge y....(18)$$

where P_f is the probability of the first transmitted packet that is received successfully. P_{EEC} is the probability of the error packet that can be recovered when the first transmitted packet and the first retransmitted packet were not received

successfully. E_s is the average number of transmissions for a successful packet. P_e is the bit error rate. B is the packet size. n is the maximum number of marked bits. P_1 , P_2 , P_3 and P_4 are the probabilities that the output values of the correlator is fallen in the regions (r, ∞), (0, r), (-r, 0), and (-r, $-\infty$) respectively. P_{xy} is $P_x P_y$. ('x' and 'y' can be 1, 2, 3 or 4.)

4. Numerical Results and Discussion

In this section, we will show the results of the side-information error correction scheme. In Fig 4, it is obviously the performance is the best when the maximum number of the marked bits is ten (n=10). Because we can correct the erroneous packet by n-bits-marked error correction scheme when the error bits are all in the marked bits. The larger n is the more possibility of the error bits is included in the marked bits. The maximum gain occurs when the BER is 2.6×10^3 . We define the gain as the difference of the throughputs of side-information error correction scheme and the conventional SR. Fig 5 depicts the throughput versus the average signal to noise ratio. The maximum gain occurs when average signal to noise ration is 20dB.



5. Conclusion

A novel error correct scheme with the aid of physical layer side information is proposed and analyzed. This scheme is applicable for wireless ATM transmission over Rayleigh fading channel especially for time sensitive packets such as voice or video. The result shows that this scheme can improve the ATM throughput tremendously when the BER is between 10^{-2} and 10^{-3} or the signal to noise ratio around 20dB. This scheme does not change the transmitter but requires modifying the receiver a little and needs computation power which can be solved as more powerful and low power comssuption processors are available.

6. References

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