行政院國家科學委員會補助專題研究計畫成果報告

※※※※※※※※※※※※※※※※※※※※※※※※※

※ **毫米波單晶電路之研製(1/3)** ※

※ Research and Development ※

※ of ※

※ Millimeter-wave Monolithic Circuits (1/3) ※

※※※※※※※※※※※※※※※※※※※※※※※※※

計畫類別：☑個別型計畫　□整合型計畫
計畫編號：NSC89-2213-E-002-178
執行期間：89 年 8 月 1 日至 90 年 7 月 31 日

計畫主持人：王　暉
共同主持人：

本成果報告包括以下應繳交之附件：
- □赴國外出差或研習心得報告一份
- □赴大陸地區出差或研習心得報告一份
- □出席國際學術會議心得報告及發表之論文各一份
- □國際合作研究計畫國外研究報告書一份

執行單位：

中　華　民　國　90 年 10 月 30 日

毫米波單晶電路之研製(1/3)
Research and Development of Millimeter-wave Monolithic Circuits (1/3)

計畫編號：NSC89-2213-E-002-178

執行期限：89 年 8 月 1 日至 90 年 7 月 31 日

主 持 人：王暉　　國立台灣大學電信所教授

E-mail　：hueiwang@ew.ee.ntu.edu.tw

計畫參與人員：王暉、連俊憲、張鴻埜、陳炳佑、魏淑芬、曾柏森、王毓駒、雷明峰、張家祺、吳佩喜、林晉申、蔡作敏

一. 中文摘要(關鍵詞：毫米波，Q-頻段，V-頻段，W-頻段，高速場效晶體，單晶微波積體電路。)

本三年期之計畫預備研製毫米波頻段(Q-band，33-50GHz)以上之單晶體電路。積體電路之製程將使用 CIC 洽商美國 TRW 公司所提供之 0.15 及 0.1 微米之高速場效電晶體(HEMT)之製程。所計劃研製之單晶積體之電路，包括放大器、混頻器、震盪器及被動和研製電路，如毫米波切換器、相移器及平衡-不平衡轉換器等。

在我們上一年度的計劃中(群體計劃「毫米波電路與天線」，子計劃九「毫米波單晶微波積體電路之研製」)，已成功地研製出 Ka-頻段(35- GHz)之各項積體電路。此一結果係為應用 CIC 所洽商之法國飛利浦公司之 0.2 微米 HEMT，MMIC 製程。在此一新計劃中，因為我們可用到更佳之 HEMT，MMIC 製程(0.15 及 0.1 微米之 HEMT，MMIC 製程)，因此我們將研製更高頻段之積體電路。我們將由 Ka-頻段之次高頻段，即 Q-頻段(33-50 GHz)開始。並將第三年之目標訂為 W-頻段(75-110 GHz)。

在本第一年之計劃中，我們已經完成了 40-GHz 共面波導低雜訊放大器、35-45 GHz 次諧波混頻器、35-GHz 振盪器、Q 頻段單刀雙擲開關，所有晶片皆已獲得量測結果。

Abstract (Keywords : Millimeter-wave, Q-band, V-band, W-band, HEMT, MMIC)

This three-year project is proposing the development of monolithic millimeter-wave (MMW) components at Q-band (33-50 GHz) and above using GaAs MMIC process technologies (e.g. 0.15 or 0.1-μm gate-length HEMT), which are available through a certain foreign commercial foundries, coordinated by CIC, National Science Council. The MMIC components will include low noise amplifiers, power amplifiers, mixers and oscillators, as well as some passive and control components, such as MMW switches, phase shifters, and baluns, etc.

The MMIC component development for frequency up to Ka-band (35 GHz) has been demonstrated by our research group in the previous Group Research of "Millimeter-wave Circuits and Antenna (NSC 89-2213-E-002-048), Subproject 9 (NSC 89-2213-E-002-052). This research utilized 0.2-μm gate-length HEMT MMIC process provided by Philip, France, also through CIC. In this new proposed project, since we have the access to more advanced technologies (0.15 and 0.1-μm gate-length HEMT MMIC processes, provided by TRW, USA through CIC), it is natural to investigate the feasibility of higher frequency MMIC components. We will start from the next higher band to Ka-band, that is, Q-band and target the W-band (75-110 GHz) frequency in the third year of this new project.

In the first year, we have completed the development of a 40-GHz CPW low noise amplifier, a 35-45 GHz sub-harmonic mixer, a 35-GHz voltage control oscillator, and an SPDT Q-band switch. All the MMICs have been measured.

二. 研究計畫之背景及目的

Millimeter-wave (MMW) frequency (30 - 300 GHz) transceiver will play a very import role in the next generation's wireless communication systems. There are many MMW MMIC components, including low noise amplifiers, power amplifiers, mixers and oscillators reported in US, Japan, and European countries [1]-[5] for MMW radar, communication and radiometer applications. There have been some research and development effort devoted in microwave frequency range MMICs [6]-[9] in Taiwan. In MMW frequency range, Ka-band MMIC components was demonstrated recently by our research group in the previous Group Research. This research utilized 0.2-μm gate-length HEMT MMIC process provided by Philip, France, also through CIC. Since we have the access to more advanced technologies (0.15 and 0.1- m gate-length HEMT MMIC processes, provided by TRW, USA through CIC), it is natural to investigate the feasibility of higher frequency MMIC components. The development of monolithic MMW transceiver components from Q-band (33-50 GHz) to W-band (75-110 GHz) are proposed in this new project. The objective of this project is to establish the design and modeling techniques for MMW MMIC up to W-band frequency using accessible MMIC processes and to train qualified personnel's (student and/or engineer).

三. 研究方法與結果

In this research, the procedures of MMW MMIC development is presented as follows.

1) **Establish design goal of each component.** The design goal of each component need to be determined by certain system requirements. Before the design starts, the system application and the detail design goal will be identified.
2) **Device model investigation.** For each solid-state device, the device figure of merit (FOM) need to be calculated in order to decide the circuit topology, e.g., f_T, f_{max}, maximum available gain of the transistor and cut-off frequency of the diode. For those devices that the models are not available, we need to perform the device dc and RF characterization and generate the models.
3) **Passive model library establishment.** Mainly for some special structures, e.g. power dividers/combiners, 90° and 180° couplers, baluns and etc. The goal will be targeted for miniature size.
4) **Circuit topology trade study and initial circuit design.** After the device FOM is obtained, the gain stage number of amplifiers can be determined. Regarding the mixer topology, sub-harmonic mixer is preferred in this project since it can use low frequency low phase noise source without frequency multiplication. The design approach of other components will be also determined via certain FOM and trade-off considerations.
5) **Circuit simulation, detailed design and layout.** In MMW frequency, the EM analysis of entire matching structure may be needed.
6) **Circuit fabrication and evaluation.** We share the R&D mask with CIC of National Science Council and get the chip fabricated using the 0.15- and 0.1- m PHEMT MMIC processes (provided by TRW). For circuit testing, on-wafer probing is planned to avoid the complicated fixture test.

In the first year, we have followed the above-mentioned procedure to develop Q-band (44-GHz) transceiver MMIC components. The chip design, simulation and layout were be completed and some chips have been measured.

LNA Fig. 1 shows the chip photo of the monolithic 40GHz CPW LNA, with a chip size of 3 mm × 2 mm. The three-stage LNA was designed using CPW transmission lines. The 4-finger 120 μm PHEMT was used for each stage. Drain short stubs use as feedback inductors to improve the stability. Fig. 2 shows the measurement result of small-signal gain and input return loss. In 37 to 43 GHz over 21 dB gain and 10 dB input return loss was achieved. The output return loss is better than 10 dB. The result is shown in Fig. 3.

Mixer Fig. 4 shows the chip photo of the sub-harmonic mixer, with a chip size of 1.5 mm × 1 mm. Using anti-parallel diode to produce the LO second harmonic power. Quasi-lumped stubs replace the quarter wave open stubs and short stubs and good isolation between RF and LO. Fig. 5 illustrates the conversion loss measurement result of the mixer. The conversion loss is less than 15 dB in 35 GHz ~ 45 GHz.

VCO Fig. 6 shows the chip photo of the 35 GHz VCO, with a chip size of 3 mm × 1 mm. The total gate width of transistor is 200 μm. MIM capacitor is RF bypass and DC block. Short stubs are used in gate and source as the feedback circuit. The match circuit contains open stubs, short stubs and coupled lines Fig. 7 presents the measurement result of the output power and output frequency, 10 dBm output power and 0.8 GHz tuning range are achieved. Fig. 8 shows the spectrum of the VCO output.

Q-Band Switch Fig. 9 shows the chip photo of the 35 GHz VCO, with a chip size of 1 mm × 2 mm. Fig. 10 is the measurement results. Over 30 dB isolation is achieved and it has about 3 dB insertion loss at 40 GHz

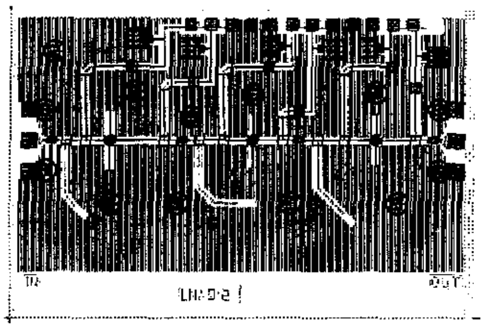

Fig. 1. Chip photo of the 40 GHz CPW LNA (3 mm × 1 mm)

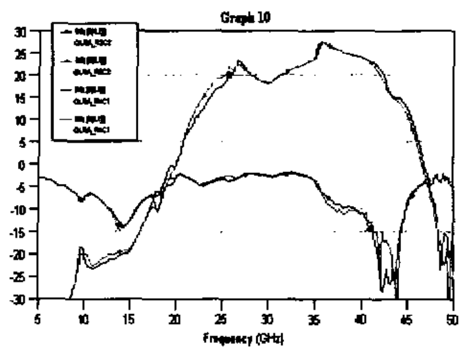

Fig. 2. Measured small-signal of gain and input return loss.

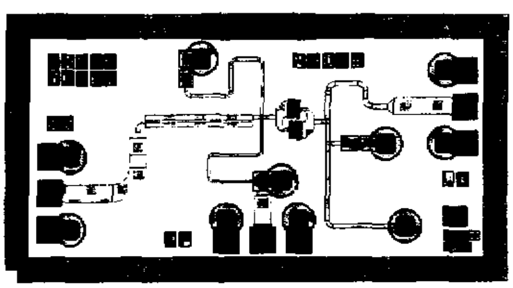

Fig. 3. Chip photo of the 35-45 GHz sub-harmonic mixer (1 mm × 1.5 mm)

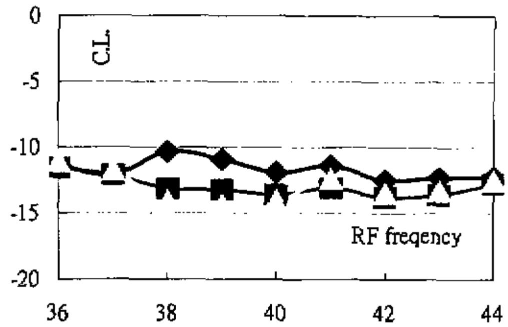

Fig. 4. Three conversion loss to measurement result of the Sub-harmonic mixer.

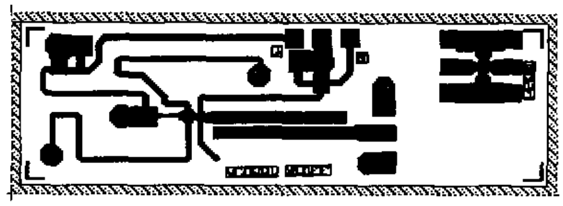

Fig. 5. Chip photo of the 35 GHz VCO (3 mm × 1 mm)

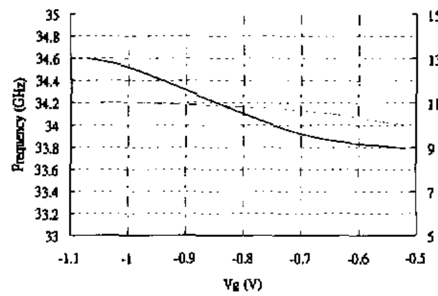

Fig. 6. Measurement result of output power and output frequency to tuning voltage

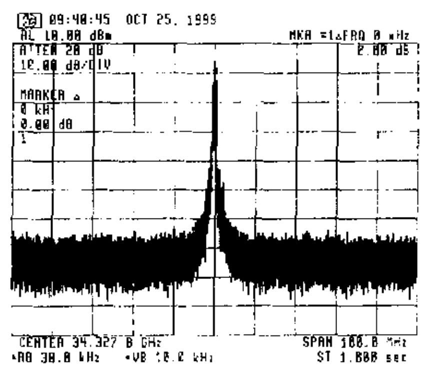

Fig. 7. Spectrum of the VCO output.

Fig. 8. Chip photo of the Q-band Switch (1 mm × 2 mm)

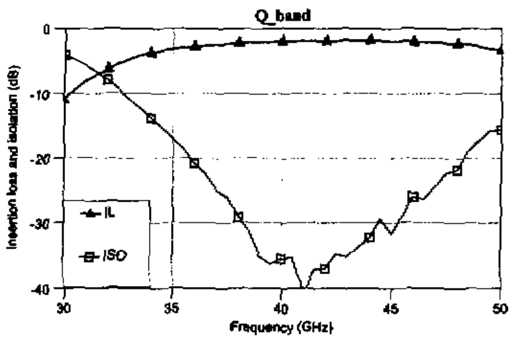

Fig. 9. The measurement result of the Q-band Switch including insertion loss and isolation.

四、參考文獻

[1] K. W. Chang, H. Wang, G. Shreve, J. Harrison, M. Core, A. Paxton, M. Yu, C. H. Chen, and G. S. Dow, "Forward looking automotive radar using a W-band single-chip transceiver," *IEEE Trans. on Microwave Theory Tech.*, vol. 43, no. 7, part 2, pp. 1659-1668, July 1995.

[2] H. Wang, Y. Hwang, L. Shaw, M. Ahmadi, M. Siddiqui, B. Nelson, D. Tait, B. Martin, R. Kasody, W. Jones, D. Brunone, and M. Sholley, "Monolithic V-band frequency converter chip set development using 0.2-micron AlGaAs/InGaAs/GaAs pseudomorphic HEMT technology," *IEEE Trans. on Microwave Theory Tech.*, vol. 42, no. 1, pp. 11-17, Jan. 1994.

[3] H. Wang, R. Lai, Y. C. Chen, Y. L. Kok, T. W. Huang, T. Block, D. Streit, P. H. Liu, P. Siegel, and B. Allen, "A 155-GHz monolithic InP-based HEMT amplifier," *1997 IEEE MTT-S International Microwave Symposium Digest*, vol. 3, pp. 1275-1278, Denver, Colorado, June 1997.

[4] Y. Itoh, K. Nakahara, T. Sakura, N. Yoshida, T. Katoh, T. Takagi, and Y. Ito, "W-band monolithic low noise amplifiers for advanced microwave scanning radiometer," *IEEE Microwave Guided Wave Lett.*, vol. 5, no. 2, pp. 59-61, Feb. 1995.

[5] J. Muller, T. Grave, H. Siweris, M. Karner, A. Schafer, H. Tischer, H. Riechert, L. Schleicher, L. Verweyen, A. Bangert, W. Kenllner, and T. Meier, "A GaAs HEMT MMIC chip set for automotive radar systems fabricated by optical stepper lithography," *IEEE J. Solid-State Circuits*, vol. 32, no. 9, pp. 1342-1349, Sept. 1997.

[6] T. H. Hsieh, H. Wang, Tahui Wang, T. H. Chen, Y. C. Chiang, S. T. Tseng, Andy Chen, and Y. E. Chang, "An ultra low cost and miniature 950-2050 MHz GaAs MMIC downconverter - I: design approach and simulation," *J. Chinese Institute of Engineers*, vol. 18, no. 3, pp. 437-444 , 1995.

[7] H. K. Chiou and H. H. Lin, "A miniature MMIC double doubly balanced mixer using lumped dual balun for high dynamic receiver application," *IEEE Microwave Guided Wave Lett.*, vol. 7, no. 8, pp. 227-229, Aug. 1997.

[8] H. K. Chiou, H. H. Lin, and C. Y. Chang, "Lumped-element compensated high/low-pass balun design for MMIC double-balanced mixer," *IEEE Microwave Guided Wave Lett.*, vol. 7, no. 8, pp. 248-250, Aug. 1997.

[9] Y. L. Lai, E. Y. Chang, C. Y. Chang, T. H. Liu, S. P. Wang, and H. T. Hsu, "2-V operation d-doped power HEMT's for personal handy-phone systems," *IEEE Microwave Guided Wave Lett.*, vol. 7, no. 8, pp. 219-221, Aug. 1997.

[10] T. H. Chen, K. L. Tan, G. S. Dow, and H. Wang, K. W. Chang, T. N. Ton, B. Allen, J. Berenz, P. H. Liu, D. Streit, and G. Hayashibara, "A 0.1-W W-band pseudomorphic HEMT MMIC power amplifier," *14th Annual IEEE GaAs IC Symposium Dig.*, pp. 71-74, Miami, FL, Oct., 1992.