# 應用於內建自我測試的低成本抖動測試技術

A Low-Cost Jitter Measurement Technique for BIST Applications

研究生 黃瑞澤
指導教授 黃俊郎 博士
台大電子所 VLSI Testing & Verification 實驗室 http://140.112.18.46

Quality of the clock signal plays an import role in modern high-speed systems because most activities are synchronized to the clock. However, in the existence of jitter, the clock edges may deviate from their ideal positions. To tolerate this, one has to lengthen the clock period, which degrades the system performance. Measuring high-speed clock jitters is a difficult task which relies on expensive ATE (automatic test equipment) and usually requires long test time. One promising solution to alleviate these problems is built-in self-test (BIST). Since on-chip BIST circuitry can be made close to the signal sources under test, accessing embedded signals becomes much easier and not limited by the bandwidth of the I/O pins.

Assuming that the jitter is a Gaussian random variable, the proposed technique measures the RMS value of the period jitter by comparing the phase relationships (lead or lag) between the signal under test and two delay versions of itself. Figure 1 depicts this concept. Once the two probability values ($p_1$ and $p_2$) with respect to the two delay values ($d_1$ and $d_2$) are available, the RMS jitter value can be derived in the following way:

1. Solve for $x_1$ and $x_2$ such that $F_X(x_1) = p_1$ and $F_X(x_2) = p_2$, where $F_X(x)$ is the normalized Gaussian cumulative distribution function.
2. $\text{RMS}_J = (d_1 - d_2) \div (x_1 - x_2)$.

The proposed BIST circuitry is shown in Figure 2. The BIST circuitry has two operation modes: the calibration mode and the measurement mode. In the calibration mode, $(d_1 - d_2)$ is derived. In the measurement mode, $p_1$ and $p_2$ are measured.

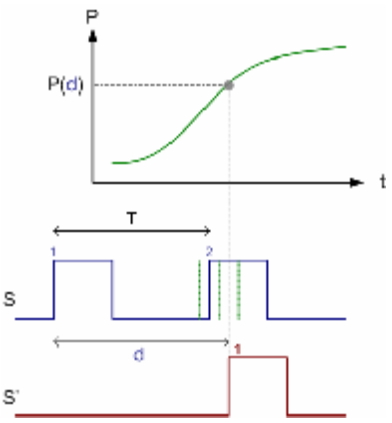

Fig.1 The basic idea.

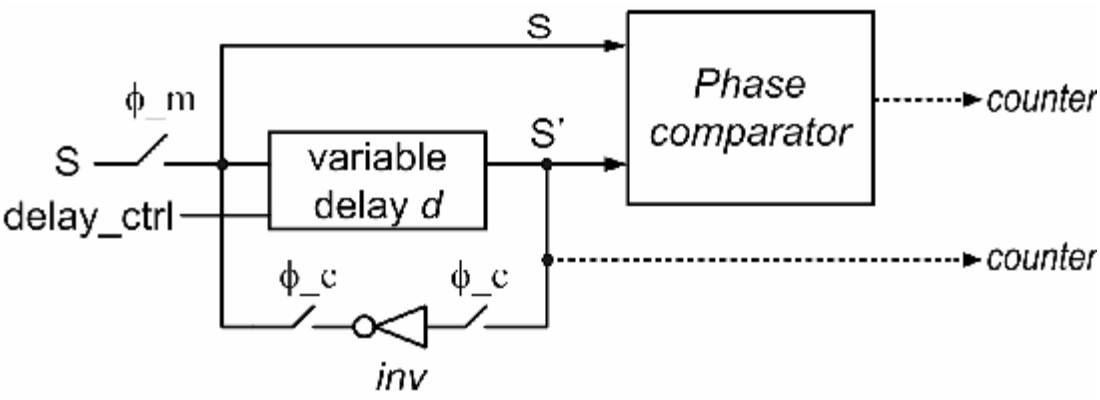


Fig.2 The proposed BIST circuitry