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A 2.17 dB NF, 5 GHz Band Monolithic CMOS LNA with 10 mW DC Power Consumption

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Abstract

The state-of-the-art noise figures of 2.17 dB and 3.0 dB at 5 GHz band from monolithic CMOS LNA's with 10 mW dissipation on thin (~ 20 μm) and normal (750μm) substrates are presented. Excellent Input return loss (S_{11}) of -45 dB, high P_{1dB} of -8.3 dBm and large IIP3 of 0.3 dBm were also obtained. The excellent performance of the LNA's is attributed to the methodology we developed.

Introduction

High data rate wireless local area networks (LAN) in the 5-GHz frequency band have become increasingly popular for mobile computing devices such as notebook computers, which impose severe demand on low power dissipation to extend the battery life. Recently, C-band LNA's [1-8] with low dc power consumptions (<15 mW) in various technologies have been developed and some of them are summarized in Table I. From this table it clear that CMOS integrated circuits, which are receiving much attention due to their potential for low cost and the prospect of system-level integration [9], must equal or surpass the low power consumptions (~10 mW) *and* low nois figure (<3 dB) of the bipolar and GaAs circuits to be competitive with them.

In this paper, we describe 5 GHz band CMOS LNA's on thin substrate (~ 20 μm) and normal (750 μm) substrates. It is found that the noise figure (2.17 dB) of the LNA on the thin substrate is better than that (3 dB) of the LNA on the normal substrate because of the reduction of substrate noise. Both nose figures are the-state-of-the-art values of all CMOS LNA's operating at 5 GHz band. The excellent performance of our LNA is attributed to the careful selection of device size based on the methodology we developed. Our LNA was implemented in a standard 0.25 μm CMOS technology provided by a commercial foundry.

Circuit design

The schematic of our LNA is shown in Figure 1, which consists of a cascode amplifier with a source degenerative inductor L_S used for simultaneous input and noise matching. Inductors L_1 and L_2 and capacitor C_{out} are used for output matching. By extending the noise theory for an FET *without* source inductor published by Pucel *et al* [10], we have derived the noise figure F for an FET *with* source and gate inductors. Our results show that F_{min} and R_{opt} are independent of L_S while X_{opt} is reduced when L_S is introduced. That is, Z_{opt} in the Smith chart should follow a constant resistance (R_{opt}) circle with decreasing reactance (X_{opt}) when L_S is increased as shown in Fig. 2, which, to a first order approximation, agrees with the published experimental data [11]. On the other hand, the locus of the complex conjugate of the input impedance, Z_{in}^*, follows roughly a constant reactance curve in a Smith chart when an increasing but small L_S is introduced as is also shown in Fig. 2. The two loci intercept at some point, which represents for the simultaneous impedance and noise matching. If only a single input matching component L_g is desired, then R_{opt} has to be 50 Ω for simultaneously impedance and noise matching as is also shown in Fig. 2. Therefore a method of designing R_{opt} to a desired value by the selection of transistor device size and transconductance is required. According to Pucel's FET noise model [10], R_{opt} is given by

$$R_{opt} = \sqrt{(R_g + R_s)^2 + \frac{(R_g + R_s)g_m + K_r}{K_g \omega^2 C_{gs}^2}} \qquad (1)$$

where R_g and R_s are gate and source parasitic resistances, respectively; g_m is the transconductance; C_{gs} is gate to source capacitance; ω is the radian frequency; and K_g, K_c and K_r are the noise coefficients defined by Pucel *et al* [10]. By plotting $\left[R_{opt}^2-(R_g+R_s)^2\right]\omega^2 C_{gs}^2$ vs $(R_g + R_s)g_m$, a straight line should be obtained. From the slope and the intercept of this line, K_g and K_r can be determined, respectively. Once K_g and K_r are known R_{opt} can be designed to the desired value by the selection of suitable device size (C_{gs}) and bias (g_m).

Experimental Results

The LNA were fabricated in a standard 0.25 μm CMOS mixed-mode process provided by a commercial foundry. g_m and C_{gs} were carefully selected according to (1) to make R_{opt} as close to 50 Ω as possible. L_S is chosen so that $\omega_T L_S$ = 50 Ω for input matching. Fig. 3 shows a die photo of the LNA. This circuit is operated with V_{DD}=2 V.

The measured characteristics of NF versus frequency for the LNA at 10 mW are shown in Fig. 4. Minimum noise figures of 2.17 and 3.0 dB are obtained around the desired frequency 5.25 GHz for the LNA's on the thin and normal substrates, respectively. To our knowledge, these are the lowest noise figures reported to date of all on-chip matched CMOS LNA's operating in 5-GHz band with power consumptions ≤ 12 mW. Our results unequivocally demonstrate that low noise figures and low power consumptions can be achieved simultaneously with on-chip input and output matching networks in CMOS

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technology at 5 GHz band. The lower noise figure achieved by the LNA on a thinner substrate is mainly due to reduction of substrate loss of the gate inductor. Separate measurement of the noise figures on the gate inductor shows a 0.6 dB reduction of noise figure after substrate thinning. Fig.5 shows the characteristics of input return loss (S_{11}) versus frequency for the LNA. Minimum return losses of –45 dB at 5.1 GHz (thin substrate) and –30 dB at 5.3 GHz (normal substrate) are achieved as a result from the right choice of L_S . To our knowledge, the value -45 dB is the lowest input return loss attained for all silicon based LNA's. The in-band (5.15~5.35 GHz) return losses are all below -18 dB, indicating a very good matching even over the band. The measured transducer gain (S_{21}) appears in Fig.6. The gain has peak values of 11.2 dB and 10 dB for thin and normal substrates, respectively. Clearly, S_{21} over the band of interest improves after substrate thinning. One figure of merit is the ratio of gain to dc-power-consumption [1]. The values of gain-to-dc-power-consumption attained by this CMOS LNA are 1.12 (thin substrate) and 1.0 (normal substrate) dB/mW. As can be seen clearly in Table I, the ratios of gain to dc-power-consumption obtained are comparable to other state of the art C-band LNA's shown in Table I. The reverse isolation (Fig.7) for the LNA is quite good with more than 35 dB of isolation for each bias. This is due to the use of the cascode configuration. The measured P_{1dB} and *IIP3* data are shown in Fig. 8. An input P_{1dB} of ~ -8.3 dBm and an *IIP3* of ~ 0.3 dBm were obtained. These results demonstrate that high dynamic range and good linearity have also been achieved. A summary of the measured amplifier characteristics is also included in Table I. Brederlow *et al* [10] has proposed a figure of merit that takes noise figure, IIP3, dc-power-consumption, gain and frequency into account as follows

$$FOM_{LNA} = \frac{Gain[abs] \cdot IIP3[mW]}{P_{sup\,ply}[mW]} \cdot \frac{1}{(NF-1)[abs]} \cdot f[GHz] \quad (2)$$

From Table I, it is clear the FOM_{LNA} of our CMOS LNA are the best reported values among the 5 GHz band CMOS LNA's and are better than or comparable to some of other state-of-art C-bnad LNA's using SiGe HBT or GaAs MESFET technologies.

Conclusion

A method of designing R_{opt} to a desired value by the selection of transistor device size and transconductance is proposed. By setting R_{opt} ~50 Ω, we have demonstrated a 5 GHz-band low noise amplifier in a standard 0.25 μm CMOS process, which is suitable as a first amplifier in a HIPERLAN2 or IEEE 802.11a receiver. This single-stage LNA showed a 2.17 dB NF(thin substrate) and a 3.0 dB NF (normal substrate) at 10 mW with minimum input return losses of -45 dB and-30 dB, respectively. No off-chip components are required for impedance matching. To our knowledge, both LNA's exhibit the state-of-the-art noise performance at 5 GHz band for all CMOS LNA's with on-chip input and output impedance matching networks under low power consumption (≤ 12mW). From both a performance standpoint and a cost standpoint, these experimental results show that CMOS is very competitive with silicon bipolar and GaAs technologies.

Acknowledgement

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Reference

[1] K. W. Kobayashi, A. K. Oki, L. T. Tran, and D. C. Streit, "Ultra low dc power GaAs HBT S- and C-band low noise amplifiers for portable wireless applications," *IEEE Trans. Microwave Theory Tech.*, vol.MTT-43, pp.3055-3061, Dec. 1995.

[2] U. Lott, "Low dc power monolithic low noise amplifier for wireless applications at 5 GHz," *IEEE Microwave and Millimeter-Wave Monolithic Circuits Symposium*, pp.81-84, 1998.

[3] S. Yoo, D. Heo, J. Laskar and S. S. Taylor, "A C-band low power high dynamic range GaAs MESFET low noise amplifier," *IEEE Microwave and Millimeter-Wave Monolithic Circuits Symposium*, pp.81-84, 1999.

[4] J. J. Kucera and U. Lott, "A 1.8 dB noise figure low dc power MMIC LNA for C-band," *IEEE GaAs IC Symposium*, pp.221-224, 1998.

[5] M. Soyuer, J-O. Plouchart, H. Ainspan, and J. Burghartz, "A 5.8 GHz 1-V low noise amplifier in SiGe bipolar technology," *IEEE Radio Frequency Integrated Circuits Symposium*, pp.19-22, 1997.

[6] H. Samavati, H. R. Rategh, and T. Lee "A 5-GHz CMOS wireless LAN receiver front end, " *IEEE J. Solid-State Circuits*, vol.35, pp.765-772, May 2000.

[7] E. Westerwick, "5-GHz band CMOS low noise amplifier with a 2.5 dB noise figure," *IEEE International Symposium on VLSI Technology, Systems, and Application*, pp.224-227, 2001.

[8] T. P. Liu and E. Westerwick, "5-GHz CMOS radio transceiver front-end chipset, " *IEEE J. Solid-State Circuits*, vol.35, pp.1927-1933, Dec. 2000.

[9] B. A. Floyd, J. Mehta, C. Gamero, and K. O. Kenneth, "A 900-MHz, 0.8-μm CMOS low noise amplifier with 1.2-dB noise figure," *CICC Proc.*, pp.661-664, 1999.

[10] R. A. Pucel, H. A. Haus, and H. Statz, "Signal and noise properties of gallium arsenide field effect transistors," in *Advances in Electronics and Electron physics*, Vol.38, L. Morton, Ed. New York: Academic Press, pp.195-265, 1975.

[11] M. Aikawa, T. Oohira, T. Tokumitsu, T. Hiroda, and M. Muraguchi, *Monolithic Microwave Integrated Circuits* (in Japanese). Tokyo: EIC, p.90, 1997.

[12] D. Allstot, "Low noise amplifiers"Short Course *IEEE International Solid-State Circuits Conference*, Feb. 2001.

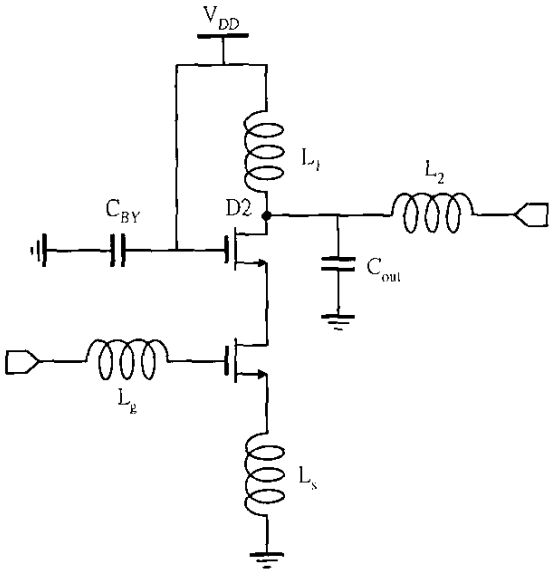

Fig. 1. The schematic of the LNA.

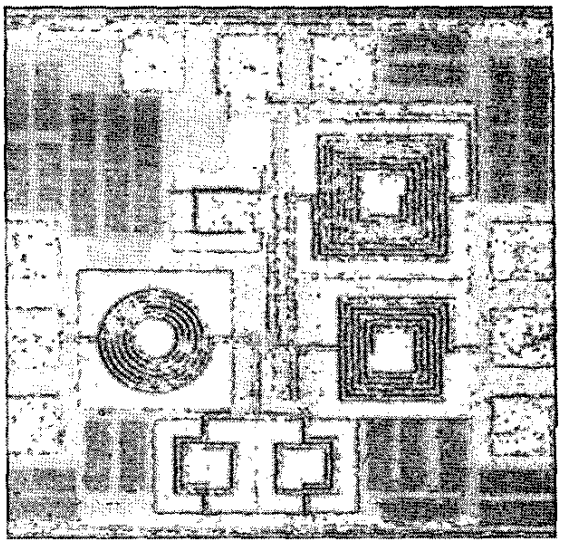

Fig. 3. The die photo of the LNA.

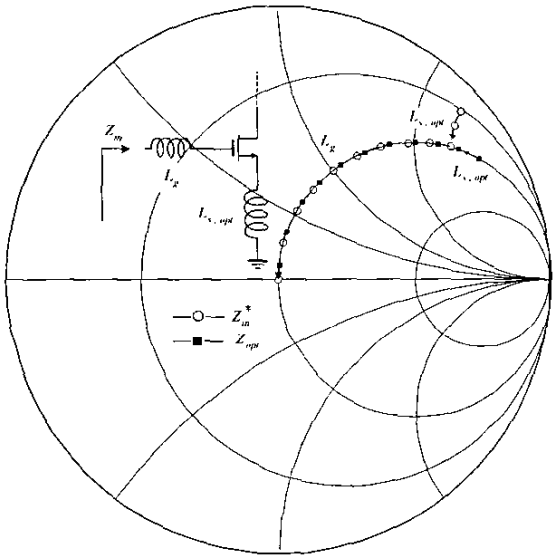

Fig. 2. The loci of Zopt and Zin* in the Smith chart with increasing Lg and Ls.

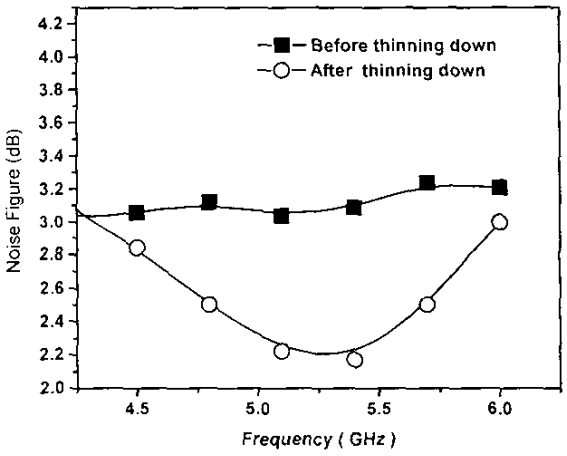

Fig. 4. The characteristics of NF versus frequency.

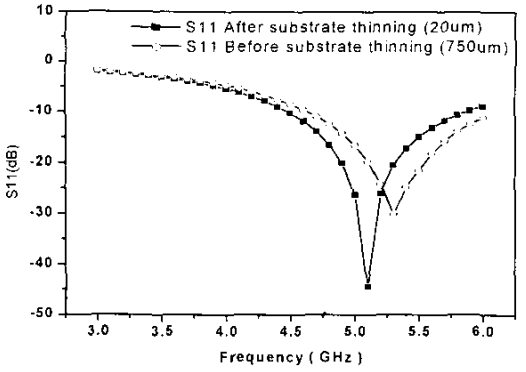

Fig. 5. The measured characteristics of input return loss (S_{11}) versus frequency

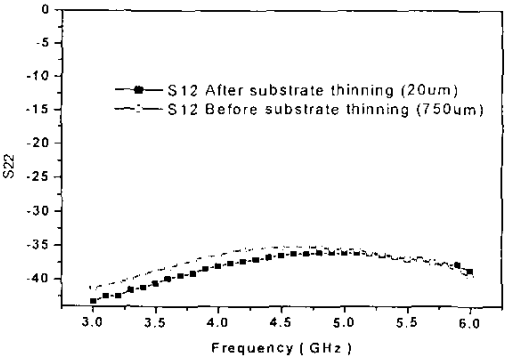

Fig. 7. The measured isolation (S_{12}).

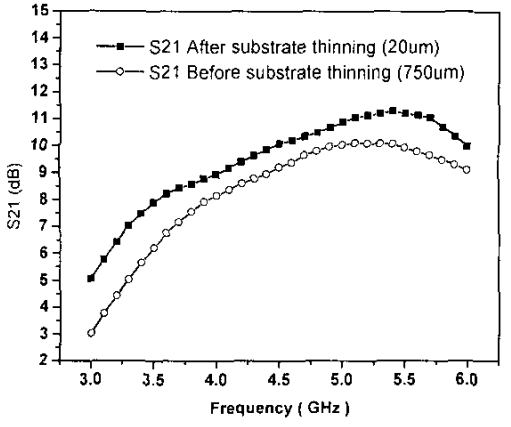

Fig. 6. The measured transducer gain (S_{21}).

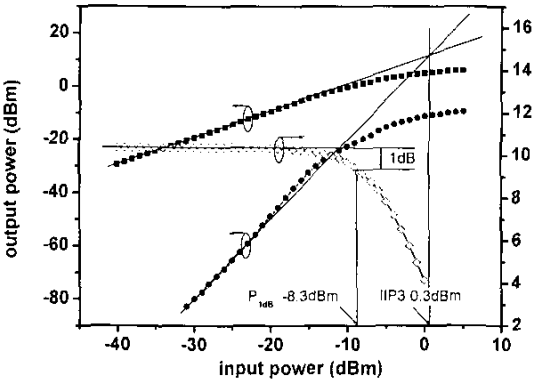

Fig. 8. The measured compression point input P_{1dB} and IIP3.

Table I. Summary of state-of-the-art C-band LNA's

Ref	Substrate thickness	fc	NF	P_{DC}	Gain/P_{DC}	Gain	input return loss	IIP3	P_{1dB} (input)	FOM
	um	(GHz))	(dB)	(mW)	(dB/mW)	(dB)	(dB)	(dBm)	(dBm)	
(CMOS)	20	5.2	2.17	10	1.1	11	-45	0.3	-8.3	3.12
This work	750	5.2	3	10	1	10	-30	0.3	-8.3	1.81
MESFET[2]		5.5	3.5	9.9	1.5	14.85			-21	
MESFET[3]		5	1.9	13.2	0.833	10.9	-21	5		7.84
MESFET[4]		5	1.8	6	2.75	16.5	-16	-6	-16	2.72
SiGe HBT[5]		5.8	2.1	13	1	13	-6	-10.5	-21	0.28
CMOS[6]		5	5.5	3.6	5	18	-12			
		5	3.5	12	0.81	9.72	-10.9	-1.5	-8.7	0.73
CMOS[8]		5	5.3	6	0.9	5.4	-10.4	-3.5	3.3	0.29