Monolithic InGaP-GaAs HBT receiver front-end with 6 mW DC power consumption for 5 GHz band WLAN applications

K.-Y. Yeh, S.-S. Lu and Y.-S. Lin

A very low power consumption (6 mW) 5 GHz band receiver front-end using InGaP-GaAs HBT technology is reported. The receiver front-end is composed of a cascode low noise amplifier followed by a double-balanced mixer with the RF transconductor stage placed above the Gilbert quad for direct-coupled connection. The RF band of this receiver front-end is set to be 5.2 GHz, being downconverted to 1 GHz IF frequency. Input-return-loss (S_{11}) in RF port smaller than −12 dB and excellent power-conversion-gain of 35.4 dB are achieved. Input 1 dB compression point (P_{1dB}) and input third-order intercept point (IIP3) of −24 and −3 dBm, respectively, are also achieved.

Introduction: Among the many versions of 5 GHz band receiver front-ends [1, 2], the topology with the RF transconductor stage of the mixer placed above the Gilbert quad makes the DC level of the cascode low noise amplifier (LNA) output, which is close to the supply voltage, easier to be direct-coupled to the RF input of the mixer [1]. This kind of circuit has been fabricated by CMOS technology with excellent performance [1]. Recently, InGaP-GaAs HBT technology has attracted much attention because of its uniformity [3, 4] and reliability [5]. However, no detailed accounts of the performance of the InGaP-GaAs HBT receiver front-end with this topology have been reported in the literature. Therefore, in this Letter, we present a very low power consumption (6 mW) 5 GHz band monolithic receiver front-end with a similar topology using InGaP-GaAs HBT technology.

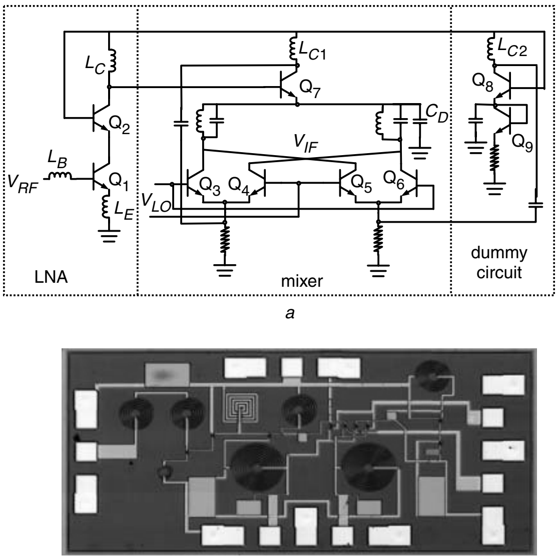

Fig. 1 *Complete circuit, and die photograph of 5 GHz band InGaP-GaAs HBT monolithic receiver front-end*

a Complete circuit
b Die photograph

Circuit design: A complete circuit of the designed 5 GHz band monolithic GaInP-GaAs HBT receiver front-end is shown in Fig. 1*a*. This circuit has several characteristics. First, the RF transconductor stage of the double-balanced mixer is placed above the Gilbert quad to achieve direct-coupled connection. The DC quiescent current of the RF stage can be reused by the switch pairs of the mixer and hence reduction of power consumption of the switch pairs can be achieved. Secondly, a dummy circuit is added for symmetry. Thirdly, the decoupling capacitor C_D, which provides a virtual ground in current-reusing technique, should be large enough to suppress the RF–IF feedthrough of the mixer. The load stage of the mixer is a couple of LC tanks designed for a fixed IF frequency of 1 GHz. The choice of 1 GHz high IF frequency makes this mixer suitable for sliding IF heterodyne architecture [6] and may eliminate the need for the off-chip image rejection filter [6]. Note that, although the circuit topology we use here is very similar to that of the previous report [1], the philosophy of frequency planning is totally different. In [1], the frequency of the local oscillator (LO) is 2.6 GHz, while in this Letter, the LO frequency is 4.2 GHz.

The input impedance matching of the LNA at frequency $\omega_0 = 5.2$ GHz could be achieved by appropriately selecting the values of L_E, L_B and C_π and g_m of Q_1. The load inductor L_C of the LNA and the imaginary part of the input impedance of the mixer were designed to form an LC tank, which resonated at frequency $\omega_0 = 5.2$ GHz. The RF signal passing through the LNA was sent to the RF stage Q_7 of the mixer, and then was fed into the switch pairs for frequency down-conversion. The other RF input was AC ground provided by the dummy circuit. The frequency-dependent property of L_{C1} and L_{C2} also determined the conversion gain and linearity of the overall circuit.

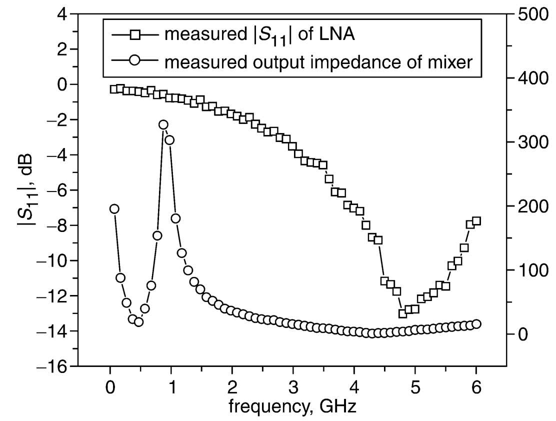

Fig. 2 *Measured input-return-loss S_{11} in RF port and output impedance in IF port of 5 GHz band InGaP-GaAs HBT monolithic receiver front-end*

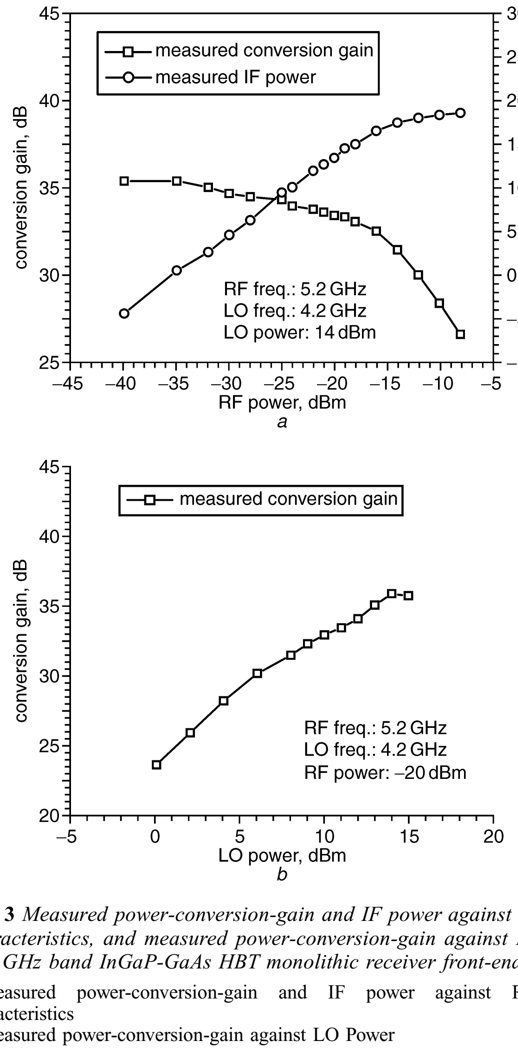

Fig. 3 *Measured power-conversion-gain and IF power against RF power characteristics, and measured power-conversion-gain against LO power of 5 GHz band InGaP-GaAs HBT monolithic receiver front-end*

a Measured power-conversion-gain and IF power against RF power characteristics
b Measured power-conversion-gain against LO Power

Results: The receiver front-end was implemented with a 2 μm GaInP-GaAs HBT process. The die photo of the fabricated GaInP-GaAs HBT receiver front-end is shown in Fig. 1*b*. On-wafer measurement was performed. The total quiescent current consumed was 1.67 mA at supply voltage of 3.6 V. That is to say, it only consumed 6 mW power, a very low value for a monolithic RF receiver front-end. Moreover, the measured LO–IF, RF–LO and RF–IF isolations were 40, 54 and 20 dB, respectively. Input return loss S_{11} in RF port smaller than −12 dB was achieved, as shown in Fig. 2. Also shown in Fig. 2 is the output impedance in IF port of the 5 GHz band InGaP-GaAs HBT monolithic receiver front-end. As can be seen, the measured magnitude at 1 GHz was about 310 Ω, while the peak value (at 900 MHz) was about 330 Ω. As shown in Fig. 3*a*, excellent power conversion gain of 35.4 dB was achieved, high enough for utilising in the RF chain of a system. The corresponding IF powers are also shown in Fig. 3*a*. The maximum power conversion gain was achieved when the input LO power was about 14 dBm, as shown in Fig. 3*b*. Excellent performances in linearity (i.e. P_{1dB} of −24 dBm and IIP3 of −3 dBm (not shown here)) were also achieved. These results are superior to those of its CMOS version (13.75 mW power dissipation, P_{1dB} of −26.5 dBm, and IIP3 of −15 dBm) [1].

Very good results (especially very low power consumption) from this work have proved the potential of InGaP-GaAs HBT technology for future communication systems in want of pre-eminent performance.

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