A Spread-Spectrum Clock Generator With Triangular Modulation

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***Abstract*—In this paper, a spread-spectrum clock generator (SSCG) with triangular modulation is presented. Only a divider and a programmable charge pump are added into a conventional clock generator to accomplish the spread-spectrum function. The proposed circuit has been fabricated in a 0.35-μm CMOS single-poly quadruple-metal process. The proposed SSCG can generate clocks of 66, 133, and 266 MHz with center spread ratios of 0.5%, 1%, 1.5%, 2%, and 2.5%. Experimental results confirm the theoretical analyses.**

***Index Terms*—Phase-locked loops (PLLs), spread spectrum.**

I. Introduction

FASTER operating speeds of electrical devices today result in much electromagnetic interference (EMI) at higher frequencies. Many methods have been used to diminish EMI, such as shielding, pulse shaping, slew-rate control, low-voltage differential clocking, staggering the outputs, special layout techniques, and spread-spectrum clocking. Among these, the spread-spectrum clock generator (SSCG) [1], which is a special case of frequency modulation, can reduce the peak power of the higher order harmonics to reduce EMI effectively. There are three types of SSCGs in the literature. The first type modulates the divider [2], [3] in a phase-locked loop (PLL). The second type modulates the voltage-controlled oscillator (VCO) [4] directly. The third type combines the multiphase outputs of the clock source and the special digital processing circuits to achieve the spread-spectrum function [5]–[7]. In this brief, a conventional PLL-based clock generator can realize the center-spread SSCG with the triangular modulation signal generator being integrated into the low-pass loop filter.

II. Circuit Descriptions

The proposed SSCG is based on a conventional PLL using the proposed method to modulate the VCO directly. Fig. 1 shows the block diagram of the proposed SSCG. The feature of the proposed SSCG is how to generate the modulation signal. In Fig. 1, the reference clock of the PLL uses the divide-by-358 divider to produce a square wave of 40 kHz as the control signal of the programmable charge pump. The schematic of the programmable charge pump is shown in Fig. 2(a). It is composed of a square-wave generator of 40 kHz from Fig. 1 and two programmable current sources. Fig. 2(b) shows one of the programmable current sources. It can generate five kinds of spread ratios (ON1–ON5) in the spread-spectrum mode and zero spread ratio in the nonspread-spectrum mode (SSON).

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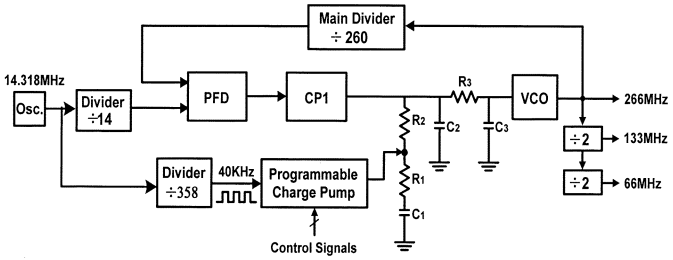
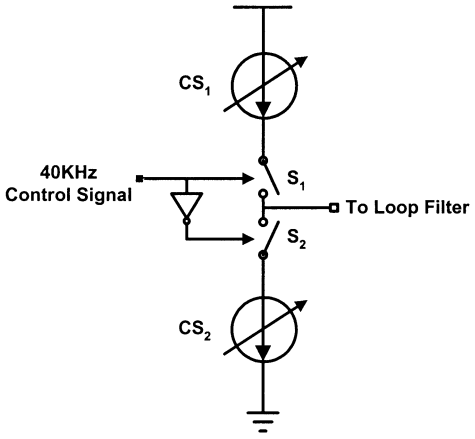
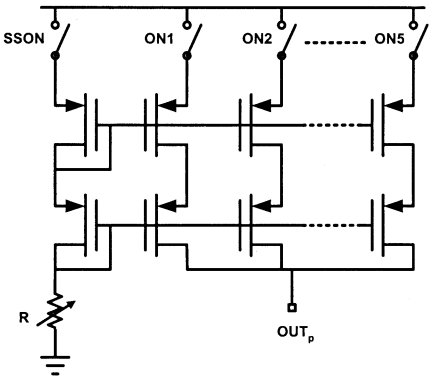


Fig. 1. Block diagram of the proposed SSCG.



(a)



(b)

Fig. 2. (a) Programmable charge pump. (b) Programmable current source.

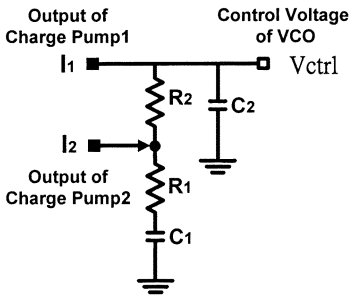


Fig. 3. Second-order filter and both charge pumps in the SSCG.

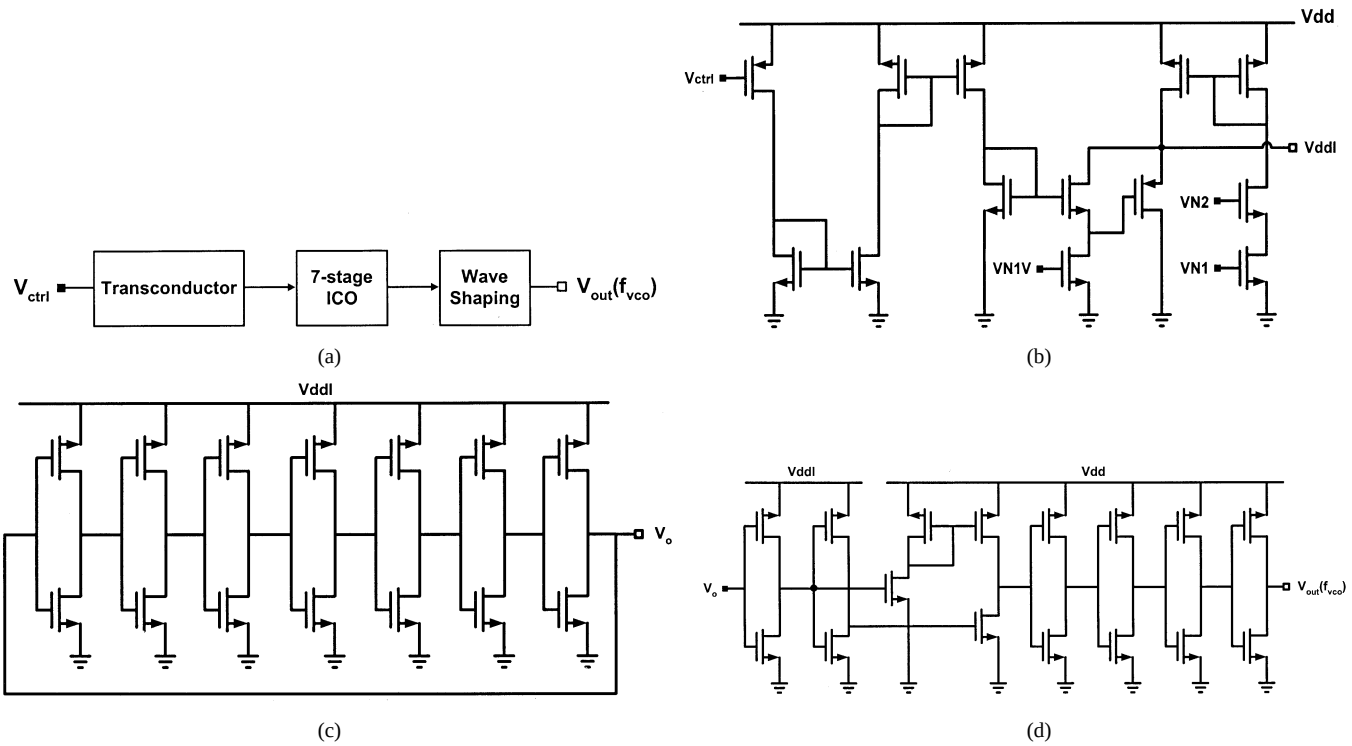


Fig. 4. (a) Block diagram of the VCO. (b) Transconductor. (c) Seven-stage ICO. (d) Wave-shaping buffer.

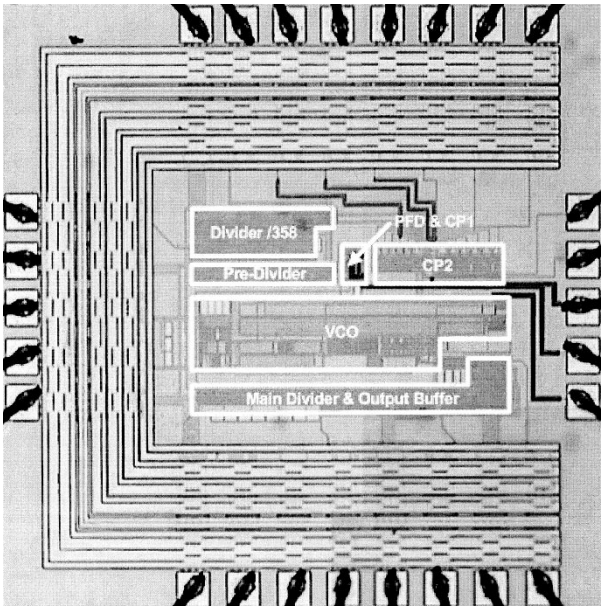


Fig. 5. Microphotograph of the SSCG.

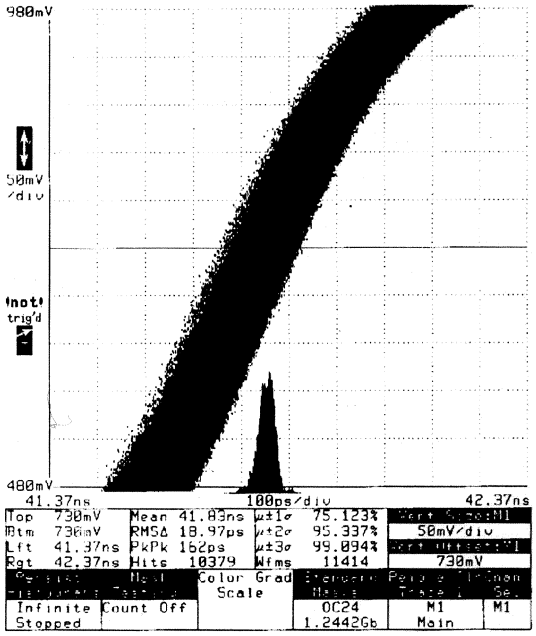


Fig. 6. Measured jitter of the 266-MHz output signal.

In the nonspread-spectrum mode, the programmable charge pump is turned off and this SSCG is a conventional clock generator with the first charge pump as shown in Fig. 1. In the spread-spectrum mode, both charge pumps are turned on. To explain the operation, only a second-order low-pass filter and both charge pumps are shown in Fig. 3. Assume that the SSCG is in the steady state and neglect the first charge pump I_1. The transfer function between the control voltage of the VCO and the programmable charge pump can be expressed as

$$\frac{V_{\text{ctrl}}}{I_2} = \frac{sC_1R_1 + 1}{s\left[s\frac{C_1C_2}{C_1+C_2}\cdot(R_1+R_2)+1\right]}\cdot\frac{1}{C_1+C_2}. \quad (1)$$

Supposing that $R_1C_1 = R_2C_2$, (1) can be rewritten as

$$\frac{V_{\text{ctrl}}}{I_2} = \frac{1}{s(C_1+C_2)}. \quad (2)$$

According to (2) and $R_1C_1 = R_2C_2$, the current I_2 generated by the programmable charge pump will create the periodical triangular modulation signal at the input node of the VCO.

The specified spread ratios can be achieved by appropriately choosing the current I_2. Assume there is a SSCG with the nominal output frequency f_n and the conversion gain K_v of the

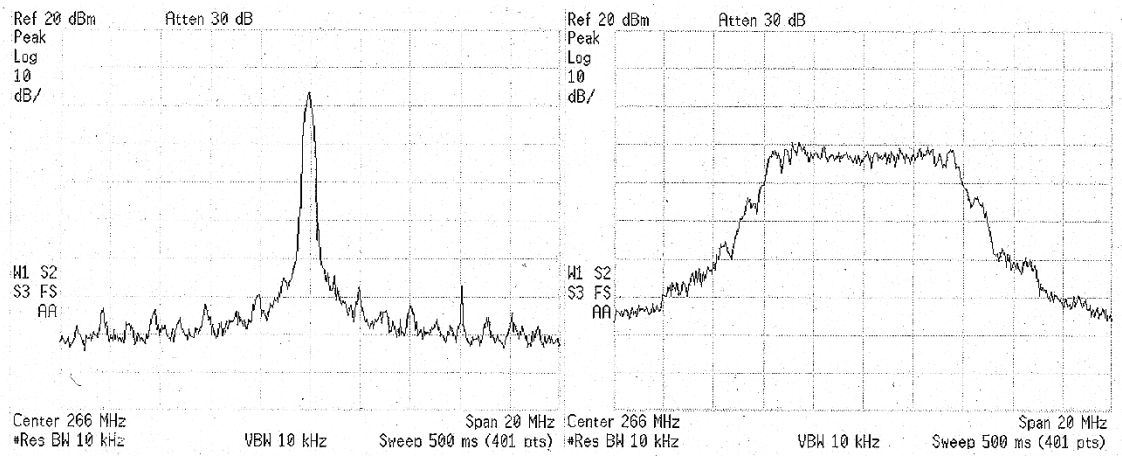


Fig. 7. Measured spectrums of the 266-MHz output signals. (a) Without spread. (b) With 2.5% center spread.

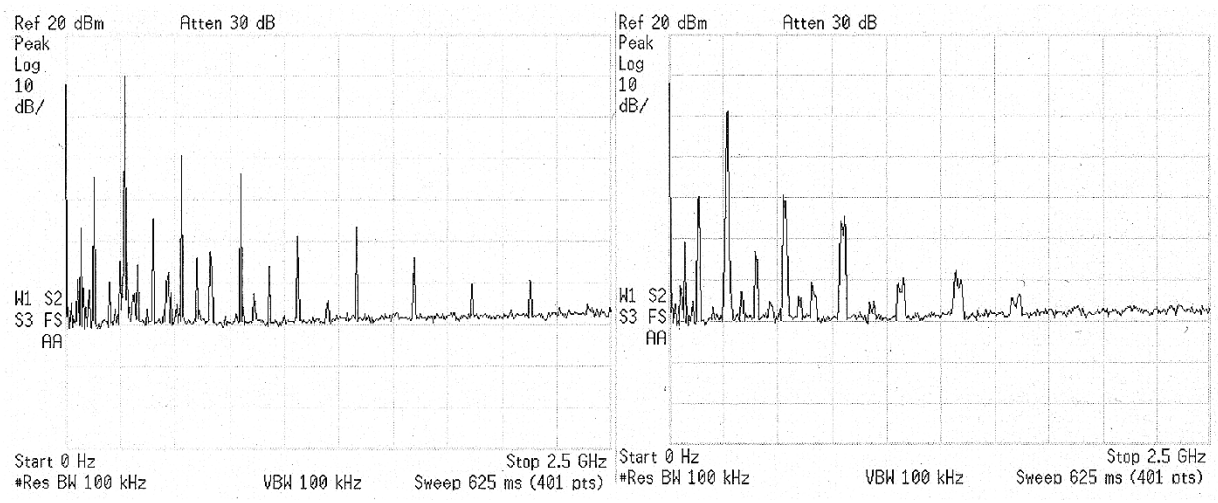


Fig. 8. Measured spectrums (expanded view) of the 266-MHz output signals. (a) Without spread. (b) With 2.5% center spread.

VCO. To supply a spread ratio δ%, the current I_2 can be given as

$$I_2 = \frac{f_n \cdot \delta\% \cdot (C_1 + C_2)}{K_v}. \tag{3}$$

Equation (3) indicates that the variation of K_v will directly change the spread ratio.

The loop bandwidth of the PLL is critical because it influences the modulation profile and the jitter performance. In the PLL, one of the input signals of the phase-frequency detector (PFD) also contains the modulation component. Thus, the bandwidth of this PLL in the nonspread-spectrum mode must be small enough to filter this feedback component generated by the modulation signal. Moreover, to diminish spikes induced by the reference clock, the additional filter, which consists of R_3 and C_3, is added as shown in Fig. 1. The remaining circuits used in this SSCG will be discussed briefly next. The dynamic PFD in [8] is used. The VCO is composed of a transconductor, a seven-stage current-controlled oscillator (ICO), and a wave-shaping buffer. Its diagram and schematic are shown in Fig. 4. Synchronous dividers using static logics are used.

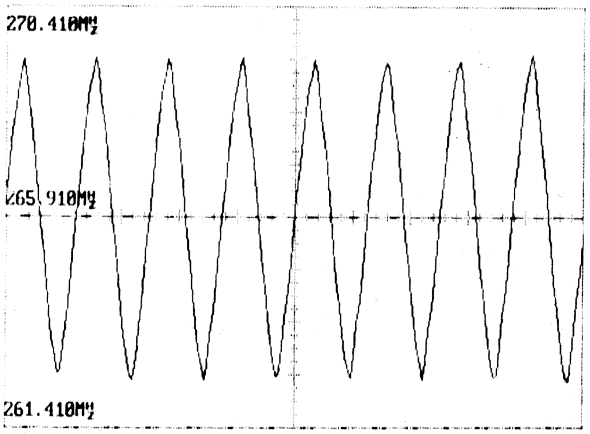


Fig. 9. Modulation profiles of the 266-MHz output signals with 2.5% center spread. The horizontal scale is 30 μs/div.

III. Experimental Results

The proposed SSCG has been fabricated in a 0.35-μm CMOS single-poly quadruple-metal CMOS process. Its

TABLE I
PERFORMANCE SUMMARY

Modulation Method	Modulation on VCO
Modulation Profile	Triangular
Modulation Type	Center-spread
Output Frequency	66/133/266MHz
Input Frequency	14.31818MHz
Open-Loop Bandwidth	130KHz (simulated)
VCO Gain (Kv)	190MHz/V (simulated)
Charge Pump Current (CP1)	1.12mA (simulated)
Modulation Frequency	40kHz
Spread ratios	0.5, 1, 1.5, 2, 2.5%
Loop Filter	R_1 : 66Ω, R_2 : 1KΩ, R_3 :2.2KΩ, C_1 : 0.33μF, C_2: 0.022μF, C_3: 470pF
Chip Area	$1.36\times1.48mm^2$
Supply Voltage	3.3V
Power Dissipation	300mW @ 266MHz including output buffers

microphotograph is shown in Fig. 5. The active area occupies 0.48×0.82 mm^2 and the total area including pads is 1.36×1.48 mm^2. Table I gives the performance summary of the proposed SSCG. The low-pass filter is left off-chip to facilitate measurements. All the components are also listed in Table I. Fig. 6 shows the peak-to-peak jitter of 162 ps for the 266-MHz output in nonspread-spectrum mode. Fig. 7 shows the measured spectrums of the 266-MHz output signals without and with the spread ratio of 2.5%. Fig. 8 shows the expanded views of the 266-MHz output signals without and with the spread ratio of 2.5%. Fig. 9 shows the modulation profile (triangular waveform of 40 kHz) of the 266-MHz output signals with the center spread of 2.5%. This SSCG can provide clock outputs of 66, 133, and 266 MHz with spread ratios of 0.5%, 1%, 1.5%, 2%, and 2.5%.

IV. CONCLUSION

In this brief, the SSCG with triangular modulation on the VCO fabricated in a 0.35-μm CMOS process is presented. The triangular modulation signal is integrated into the low-pass filter of the PLL; thus, both the hardware complexity and the chip area can be reduced. The measured spectrums show that peak amplitudes of each harmonic are attenuated and the proposed architecture does achieve the spread-spectrum function as expected.

ACKNOWLEDGMENT

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