

A 500-MHz–1.25-GHz Fast-Locking Pulsewidth Control Loop With Presetable Duty Cycle

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Abstract—A 500-MHz–1.25-GHz fast-locking pulsewidth control loop (PWCL) with presetable duty cycle is realized in 0.35- μm CMOS technology. The proposed voltage-difference-to-digital converter and switched charge pump circuits reduce the lock time of a conventional PWCL. Compared with the conventional PWCL, the proposed circuit can reduce the lock time by a factor of 2.58. A method to preset the duty cycle of the output clock is also described. Circuit measurements verify that the duty cycle of the output clock can be adjusted from 35% to 70% in steps of 5%.

Index Terms—Duty-cycle presetting, fast locking, pulsewidth control loop (PWCL), switched charge pump, voltage-difference-to-digital converter.

I. INTRODUCTION

TO MEET the demand for high-speed operation today, many systems adopt a double data rate (DDR) technology, such as DDR SDRAM and double-sampling ADC. In these systems, both rising and falling edges of the clock are used to sample the input data, requiring that the duty cycle of the clock be precisely maintained at 50%. Therefore, how to generate a clock with precise 50% duty cycle for high-speed operation is an important issue. Several approaches [1]–[5] can provide 50% duty-cycle clocks. However, open-loop methods [1], [2] that rely on complementary clocks cannot provide immunity to device mismatches. A delay-locked loop (DLL)-based method [3] has the speed limitation in the phase detector. Methods in [4] and [5] suffer from duty-cycle distortion in high-speed operation due to clock mismatches and dc level mismatches, respectively.

The pulsewidth control loop (PWCL) [6], whose architecture is suitable for high-speed application, was proposed to adjust the output duty cycle of the multistage driver. In a PWCL, because of the high gain of the multistage driver, the control voltage must be quiet enough to ensure a precise duty cycle as the loop is locked. Since both the rising and falling edges of the input clock contribute to the jitter, the duty-cycle variation can be twice the peak-to-peak jitter. For these reasons, the loop gain must be kept low, however, with low gain the loop may take a long time to settle. This long settling time reduces the timing budget for other function blocks in a system. Although the proposed phase-fixed PWCL [7] was intended to be used with a DLL/PLL, the same problem will occur when a precise duty cycle is required.

This paper proposes using a new approach to achieve a fast-locking and duty-cycle-presetable PWCL. The operation of the circuit is investigated in Section II where new circuit models and design equations are developed. The design approach for a fast-locking PWCL is described in Section III. Section IV discusses the design issues of duty-cycle setting. The experimental results are illustrated in Section V. Finally, conclusions are presented in Section VI.

II. TRANSIENT ANALYSIS OF THE CONVENTIONAL PWCL

The conventional PWCL [6] is shown in Fig. 1(a). In order to design a fast-locking PWCL, the transient mechanism must be investigated. To simplify analysis, V_c is initialized to V_{dd} and V_r is initialized to its equilibrium voltage, V_{ref} . Based on this condition, the transient response of the control voltage V_{ctl} can be sketched in Fig. 1(b). As shown in the figure, there are four regions in the transient. The behavior of each region can be described as follows.

A. Nonlinear Region

In this region, because the voltage difference between V_c and V_r is very large, the amplifier is saturated and the control voltage V_{ctl} is the lower bound voltage V_{lb} of the differential pair. Thus, under these conditions clock_{out} is always high. The circuit operation in this region can be modeled as shown in Fig. 2(a). The parameters I_{cp2} and C model the second charge pump and the loop filter, respectively. Throughout this region, the control voltage is always V_{lb} .

B. Linear Region

As V_c is discharged, the input voltage difference becomes small enough to allow the amplifier to operate in the linear region, and the transient enters the linear region. In this region, although the control voltage V_{ctl} increases gradually, clock_{out} remains at a high level. A circuit model for this region is shown in Fig. 2(b) where the factor A_0 is the dc gain of the amplifier. If the output common-mode voltage of the amplifier is defined as V_{cm} , then V_c at the end of this region can be expressed as

$$V_{c,final} = V_{ref} + \frac{2 \cdot (V_{cm} - V_{lin})}{A_0} \quad (1)$$

where V_{lin} is the control voltage at which the transient starts to enter the acquisition region. The transient time required for both nonlinear and linear regions can be expressed as

$$t_{n-l} = \frac{C \cdot [V_{dd} - V_{c,final}]}{I_{cp2}} \quad (2)$$

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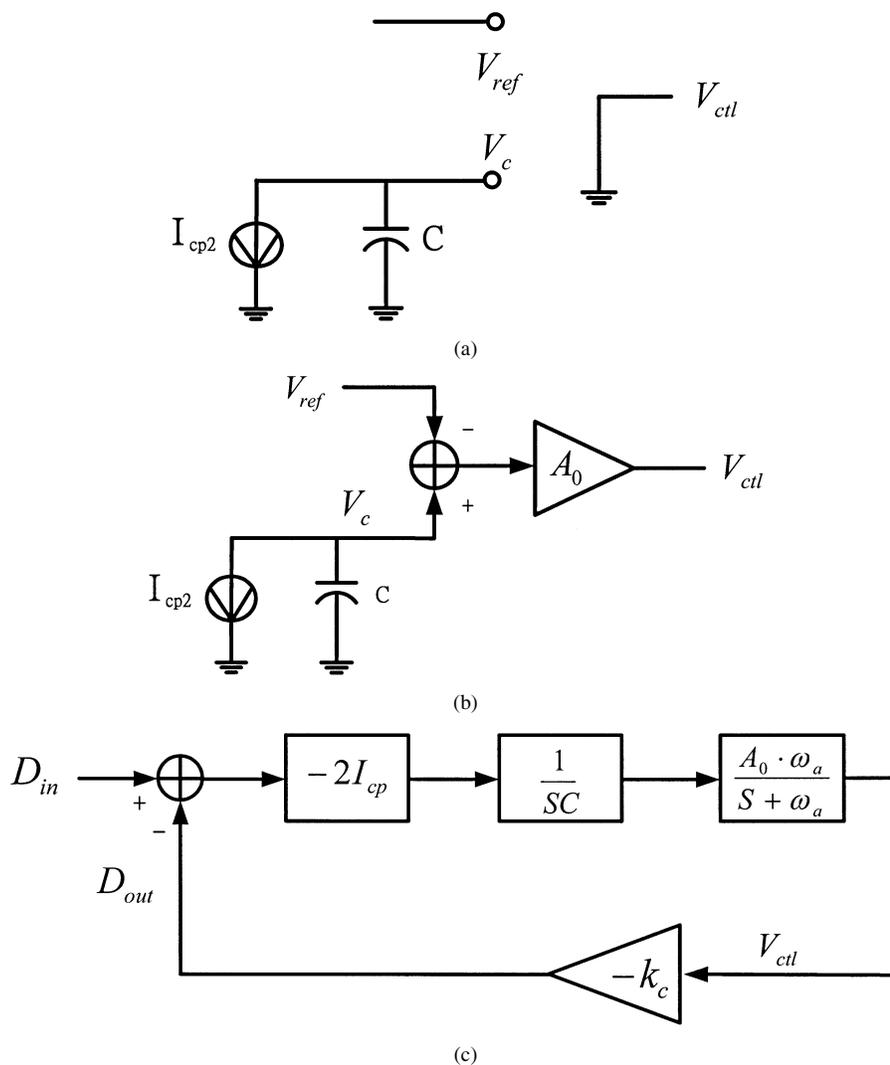


Fig. 2. Circuit models in different regions. (a) Nonlinear region. (b) Linear region. (c) Acquisition region.

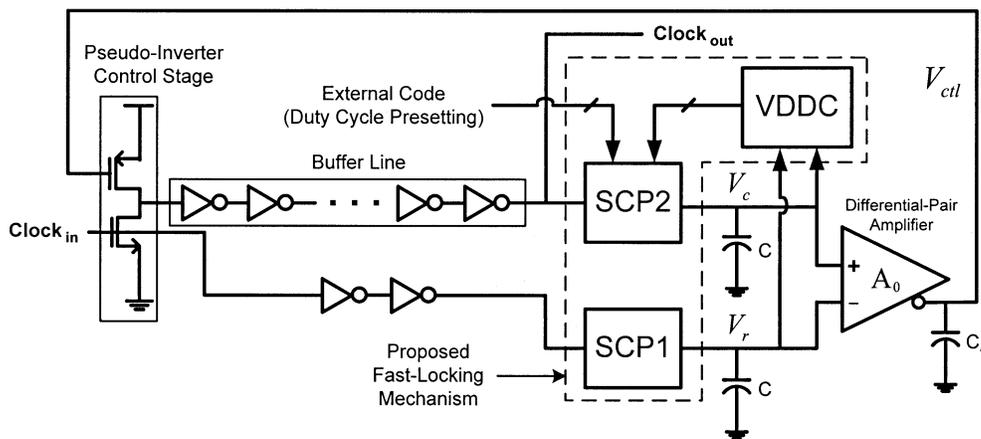


Fig. 3. Proposed fast-locking PWCL.

achieved with the proposed architecture shown in Fig. 3. The fast-locking mechanism is shown enclosed in the dashed line. It consists of a voltage-difference-to-digital converter (VDDC) and a switched charge pump (SCP) circuit. The VDDC is used to

detect the transient region of the four regions discussed in Section II. The SCP circuits provide different charge pump currents corresponding to the control codes from VDDC and the external codes which are used to preset the duty cycle of $clock_{out}$.

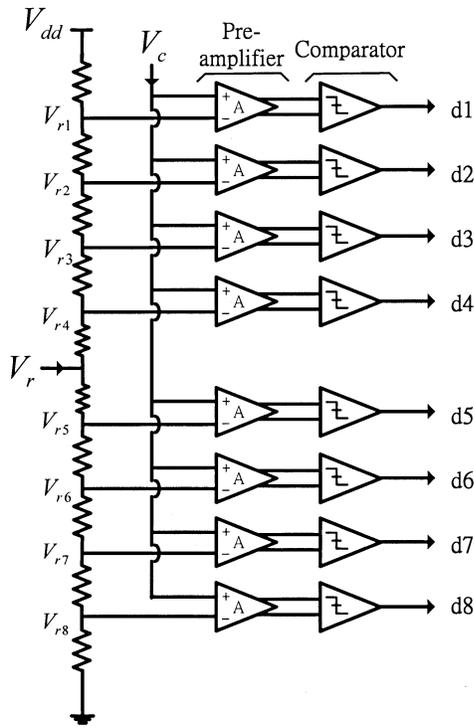


Fig. 4. Voltage-difference-to-digital converter.

A. VDDC

The VDDC is depicted in Fig. 4. It is similar to a flash ADC [9], however, the reference voltage V_r is connected to the middle of the resistor string. Relative to V_r , an additional eight reference voltages, $V_{r1} \sim V_{r8}$, are generated in the resistor string. By comparing these reference voltages with V_c , the output digital codes of the comparators represent the voltage difference between V_c and V_r . The correspondence between the voltage difference and the output code is described as follows. If V_c is greater than V_r , d_5-d_8 are always high and the code of d_1-d_4 is proportional to the voltage difference. On the other hand, if V_r is greater than V_c , then d_1-d_4 are always low, and the code of d_5-d_8 is inversely proportional to the voltage difference. In the locked state, d_1-d_4 are low, and d_5-d_8 are high. Therefore, the regions of the transient can be recognized by these codes. There is a lock window set by V_{r4} and V_{r5} to detect when the loop approaches a locked state. As the voltage difference becomes small enough for V_c to enter the lock window, the fast-locking mechanism will be disabled.

B. Switched Charge Pump

The purpose of the SCP circuit is to provide output current which is proportional to the voltage difference between V_c and V_r . The SCP circuit shown in Fig. 5 is based on the Mu-Svensson charge pump [6] and multiple-path charge pump [10]. If the output bits of the VDDC, d_1-d_8 , are all low, a large constant current is provided. As the code of d_5-d_8 is increased, the output current decreases to correspond to a smaller voltage difference. Until d_1-d_4 are all low and d_5-d_8 are all high, the SCP outputs the minimum current I_{cp} , which is the same as the charge pump current in the conventional circuit. However, as the code of d_1-d_4 is increased, the output current is increased

again to correspond to the larger voltage difference. The magnitude of the current in each current source path is shown in the figure. All 18 currents are represented as a ratio of I_{cp} .

To verify the fast-locking mechanism, the designed case is illustrated as follows. Because the initial voltage of V_c is V_{dd} , the reference voltages used to compare with V_c are $V_{r1}-V_{r4}$. When V_c is greater than V_{r1} , the transient is in the nonlinear region. When the transient is in the linear region, V_c is between V_{r1} and V_{r2} . Reference voltages V_{r3} and V_{r4} are set to speed up the transient in acquisition region. Because the transient time during nonlinear and linear regions dominates the lock time, the following calculation focuses on these two regions and the effect of acceleration in acquisition region is ignored. Assuming the charge pump current corresponding to acquisition region is the same as the charge pump current I_{cp} in locked state, the lock time can be derived as follows:

$$t_{n-l} = C \left\{ \frac{V_{dd} - V_{r1}}{I_{cp,n}} + \frac{V_{r1} - V_{r2}}{I_{cp,l}} + \frac{V_{r2} - V_{c,final}}{I_{cp}} \right\} \quad (6)$$

where $I_{cp,n}$ and $I_{cp,l}$ are the charge pump currents in the nonlinear and linear regions, respectively. Three segments of voltage difference in (6) are designed to be 1.3, 0.25, and 0.1 V, respectively. The remaining parameters are the same as in Section II. The transient time during the nonlinear and linear regions can be calculated as 196 ns. Thus, adding the transient time in the acquisition region, 101.6 ns, the lock time becomes 297.6 ns. This time is less than half that of the conventional lock time, 761.6 ns. Furthermore, if the added charge pump currents are made larger, the lock time can be reduced dramatically.

IV. DUTY-CYCLE PRESETTING DESIGN

Because the ratio of the charge current to the discharge current of the charge pump 2 determines the output duty cycle [6], the duty cycle can easily be set by controlling both currents. There are two ways to set the same current ratio: increasing the charge/discharge current or decreasing the discharge/charge current. Because the former has a larger current difference between the two charge pumps, the resulting jitter is larger. Thus, the later approach is adopted here. In this design, another seven current sources with switches controlled by external code, $d'_1-d'_7$, are added to SCP2 to generate an output clock with duty cycle ranging from 35% to 70% in steps of 5%. The circuit is shown in Fig. 6.

V. EXPERIMENTAL RESULTS

The proposed circuit has been fabricated in 0.35- μm CMOS technology. A microphotograph of the proposed circuit is shown in Fig. 7. The total area of the chip is $0.86 \times 0.32 \text{ mm}^2$ without pads. In this design, the loop filters and the loading capacitors are off-chip. The supply voltage is 3.3 V and the input clock frequency can be 500-MHz–1.25-GHz. For the purpose of comparing fairly and saving chip area, the conventional and proposed architectures are implemented in the same chip with switches switching between the two circuits.

Fig. 8 shows the measured reference and output clocks when the loop is in the locked state. The measured rms jitter shown in Fig. 9 is 3.15 ps. In Fig. 10, the transient responses of the control

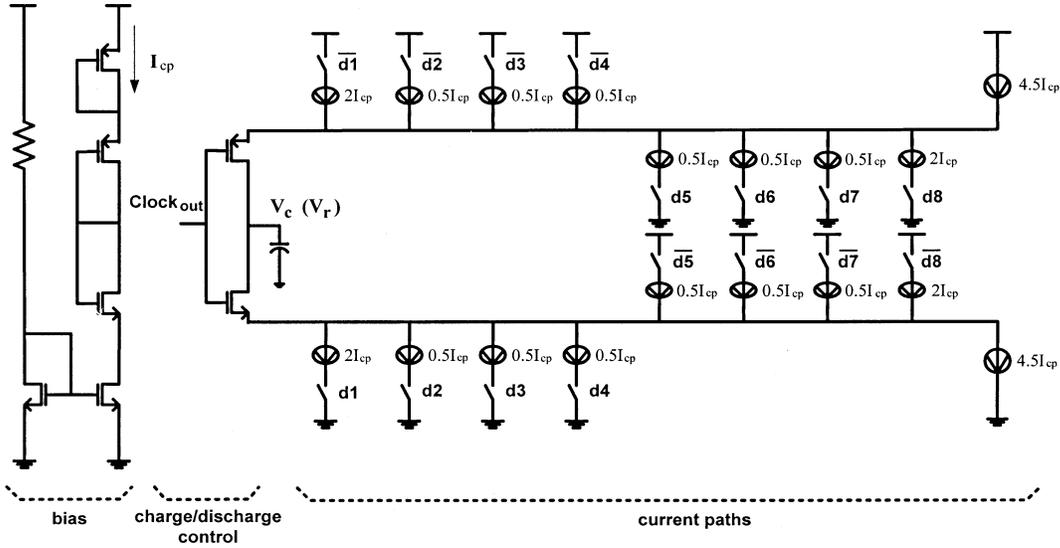


Fig. 5. Switched charge pump circuit.

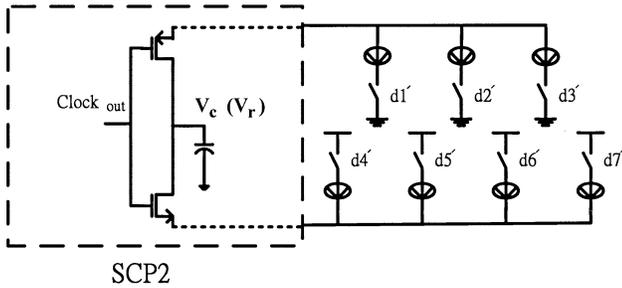


Fig. 6. Duty-cycle presetting current paths.

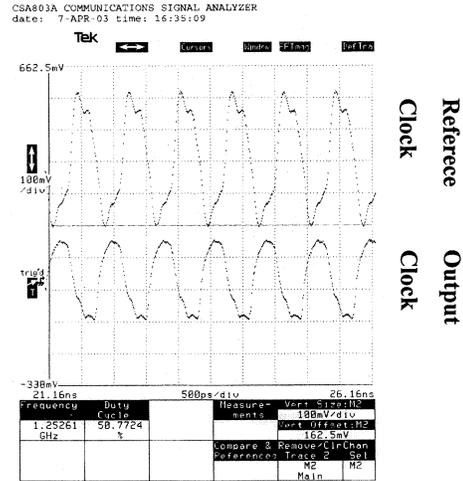


Fig. 8. Output waveform of reference and output signals.

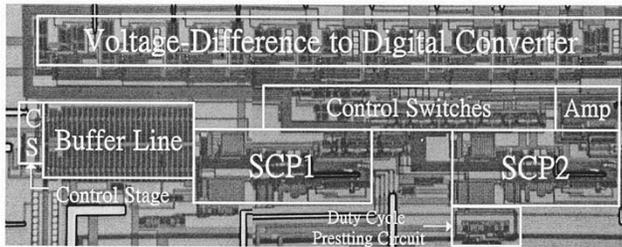


Fig. 7. Chip microphotograph.

voltage in the conventional and proposed circuits are shown together for comparison. When the duty cycle of the output clocks settle to $50\% \pm 0.1\%$, in which the 0.1% duty-cycle variation is the defined lock point in this paper, deduced from the measured waveform of the control voltage, the lock times of the conventional and proposed circuits are 800 and 310 ns, respectively. Consequently, compared with the conventional PWCL, the proposed circuit can reduce the lock time by a factor of 2.58. Fig. 11 shows the preset duty-cycle output waveforms. The measured duty cycles of the output clocks can range from 35% to 70% in steps of 5%. Table I gives a performance summary of this work.

VI. CONCLUSION

This paper describes the proposed methods that can be used to design a fast-locking and duty-cycle-presettable PWCL.

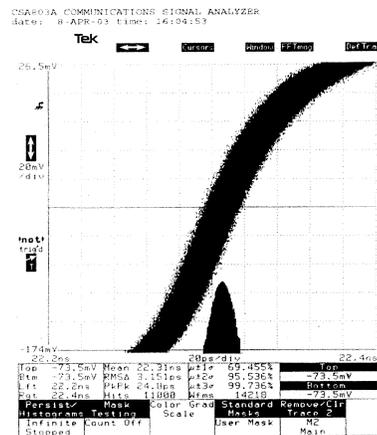


Fig. 9. Output jitter.

First, the operating mechanism of the system is investigated to fully understand system behavior. Second, the system is analyzed to develop accurate system models and design equations

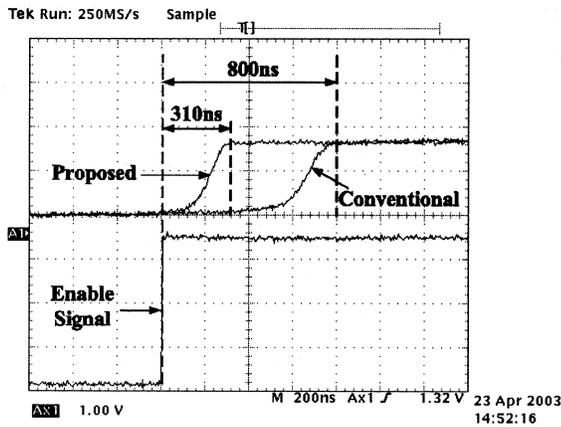


Fig. 10. Transient behavior of the conventional and proposed circuits.

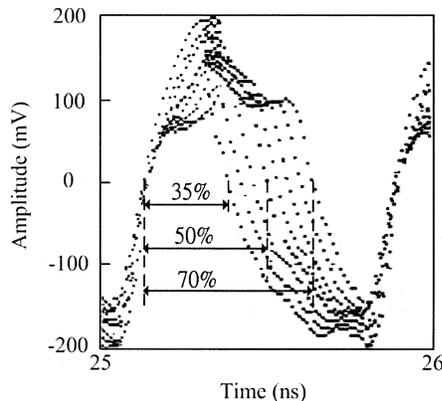


Fig. 11. Output waveforms with different duty cycles.

TABLE I
PERFORMANCE SUMMARY

Technology	0.35 μ m, 1-poly, 4-metal CMOS
Supply Voltage	3.3V
Frequency Range	500MHz~1.25GHz
Lock Time (Conventional)	800ns
Lock Time (Proposed)	310ns
Output Duty Cycle Range	35%~70% (@ a step of 5%)
Core Size	0.86*0.32 mm ²
Power Consumption	270 mW

to mathematically estimate the amount of improvement by the proposed method. Finally, the design issues associated with preset duty cycle are discussed. From the measurement results, the proposed circuit increases the lock speed by a factor of 2.58 times over the conventional circuit. Further, the lock speed of the system can be improved if the additional currents are increased.

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