$(Al_xGa_{1-x})_{0.5}In_{0.5}P/In_{0.15}Ga_{0.85}As$ $(x = 0, 0.3, 1.0)$ Heterostructure Doped-Channel FETs for Microwave Power Applications

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***Abstract*—The quaternary $(Al_xGa_{1-x})_{0.5}In_{0.5}P$ $(0 \leq x \leq 1)$ compounds on GaAs substrates are important materials used as a Schottky layer in microwave devices. In this report, we systematically investigated the electrical properties of quaternary $(Al_xGa_{1-x})_{0.5}In_{0.5}P$ materials and concluded that the best composition for improving the device performance is by substituting 30% $(x = 0.3)$ of Ga atoms for Al atoms in GaInP material. The Schottky barrier heights (ϕ_B) of $(Al_xGa_{1-x})_{0.5}In_{0.5}P$ layers were $0.85 \sim 1.00$ eV. We successfully realized the $(Al_xGa_{1-x})_{0.5}In_{0.5}P/In_{0.15}Ga_{0.85}As$ $(x = 0, 0.3, 1.0)$ doped-channel FETs (DCFETs) and demonstrated excellent dc, microwave, and power characteristics.**

***Index Terms*—AlGaInP, doped-channel FET, rf power performance.**

I. Introduction

ELECTRICAL performance of Schottky contacts in heterostructure FETs is an important key factor associated with the device characteristics. In recent years, pseudomorphic heterostructure field effect transistors (HFETs) fabricated by the AlGaAs/InGaAs/GaAs material system are well established and evidenced a superior microwave performance. However, the conduction band offset (ΔE_c) of AlGaAs/GaAs heterojunction is limited by the aluminum composition, which should be limited below 23%, to prevent the presence of donor-related complex (DX) centers and the ineffective donor activation [1]. This results in the constraint of Schottky diode performance and subsequently degrades the device characteristics. As compared with the conventional AlGaAs/GaAs heterojunction system, an alternative system, $(Al_xGa_{1-x})_{0.5}In_{0.5}P$ lattice-matched GaAs quaternary compounds, is expected to substitute AlGaAs material as a Schottky layer. This material system provides many key figures to enhance device performance, such as a lower gate leakage current, a higher breakdown voltage, a better current drive capability [2], [3], and a more controllable gate-recess etching process.

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Therefore, in this study, we first systematically grew and characterized various $(Al_xGa_{1-x})_{0.5}In_{0.5}P$ $(0 \leq x \leq 1)$ quaternary compounds. The Schottky barrier height (ϕ_B) of these quaternary compounds were investigated. Secondly, in order to obtain a high-process uniformity, the reactive ion etching (RIE) technology was applied to characterize the etching properties of the AlGaInP materials. Finally, we used this high quality $(Al_xGa_{1-x})_{0.5}In_{0.5}P$ quaternary material system as a Schottky layer, combining a super transport $In_{0.15}Ga_{0.85}As$ doped channel, to realize the $(Al_xGa_{1-x})_{0.5}In_{0.5}P/In_{0.15}Ga_{0.85}As$ double doped-channel FETs (DCFETs), and evaluated their dc and microwave power performances. DCFETs, based on our previous studies, have achieved excellent device linearity, current density, and breakdown voltage, as compared with PHEMTs, which are the important factors for device power applications [4].

II. $(Al_xGa_{1-x})_{0.5}In_{0.5}P$ Device Growth

The $(Al_xGa_{1-x})_{0.5}In_{0.5}P/In_{0.15}Ga_{0.85}As$ DCFETs heterostructures, as shown in Fig. 1, were grown by a gas-source molecular beam epitaxy (GSMBE) system on (100)-oriented semi-insulating GaAs substrates. In order to achieve an abrupt interface between phosphide and arsenide compounds, an optimum group V gas pump-out time was applied during the growth of the epilayers [5]. Two 150 Å thick pseudomorphic $In_{0.15}Ga_{0.85}As$ doped channels $(n = 3 \times 10^{18})$ were grown on top of a 3000 Å undoped GaAs buffer layer, and a 30 Å undoped GaAs layer was inserted into these two $In_{0.15}Ga_{0.85}As$ channels. In order to study the device influenced by different Schottky layers, various aluminum composition of $(Al_xGa_{1-x})_{0.5}In_{0.5}P$ compounds $(x = 0, 0.3, 1)$ were grown on top of the channel. Finally, a 200 Å n^+-GaAs cap layer $(n = 5 \times 10^{18})$ was used to improve the ohmic contacts. Table I shows the Hall measurement results without the cap-layer removal. The mobilities were around $1150 \sim 1230$ cm^2/V-s with sheet charge densities from 1.5×10^{13} to 1.6×10^{13} cm^{-2} at 300 K. The carrier mobilities seem not to be affected at cryogenic temperatures, where the impurity scattering dominates the transport mechanism. Although the mobilities are relatively lower in doped-channel as compared with modulation-doped design, an efficient carrier modulation combining with a higher sheet charge density can still guarantee a high current density and a high modulation gain in the channel [4].

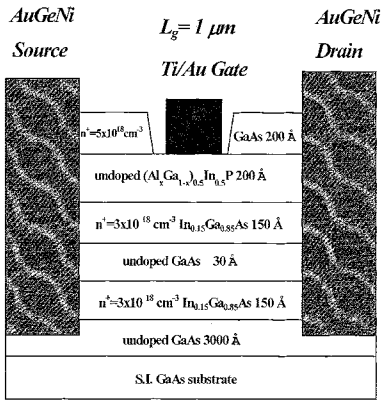

Fig. 1. Device cross section of $(Al_xGa_{1-x})_{0.5}In_{0.5}P/In_{0.15}Ga_{0.85}As$ $(x = 0, 0.3, 1.0)$ DCFETs.

TABLE I
HALL MEASUREMENT RESULTS OF $(Al_xGa_{1-x})_{0.5}In_{0.5}P$ COMPOUNDS AT 300 K AND 77 K

Al composition	300 K		77 K	
	Mobility (cm^2/V-sec)	Sheet charge density(cm^{-2})	Mobility (cm^2/V-sec)	Sheet charge density(cm^{-2})
x=0	1232	$1.5x10^{13}$	1345	$1.48\ x10^{13}$
x=0.3	1164	$1.57\ x10^{13}$	1441	$1.26x10^{13}$
x=1	1156	$1.62\ x10^{13}$	1266	$1.58x10^{13}$

III. OPTIMUM REACTIVE ION ETCHING OF $(Al_xGa_{1-x})_{0.5}In_{0.5}P$ FOR GATE RECESS

RIE etching experiments for the gate recess process were conducted by a SAMCO RIE-10 N system. In this etching study, the gas mixture of BCl_3 and CHF_3 was applied to investigate the etching characteristics between $(Al_xGa_{1-x})_{0.5}In_{0.5}P$ and GaAs materials. The RF power was operated at 50 W under a chamber pressure of 50 mtorr.

Fig. 2(a) illustrates the etching rates of quaternary $(Al_xGa_{1-x})_{0.5}In_{0.5}P$ $(x = 0, 0.3, 1)$ compounds by using the $BCl_3 + CHF_3$ gas mixture, where the flow rates of CHF_3 were varied from 0 to 12 sccm. The flow rate of BCl_3 was fixed at 12 sccm. From Fig. 2(a), the etching rates of Al-rich $(x = 1)$ compounds decreased more dramatically with the increase of CHF_3 flow rates, namely 7.5 nm/min for $x = 1, 17.8$ nm/min for $x = 0.3$, and 23 nm/min for $x = 0$ at a $BCl_3 : CHF_3 = 12 : 12$ mixing condition. However, the etching rate of Al-free compound, i.e., $In_{0.5}Ga_{0.5}P$ $(x = 0)$, is relatively independent of the flow rate of CHF_3. These phenomena, as interpreted, are due to the formation of a C_xF_y passivation layer and nonvolatile AlF_3 products, which retard the etching process in higher Al content materials [6], [7]. By increasing the CHF_3 gas flow rates from 0 sccm to 12 sccm, the etching rate change of $Ga_{0.5}In_{0.5}P$ material is insignificant, which is around 24 nm/min. The maximum etching selectivity of quaternary compounds versus GaAs material, shown in Fig. 2(b), is 45 $(BCl_3 : CHF_3 = 12 : 12)$ for $Al_{0.5}In_{0.5}P$, and this value drops in Ga-rich compounds. The maximum etching selectivity for $Ga_{0.5}In_{0.5}P$ is 15. As far as the etching rate and selectivity are concerned, we conclude that the gas mixture ratio of $BCl_3 : CHF_3 = 12 : 8$ is suitable for the gate-recessed process.

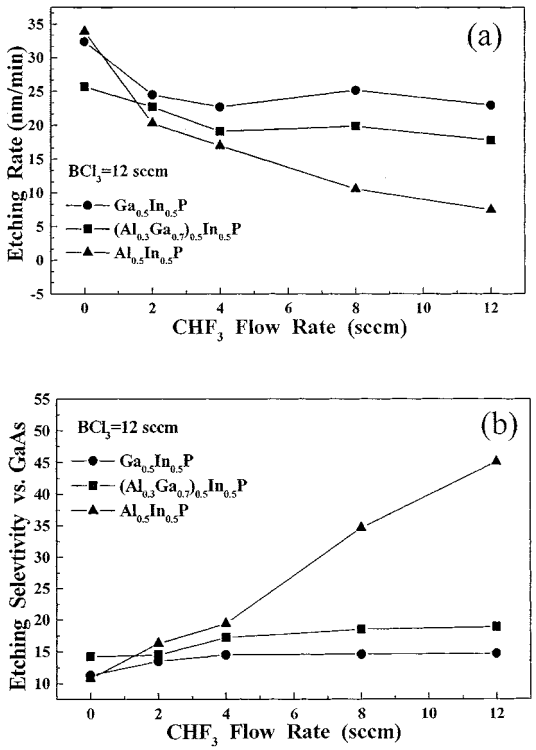

Fig. 2. (a) RIE etching rates and (b) selectivities versus GaAs of various $(Al_xGa_{1-x})_{0.5}In_{0.5}P$ quaternary compounds versus CHF_3 flow rates at a BCl_3 flow rate of 12 sccm.

IV. DEVICE FABRICATION

AlGaInP/InGaAs DCFETs were processed by conventional optical lithography and lift-off technology. Ohmic contacts were realized by using a Au-Ge-Ni alloy followed by a 430 °C, 2 min hot plate annealing. To define an active region, an $NH_4OH/H_2O_2/H_2O$ solution was used for etching GaAs and $In_{0.15}Ga_{0.85}As$ layers, and an $HCl/H_3PO_4/H_2O$ mixed solution was used to remove the $(Al_xGa_{1-x})_{0.5}In_{0.5}P$ layers. As for the critical gate-recessed process, rather than using a traditional wet etching process, we applied the optimum RIE, as just described in the previous section, to achieve a high etching uniformity crossing the wafer. The reactive gas mixture of BCl_3 and CHF_3 (12:8) was applied with an rf power of 50 W and a pressure of 50 mtorr. The etching selectivities of $15 \sim 35$ were obtained between $(Al_xGa_{1-x})_{0.5}In_{0.5}P$ and GaAs materials. After etching away the top n^+ GaAs layer, the wafer was immersed in a buffer HF solution to clean up the surface residual and minimize the damage caused by the RIE process. Finally, 1.0 μm long Ti/Au-gates were deposited by the lift-off process, and a 3000 Å Au metal layer was used for the interconnection level.

V. DEVICE DC AND MICROWAVE POWER CHARACTERIZATION

The 1.0 μm-long gate $(Al_xGa_{1-x})_{0.5}In_{0.5}P/In_{0.15}Ga_{0.85}As$ DCFETs on GaAs were tested on-wafer and characterized by dc and rf measurements. The current–voltage *(I–V)* curves of the $(Al_xGa_{1-x})_{0.5}In_{0.5}P$ $(x = 0, 0.3, 1.0)$ Schottky diodes are shown in Fig. 3. As shown in the figure, the reversed gate-to-drain breakdown voltages (BV_{GD}), defined by a 1

TABLE II
SCHOTTKY DIODE CHARACTERISTICS OF $(Al_xGa_{1-x})_{0.5}In_{0.5}P$ $(0 \leq x \leq 1)$ COMPOUNDS

Schottky Layer	Barrier height (eV)	Turn on voltage* (Volt.)	Breakdown voltage* (Volt.)	Ideality factor
$Ga_{0.5}In_{0.5}P$	0.85	0.8	-7.9	1.38
$(Al_{0.3}Ga_{0.7})_{0.5}In_{0.5}P$	1.00	1.2	-11	1.19
$Al_{0.5}In_{0.5}P$	0.93	1.1	-13.2	1.28

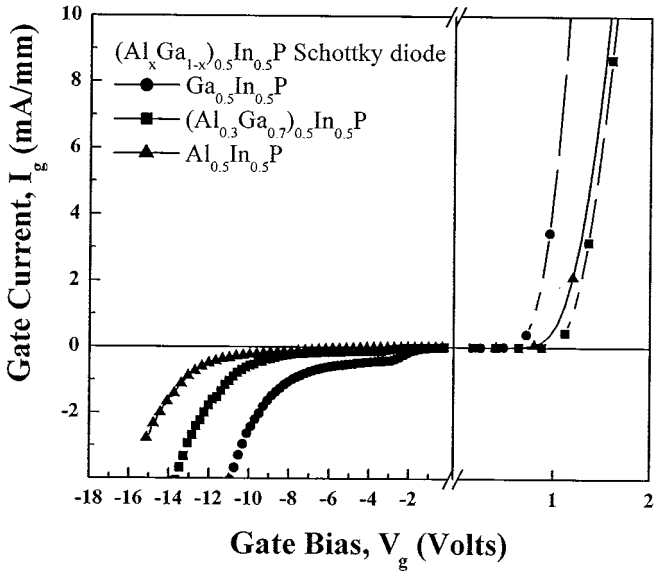

Fig. 3. Schottky diode *I–V* characteristics for different x values of $(Al_xGa_{1-x})_{0.5}In_{0.5}P$ compounds.

mA/mm of gate leakage, were -7.9 V, -11 V and -13.3 V for $x = 0, x = 0.3$ and $x = 1$. Due to a larger energy bandgap in the high Al-content layers, the enhanced performance in the Schottky diode is observed. The turn-on voltage, breakdown voltage, ideality factor, and Schottky barrier height of the Schottky diodes are summarized in Table II. The Schottky barrier height (ϕ_B) of 0.85, 1.00, and 0.93 eV for $Ga_{0.5}In_{0.5}P$, $(Al_{0.3}Ga_{0.7})_{0.5}In_{0.5}P$ and $Al_{0.5}In_{0.5}P$ were extracted by capacitance–voltage *(C–V)* measurements, which are similar to the other reports [8], [9]. The improved Schottky barrier height of $(Al_{0.3}Ga_{0.7})_{0.5}In_{0.5}P$ (1.0 eV) can significantly reduce the gate leakage even at a high gate bias, which will certainly be beneficial to the linearity of device operation. This high ϕ_B also results in a higher turn-on voltage (1.2 V for $x = 0.3$) in diode characteristics. As we can see from Table II, the $(Al_{0.3}Ga_{0.7})_{0.5}In_{0.5}P$ Schottky diode obtained an ideality factor of 1.19, and this value increased to 1.38 and 1.28 for $Ga_{0.5}In_{0.5}P$ and $Al_{0.5}In_{0.5}P$ Schottky diodes, respectively. Although $Al_{0.5}In_{0.5}P$ material demonstrates the highest bandgap (2.33 eV) in this material system, it does not help its Schottky diode performance. In fact, the diode characteristics degrade, which is associated with the formation of Al clusters or an Al-related oxidation problem in this high Al-content material. The undesired interface states associated with these defects result in the pinning of Fermi-level (E_f) and uncontrollable diode performance [10], [11].

The typical drain current-voltage (I_{DS} versus V_{DS}) characteristics of 1.0×100 μm^2 RIE-recessed

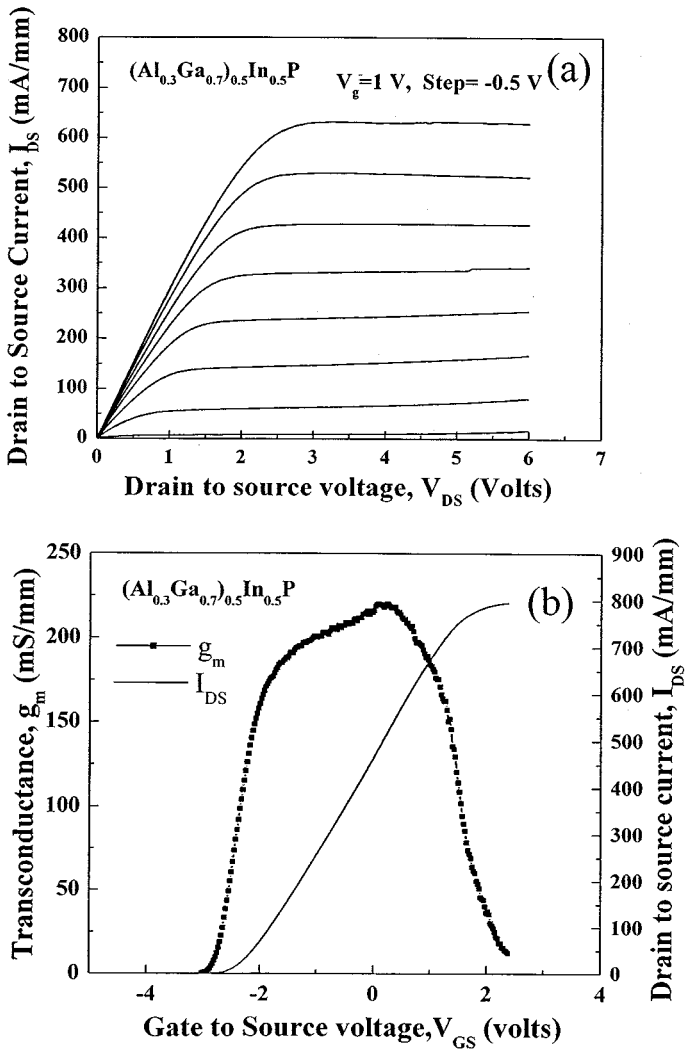

Fig. 4. DC *I–V* characteristics of $(Al_{0.3}Ga_{0.7})_{0.5}In_{0.5}P/In_{0.15}Ga_{0.85}As$ DCFETs with a gate-length of 1.0 μm: (a) I_{DS}–V_{DS} curves, and (b) g_m-I_{DS}–V_{GS} transfer curves.

TABLE III
SUMMARY OF DC CHARACTERISTICS FOR $(Al_xGa_{1-x})_{0.5}In_{0.5}P/In_{0.15}Ga_{0.85}As$ $(x = 0, 0.3, 1.0)$ DCFETs. THE TRANSCONDUCTANCE WAS MEASURED AT A DRAIN BIAS OF 3.0

Device	V_{th} (Volt.)	$g_{m,max}$ (mS/mm)	$I_{DS,max}$ (mA/mm)	Linear g_m range (mA/mm)
$Ga_{0.5}In_{0.5}P$	-2.7	180	680	380
$(Al_{0.3}Ga_{0.7})_{0.5}In_{0.5}P$	-3.0	210	800	500
$Al_{0.5}In_{0.5}P$	-3.7	175	827	410

$(Al_{0.3}Ga_{0.7})_{0.5}In_{0.5}P/In_{0.15}Ga_{0.85}As$ DCFETs are shown in Fig. 4(a). Compared with the $Ga_{0.5}In_{0.5}P$ and $Al_{0.5}In_{0.5}P$ materials, where the barrier heights are around 0.85 eV and 0.93 eV, its high Schottky barrier height of 1.00 eV results in reducing gate leakage current even at a gate bias of 1.0 V, and a complete pinched-off drain current was observed at a drain bias of 6.0 V. Fig.4(b) shows the device I_{DS} versus V_{GS} transfer characteristics biased at $V_{DS} = 3.0$ V. A wide and uniform g_m distribution of $(Al_{0.3}Ga_{0.7})_{0.5}In_{0.5}P$ DCFETs, as compared with HEMTs, was observed. The threshold voltage (V_{th}) of -3.0 V was determined from the intercept

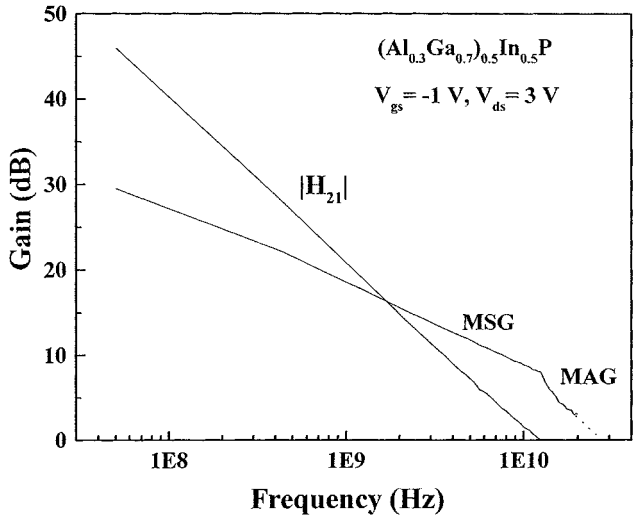

Fig. 5. Microwave characteristics of $(Al_{0.3}Ga_{0.7})_{0.5}In_{0.5}P/In_{0.15}Ga_{0.85}As$ DCFETs with a gate length of 1.0 μm and a width of 50 μm.

point by the extrapolation of $I_{DS}^{1/2}$ versus V_{GS} curves. The $Al_{0.5}In_{0.5}P/In_{0.15}Ga_{0.85}As$ device exhibited a larger $I_{DS,max}$ and V_{th} (827 mA/mm, -3.7 V) than those for $x = 0$ (680 mA/mm, -2.7 V) and $x = 0.3$ (800 mA/mm, -3.0 V), due to its highest sheet charge density (1.62×10^{13} cm^{-2}). The maximum transconductances biased at $V_{DS} = 3.0$ V for $x = 0, x = 0.3$, and $x = 1$ were 180 mS/mm, 210 mS/mm and 175 mS/mm, respectively. If we compared these three devices, by defining a flat gain region of its 10% reduction from the peak g_m value, the linear g_m regions versus the gate bias were 2.15 V for $x = 0$, 2.42 V for $x = 0.3$, and 2.23 V for $x = 1$, corresponding to current ranges of 380 mA/mm, 500 mA/mm, and 410 mA/mm, respectively. Table III summarizes these dc parameters for 1.0 μm-long gate $(Al_xGa_{1-x})_{0.5}In_{0.5}P$ $(x = 0, 0.3, 1.0)$ DCFETs. Based on the dc performance evaluation, $(Al_{0.3}Ga_{0.7})_{0.5}In_{0.5}P$ DCFETs demonstrate a larger dc gain and a better device linearity, which is directly associated with the facts that the $(Al_{0.3}Ga_{0.7})_{0.5}In_{0.5}P$ layer achieves a larger Schottky barrier and a higher turn-on voltage [4].

An on-wafer microwave S-parameters evaluation for 1.0 μm-long gate DCFETs was carried out in a common-source configuration by an HP 8510 network analyzer in conjunction with Cascade direct probes. As shown in Fig. 5, the current gain cut-off frequency (f_T) and the maximum oscillation frequency (f_{max}) of $(Al_{0.3}Ga_{0.7})_{0.5}In_{0.5}P/In_{0.15}Ga_{0.85}As$ DCFETs were 13.8 GHz and 29.2 GHz, respectively, at $V_{GS} = -1.0$ V and $V_{DS} = 3.0$ V. As to the $Ga_{0.5}In_{0.5}P$ $(x = 0)$ and $Al_{0.5}In_{0.5}P$ $(x = 1)$ devices, the f_T's were 12.3 GHz and 12.2 GHz, and the f_{max}'s were 26.5 GHz and 28.5 GHz, which are listed in Table IV.

The microwave power characteristics were evaluated by a load-pull system with automatic tuners, which provides conjugate matched input and load impedances simultaneously for the maximum output power. Microwave load-pull power performance was conducted at 1.9 GHz under a drain bias of 3.0 V. The gate bias was chosen at a class AB operation with an output current of 10% $I_{DS\text{-}max}$ for each device, which was compromised by considering the device power-added efficiency (*PAE*) and output power (P_{out}). Fig. 6 shows the P_{out}, *Gain*, and *PAE* as a function of the input power (P_{in}) for 1.0×50 μm^2 gate-dimension devices. The $(Al_{0.3}Ga_{0.7})_{0.5}In_{0.5}P$ DCFETs exhibited a saturated P_{out} of 10.4 dBm (219 mW/mm), an associated gain of 14.6 dB, and a PAE of 40.2%. As shown in Fig. 6, it is obvious that the $(Al_{0.3}Ga_{0.7})_{0.5}In_{0.5}P$ DCFETs demonstrated a better power performance than those of $Ga_{0.5}In_{0.5}P$ and $Al_{0.5}In_{0.5}P$ devices, which are all listed in Table IV. If we

TABLE IV
SUMMARY OF RF AND MICROWAVE POWER CHARACTERISTICS FOR $(Al_xGa_{1-x})_{0.5}In_{0.5}P/In_{0.15}Ga_{0.85}As$ $(x = 0, 0.3, 1.0)$ DCFETs

Device	RF Performance		Microwave Power Performance at 1.9 GHz		
	f_T (GHz)	f_{max} (GHz)	Pout (dBm)	Gain (dB)	PAE (%)
$Ga_{0.5}In_{0.5}P$	12.3	26.5	8.87	12.2	24.5%
$(Al_{0.3}Ga_{0.7})_{0.5}In_{0.5}P$	13.8	29.2	10.4	14.6	40.2%
$Al_{0.5}In_{0.5}P$	12.2	28.5	10.2	13.1	39 %

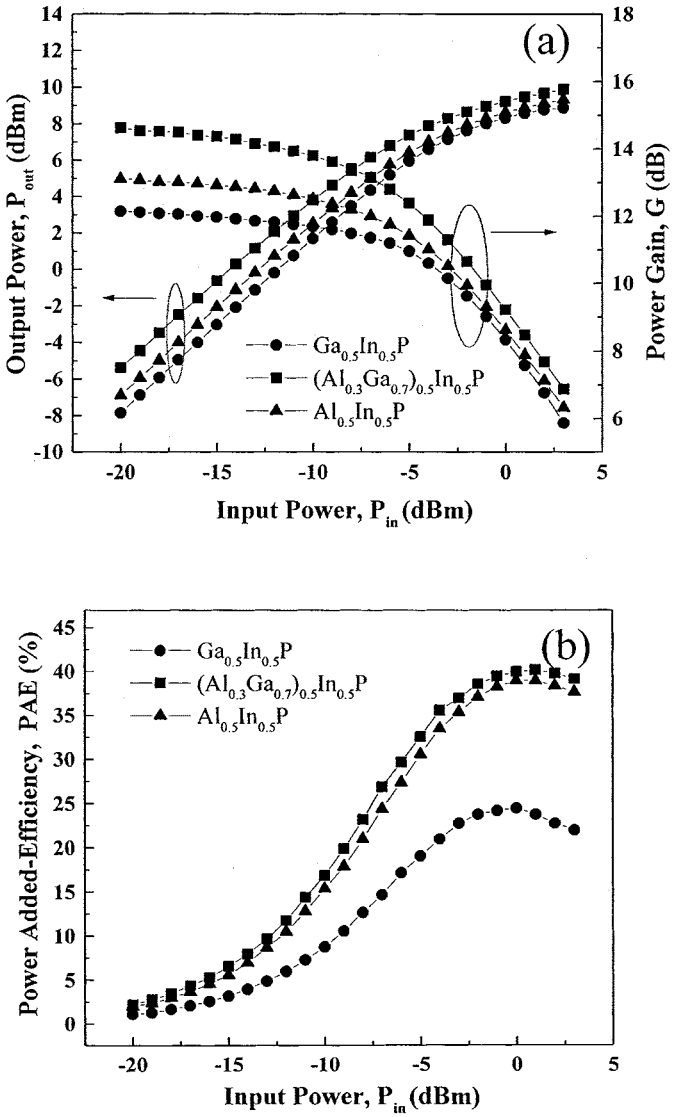

Fig. 6. Power performance of $(Al_xGa_{1-x})_{0.5}In_{0.5}P/In_{0.15}Ga_{0.85}As$ DCFETs with a gate length of 1.0 μm at 1.9 GHz ($V_{DS} = 3.0$ V): (a) output power and power gain versus input power and (b) power added efficiency (*PAE*) versus input power.

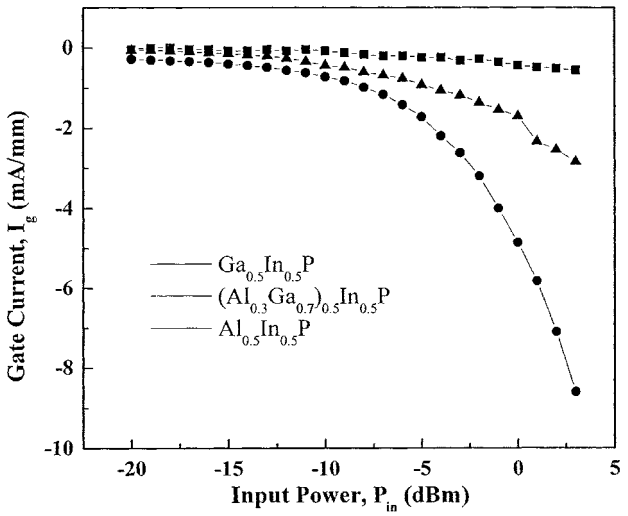

Fig. 7. Gate leakage current versus input power of $(Al_xGa_{1-x})_{0.5}In_{0.5}P/In_{0.15}Ga_{0.85}As$ $(x = 0, 0.3, 1.0)$ DCFETs for 1.0 μm $\times$ 50 μm devices.

compared their gate leakage currents versus input power at a 1.9 GHz operation, shown in Fig. 7, the $(Al_{0.3}Ga_{0.7})_{0.5}In_{0.5}P$ DCFETs performed the lowest gate leakage current up to P_{in} of 3 dBm, and all leakage currents were increased by increasing the input RF powers. This feature of the reduction in gate leakage is due to its superior quality of the Schottky performance in $(Al_{0.3}Ga_{0.7})_{0.5}In_{0.5}P$ layers, and is therefore beneficial to its device power performance.

VI. Conclusion

In summary, the quaternary $(Al_xGa_{1-x})_{0.5}In_{0.5}P$ $(0 \leq x \leq 1)$ compounds on GaAs substrates were grown and characterized. Based on the experimental results, we conclude that for the realization of DCFETs in terms of device characteristics, the best composition is aluminum content of $(Al_{0.3}Ga_{0.7})_{0.5}In_{0.5}P$, where $x = 0.3$. The dc peak extrinsic g_m of $(Al_{0.3}Ga_{0.7})_{0.5}In_{0.5}P/In_{0.15}Ga_{0.85}As$ DCFETs is 210 mS/mm, together with an f_T of 13.8 GHz and an $f_{\max}$ of 29.2 GHz. As for the power performance at 1.9 GHz, it demonstrates a 10.4 dBm (219 mW/mm) saturated output power, a 14.6 dB linear power gain and a 40.2% efficiency. These remarkable properties indeed reveal that the studied device structure has a good potentiality for high-power device applications.

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