Analysis of Gate Misalignment Effect on the Threshold Voltage of Double-Gate (DG) Ultrathin Fully-Depleted (FD) Silicon-On-Insulator (SOI) NMOS Devices Using a Compact Model Considering Fringing Electric Field Effect

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Abstract

This paper reports an analysis of gate misalignment effect on the threshold voltage of double-gate ultrathin fully-depleted (FD) silicon-on-insulator (SOI) NMOS devices using a compact model considering fringing electric field effect. Using the conformal mapping transformation approach, a closed-form compact model considering the fringing electric field effect above the non-gate overlap region has been derived to provide an accurate prediction of the threshold voltage behavior as verified by the 2D simulation results.

1. Introduction

SOI technology has been regarded as another mainstream technology for CMOS VLSI[1]. DG SOI technology has demonstrated its advantages for realizing sub-100nm CMOS devices[2]-[4]. For DG SOI CMOS devices, the gate misalignment effects have a deep impact on device performance[5]. Fig. 1 shows the 2D electric field contours in a DG SOI NMOS device with a gate oxide thickness of 70Å, a thin-film of 600Å doped with a p-type density of $4 \times 10^{17}\text{cm}^{-3}$, and a gate misalignment of 0.04μm, biased at $V_{GS} = V_{th}$, and V_{DS} = 50mV. As shown in the figure, the fringing electric field from the right edge of the bottom gate to the thin-film of the non-gate overlap region is substantial, which could cause non-negligible influence in device performance. In this paper, an analysis of gate misalignment effect on the threshold voltage of DG ultrathin FD SOI NMOS devices using a compact model considering fringing electric field effect is reported. It will be shown that using the conformal mapping transformation approach, this closed-form compact model considering the fringing electric field effect in the non-gate overlap region could provide an accurate prediction of the threshold voltage behavior as verified by the 2D simulation results. In the following sections, derivation of the analytical model is described, followed by model verification and discussion.

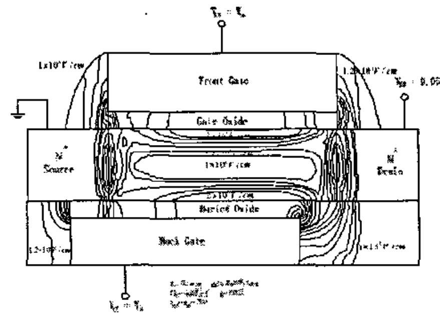

Figure 1: 2D electric field contours in a DG SOI NMOS device with n^+ polysilicon top and bottom gates, a gate oxide of 70Å, a thin-film of 600Å doped with a p-type density of $4 \times 10^{17}\text{cm}^{-3}$, and a gate misalignment of 0.04μm, biased at $V_{GS} = V_{th}$ and V_{DS} = 50mV.

2. Analytical Model

Fig. 2(a) shows the cross section of the DG SOI NMOS device with a gate misalignment. 2D Poisson's equation $\frac{\partial^2\Psi(x,y)}{\partial x^2} + \frac{\partial^2\Psi(x,y)}{\partial y^2} = \frac{qN_A}{\epsilon_{si}}$ has been used for solving the electrostatic potential in the thin-film region, which is divided into (I) gate overlap and (II) non-gate overlap regions. In the gate overlap region, a conventional approach [6] has been used to solve the 2D Poisson's equation. In the non-gate overlap region, its electrostatic potential could be approximated as: $\Psi_2(x,y) = P_{02}(y) + P_{12}(y)x + P_{22}(y)x^2$. From Gauss Law at bottom and top oxide/thin-film interfaces, the boundary condi-

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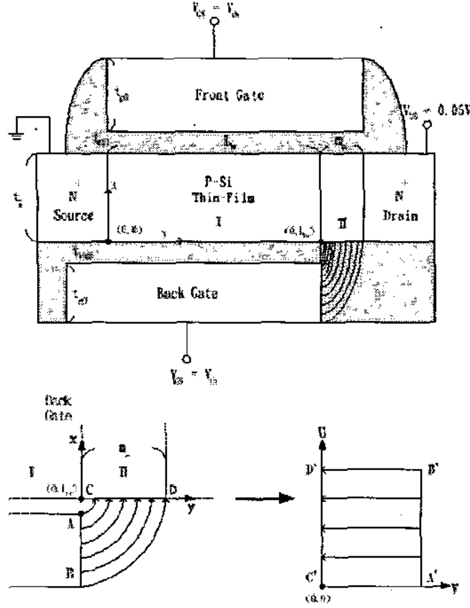

Figure 2: (a) Cross section of the DG SOI NMOS device with a gate misalignment and (b) the boundary of the sidewall oxide region next to the right edge of the bottom gate before and after conformal mapping for model derivation.

tions are: $-\frac{\partial\Psi_2(x,y)}{\partial x}|_{x=0} = \frac{\epsilon_{ox}}{\epsilon_{si}t(y)}[V_g + \Phi_{f2(poly)} - \Psi_{b2}(y)]$, $-\frac{\partial\Psi_2(x,y)}{\partial x}|_{x=ti} = \frac{C_{ox1}}{\epsilon_{si}}[\Psi_{s2}(y) - V_g - \Phi_{f1(poly)}]$. Using a decoupled approach ($\frac{\partial^2\Psi_2(y)}{\partial y^2} \cong \frac{1}{\kappa_s}\frac{\partial^2\Psi_{b2}(y)}{\partial y^2}$), one could obtain a differential equation in terms of the electrostatic potential at the bottom interface (Ψ_{b2}) as: $\frac{\partial^2\Psi_{b2}(y)}{\partial y^2} = \kappa_s(\frac{qN_A}{\epsilon_{si}} - 2(\frac{-[1+\frac{t_{ox1}}{t(y)}+\frac{t_{ox}}{t(y)C_s}]\Psi_{b2}(y)+[1+\frac{t_{ox1}}{t(y)}+\frac{t_{ox}}{t(y)C_s}]V_g+[\frac{t_{ox1}}{t(y)}+\frac{t_{ox}}{t(y)C_s}]\Phi_{f2}+\Phi_{f1}}{t_i^2(1+2\frac{C_s}{C_{ox1}})})$

Due to the fringing electric field from the right edge of the bottom gate via the oxide to the thin-film interface, the above equation is difficult to calculate. In order to simplify the analysis, a conformal mapping transformation technique [7] has been used to transform the original $x\vec{X} + y\vec{Y}$ space in terms of the $\vec{X}$ and $\vec{Y}$ as shown in Fig. 2 to the $u\vec{U} + v\vec{V}$ space in terms of $\vec{U}$ and $\vec{V}$ axes based on the following transfer function: $(y - L_m)\vec{Y} + nx\vec{X} = k\sinh(u\vec{U} + v\vec{V})$, where $L_m = L_c - m_a$, $n = \frac{m_a}{t_{ox2}\sinh[\cosh^{-1}(\frac{t_{ox2}+t_{g2}}{t_{ox2}})]}$, and $k = \frac{m_a}{\sinh[\cosh^{-1}(\frac{t_{ox2}+t_{g2}}{t_{ox2}})]}$. Based on the above formula, ABCD in the $x\vec{X} + y\vec{Y}$ coordinates is transformed into A'B'C'D' in the $u\vec{U} + v\vec{V}$ coordinates. As a result, the arc-shaped electric field contour in the oxide next to the right edge of the bottom gate in the $x\vec{X} + y\vec{Y}$ has become straight-line-shaped in the $u\vec{U} + v\vec{V}$ coordinates. Based on the transformation, the distance between the bottom gate electrode and the bottom thin-film/oxide interface t(y), which is a not a fixed value, has been transformed into $\frac{m\pi}{2}$, which is the distance between points A' and C' in the new coordinates under the condition $sinh(\frac{m\pi}{2}) = 1$. Therefore, a differential equation in terms of back surface potential Ψ_{b2} in the $u\vec{U} + v\vec{V}$ coordinates has been obtained. After solving it, the electrostatic potentials at bottom and top interfaces (Ψ_{b2}, Ψ_{s2}) are

$$\Psi_{b2}(y) = g_1\exp[\frac{\gamma}{k}(y - L_m)] + g_2\exp[-\frac{\gamma}{k}(y - L_m)] + \frac{B_1}{B_0}$$
$$\Psi_{s2}(y) = \frac{\sigma_2[\frac{2C_s}{C_{ox1}} + \frac{t_{ox1}}{t(y)}]\Psi_{b2}(y) + [1 - \frac{t_{ox1}}{t(y)}]V_g - [\frac{t_{ox1}}{t(y)}]\Phi_{f2} + \Phi_{f1}}{1 + \frac{2C_s}{C_{ox1}}},$$

where coefficients could be determined from boundary conditions. The threshold voltage is defined as the gate voltage when the sum of the electron densities at the locations with the minimum front and back surface potentials reaches the doping density of the thin-film:

$$N_A = n_i\exp(\frac{\Psi_{s(min)}}{V_T}) + n_i\exp(\frac{\Psi_{b(min)}}{V_T}).$$

Using the above condition with another condition from the solution of the minimum front and back surface potentials:

$$V_{th} = \frac{[C_{ox1} + 2C_s]\Psi_{s(min)} - [C_{ox2} + 2C_s]\Psi_{b(min)} + C_{ox2}\Phi_{f2} - C_{ox1}\Phi_{f1}}{C_{ox1} - C_{ox2}}. \quad (1)$$

the threshold voltage of the DG SOI NMOS device with a gate misalignment has been obtained.

3. Model Verification

In order to assess the effectiveness of the analytical model for the gate misalignment effect of the DG SOI NMOS devices, the model results have been compared with the 2D simulation results. Fig. 3 shows (a) back and (b) front surface potential distributions of the DG SOI NMOS device with a channel length of $0.2\mu m$, n^+ polysilicon top and bottom gates, a gate oxide of 70Å, a thin-film of 600Å doped with a p-type density of $4 \times 10^{17}cm^{-3}$, and various gate misalignments biased at $V_{GS} = V_{th}$ and $V_{DS} = 50mV$, based on the analytical model with and without considering fringing electric field effects, and 2D simulation results. As shown in the Fig. 3(a), when the gate misalignment increases, the back surface potential is lowered in the non-gate overlap region. Considering the fringing electric field effect due to gate misalignment, the dip in the back surface potential becomes smaller as compared to the case without considering it. In addition, when the gate misalignment becomes larger, the fringing electric field effect becomes more

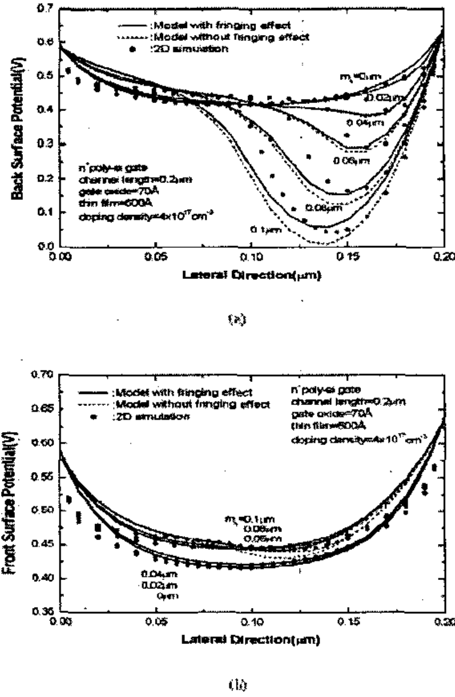

Figure 3: (a) Back and (b) front surface potential distributions of the DG SOI NMOS device with a channel length of $0.2\mu m$, n^+ polysilicon top and bottom gates, a gate oxide of 70Å, a thin-film of 600Å doped with a p-type density of $4 \times 10^{17} cm^{-3}$, and various gate misalignments biased at $V_{GS} = V_{th}$ and $V_{DS} = 50mV$, based on the analytical model with and without considering fringing electric field effects, and 2D simulation results.

important. As shown in Fig. 3(b), when the gate misalignment becomes larger, the fringing electric field effect on the front surface potential becomes more noticeable. In addition, a larger gate misalignment leads to a lower minimum front surface potential, which is also due to the fringing electric field effects. As shown in Figs.3(a)&(b), the analytical model considering the fringing electric field affect could predict front and back surface potential distributions consistently as verified by the 2D simulation results.

Fig. 4 shows the threshold voltage versus the gate misalignment of the DG SOI NMOS device with a channel length of $0.2\mu m$, n^+ polysilicon top and bottom gates, a gate oxide of 70Å, and a thin-film of 500Å and 600Å doped with a p-type density of $4 \times 10^{17} cm^{-3}$, based on the analytical model with and without considering fringing electric field effects and 2D simulation results. As shown in the figure, for both cases with a thin-film of 500Å an 600Å, the

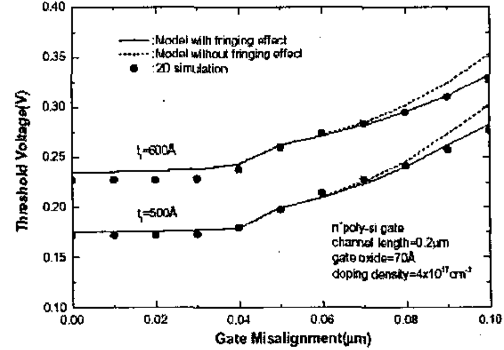

Figure 4: Threshold voltage versus gate misalignment of the DG SOI NMOS device with a channel length of $0.2\mu m$, n^+ polysilicon top and bottom gates, a gate oxide of 70Å, and a thin-film of 500Å and 600Å doped with a p-type density of $4 \times 10^{17} cm^{-3}$, based on the analytical model with and without considering fringing electric field effects and 2D simulation results.

fringing electric field effect coming from gate misalignment is important in determining the threshold voltage. Without considering the fringing electric field effect, the threshold voltage is over-estimated, which is more noticeable when the gate misalignment becomes larger. At a gate misalignment of $0.1\mu m$, the fringing electric field effect causes a reduction in threshold voltage about 0.022V (6%) for the thin-film of 600Å and 0.028V (7%) for 500Å. As shown the in the figure, as verified by the 2D simulation result, the analytical model considering the fringing electric field effect could provide an accurate prediction of the threshold voltage.

4. Discussion

Fig. 5 shows (a) minimum front and back surface potentials and (b) their locations versus gate misalignment of the DG SOI NMOS device with a channel length of $0.2\mu m$, n^+ polysilicon top and bottom gates, a gate oxide of 70Å, and a thin-film of 600Å doped with a p-type density of $4 \times 10^{17} cm^{-3}$, biased at $V_{GS} = V_{th}$ and $V_{DS} = 50mV$. As shown in Fig. 5(a)&(b), when the gate misalignment is smaller than $0.03\mu m$, the minimum front and back surface potentials are about equal, located in the gate overlap region. When the gate misalignment increases, the location with the minimum back surface potential moves toward the drain direction. At the gate misalignment of $0.04\mu m$, it is located in the nongate overlap region. A further increase in the gate misalignment leads to the situation that the location with the minimum back surface potential moves toward the source direction mildly. A similar situation

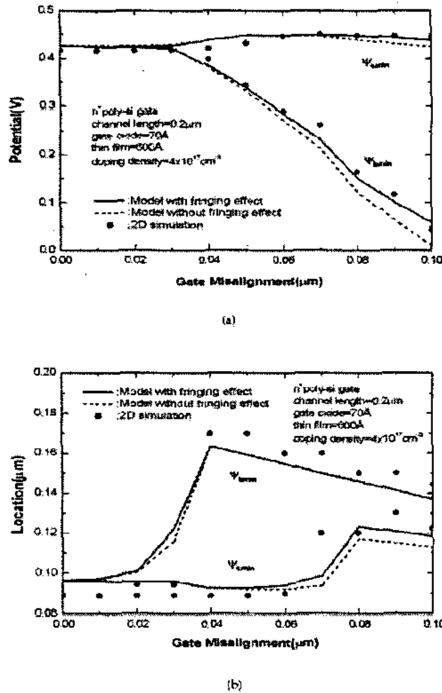

Figure 5: (a) Minimum front and back surface potentials and (b) their locations versus gate misalignment of the DG SOI NMOS device with a channel length of $0.2\mu m$, n^+ polysilicon top and bottom gates, a gate oxide of 70Å, and a thin-film of 600Å doped with a p-type density of $4 \times 10^{17} cm^{-3}$, biased at $V_{GS} = V_{th}$ and $V_{DS} = 50mV$.

exists for the front surface potential but its transition point is located at the gate misalignment of $0.08\mu m$. When the gate misalignment is greater than $0.08\mu m$, the location with the minimum front surface potential moves to the non-gate overlap region. As shown in the figure, as verified by the 2D simulation results, the analytical model considering the fringing electric field effect predicts the behavior closely.

5. Conclusion

In this paper, an analysis of gate misalignment effect on the threshold voltage of DG FD SOI NMOS devices using a compact model considering fringing electric field effect has been described. Using the conformal mapping transformation approach, a closed-form compact model considering the fringing electric field effect above the non-gate overlap region has been derived to provide an accurate prediction of the threshold voltage behavior as verified by the 2D simulation results.

6. Acknowledgments

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