A MONOLITHIC K-BAND MMIC RECEIVER

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This paper presents the designs and measurement results of a K-band monolithic microwave integrated circuit (MMIC) receiver, including a low noise amplifier and a singly balanced mixer. The MMIC chips are fabricated with a 0.15-μm gate-length pseudomorphic (PM) GaAs-based HEMT MMIC technology, carried out by commercially available foundry.

1 Introduction

As the wireless communications become more and more popular, the application frequency is moving toward higher frequency range such as K-band (18-27 GHz) or above due to the crowdness of low frequency spectrum. This paper presents the development of a 21-26 GHz integrated receiver using 0.15-μm GaAs pHEMT technology and its individual components, including a monolithic low-noise amplifier and a monolithic singly balanced mixer. All of the monolithic IC chips are fabricated on the same wafer and exhibit good measured RF performance with yield. The two-stage LNA demonstrated a measured small signal gain of 22 dB at 23 GHz; the mixer has a 10 dB conversion loss at also 23 GHz.

2 HEMT Device Characteristic and MMIC Technology

The monolithic LNA, mixer and receiver chips were fabricated on 100-μm thick substrates. The GaAs-based pseudormorphic HEMT MMIC process foundry service is provided by TRW. The device is a 0.15-μm gate-length low noise PHEMT with a maximum unit current gain frequency (f_T) of 105 GHz. The passive components include TFR resistor, MIM capacitor, and via hole through 100-μm GaAs substrate. The entire chip is also protected by silicon-nitride passivation for reliability concern.

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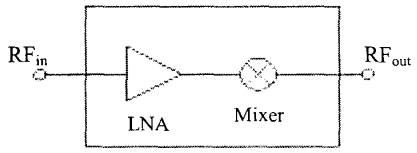
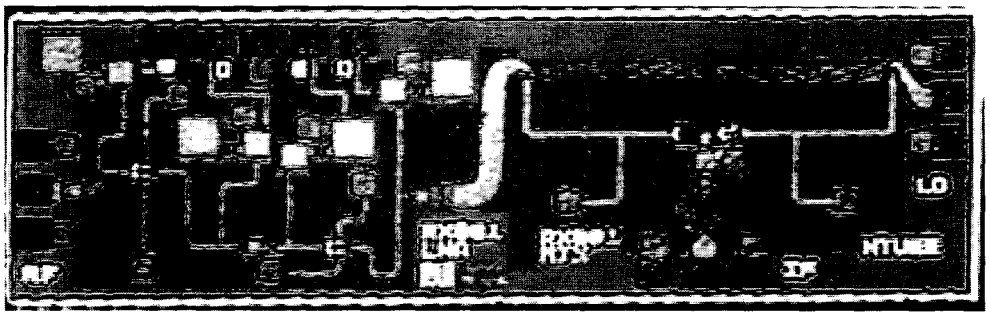
3 Receiver Design

The receiver is realized by cascading the LNA with the mixer onto a single monolithic chip. A block diagram of the receiver is shown in Fig. 1(a). Since both designs are matched to 50 Ω, a short section of 50Ω transmission line is used to join the two circuits. Though the testing is still in progress, we could make an estimate of this receiver design. It is estimated to have about 10 dB conversion gain at 23 GHz with LO signal pumped at 10-dBm power. Fig. 1(b) shows the chip photo of the receiver. The chip size is 3 mm x 1 mm.



(a)



(b)

Fig. 1(a) Block diagram of the monolithic K-band receiver.

(b) Photograph of the receiver. The chip size is 3 mm x 1 mm.

4 Low Noise Amplifier Design

The two-stage MMIC LNA utilizes four-finger 120-μm HEMT devices. The first stage of the two-stage LNA is matched for minimum NF, and the second stage of the two-stage LNA is matched for gain [1], [2]. The matching networks are all realized with the inductive T-transformer using high impedance microstrip lines and series capacitors. Source feedback transmission lines are utilized in the input stages for stability consideration without degrading the noise performance. On the bias networks, shunt RC networks are designed for low frequency stability. The chip photo is shown in Fig. 2. The chip size is 3 mm x 1 mm. Fig. 3 shows the measured small-signal gain and return loss by on-wafer probing. The two-stage amplifier has small signal gain of 22 dB at 23 GHz. It is biased at 2-V drain voltage with 15-mA drain current for each stage.

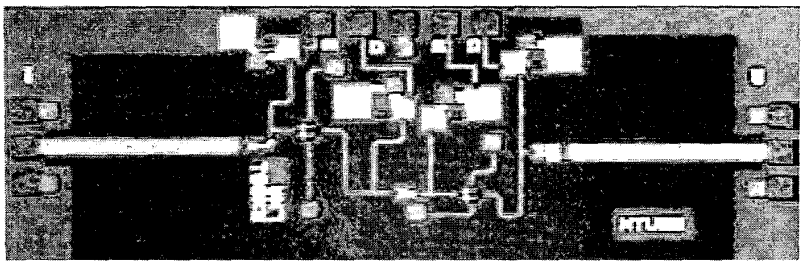


Fig. 2 The chip photo of the 2-stage low noise amplifier. The chip size is 3 mm x 1 mm.

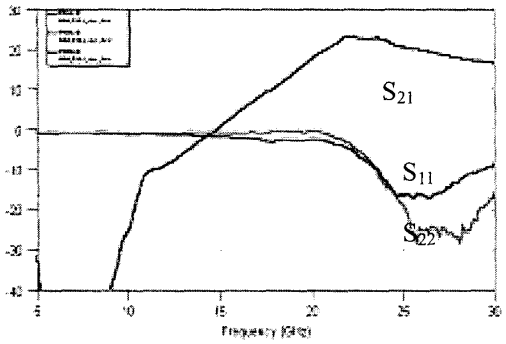


Fig. 3 The measured performance of the 2-stage LNA

5 Singly balanced mixer

The singly balanced mixer utilizes diodes as the mixing structure. The diodes are zero biased, since they have very good non-linearity at this condition. The simulation results are derived from harmonic balanced simulation using commercial software Libra^{TM} [3]. Due to the stability and the efficiency concern, the Lange coupler structure is used as the hybrid for the mixer design. As for the IF filter, it is realized by the lumped elements and it is centered at 1 GHz. The chip photo is shown in Fig. 4. The chip size is 3 mm x 1 mm.

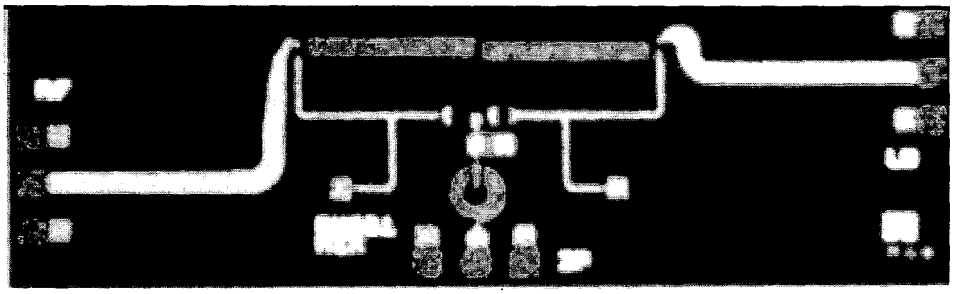
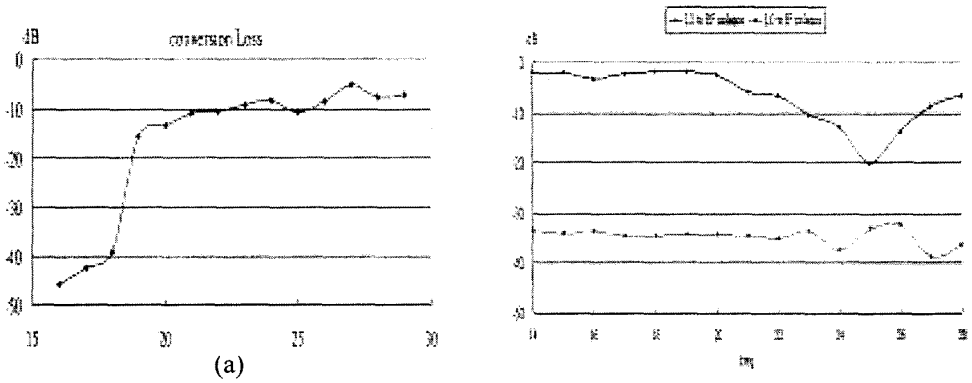


Fig. 4 The chip photo of the single balanced mixer. The chip size is 3 mm x 1 mm.

Fig. 5 shows the measured performance by on-wafer probing. The mixer has conversion loss of –10 dB at 23 GHz with LO drives at 10 dBm. The LO-to-RF isolation is better than –10 dB, and the LO-to-IF isolation is better than –30 dB.



(a)

Fig. 5 The measured performance of the single balanced mixer.

(a) The measured conversion loss while the LO is pumped at 10 dBm.

(b) The measured isolation of LO-to-RF and LO-to-IF.

6 Summary

A 21-26 GHz integrated receiver using 0.15-μm GaAs pHEMT technology and its individual components, including a monolithic low-noise amplifier and a monolithic singly balanced mixer, are presented in this paper. All of the monolithic IC chips are fabricated on the same wafer and exhibit good measured RF performance with yield. The two-stage LNA demonstrated a measured small signal gain of 22 dB at 23 GHz; the mixer has a 10 dB conversion loss at also 23 GHz.

Acknowledgements

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References

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[3] Libra user's manual. Hewlett-Packard.