A Resonant Flip-Chip Design with Controllable Transition Band

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Abstract—This paper proposes a new flip-chip structure which uses resonanting dual bumps to achieve best transition. By simply changing the distance between the two bumps, we can control the band of minimum reflection in the desired frequency band. The bandwidth over which the return loss is smaller than −20dB is 20~30%. The corresponding insertion loss in this band is less than -1.5dB. All results presented below are simulated with the FDTD method combined with PML.

I. Introduction

The coplanar waveguide has found increasing application in MMIC at millimeter wave frequencies. Emerging commercial markets request a greater demand in low cost, reliable property, and good performance in packaging structure. Comparison with the wire bond has encouraged the use of flip-chip for the chip connection. It has been shown that the flip-chip can yield better performance and lower surface wave loss [1],[2]. For single chip transition, lower reflection has been achieved by increasing the width of via or reducing its length, and the conductor on the mother board below the chip should be avoided [3]. Some efforts were made to investigate the influences on the transition characteristics due to the via positions or cross sections, and the shape of the metal [4],[5].

Although the method proposed in [3]-[5] could enhance the performance of transition, no obvious rule for tuning these parameters has been established to achieve an optimum performance. Based on the idea of resonance, this paper proposes new designs for the flip-chip transition.

II. Statement of Problem

The basic flip-chip structure under analysis is illustrated in Fig.1 where Fig.1(a) is a three-dimensional view, Fig.1(b) is the side view, and Fig.1(c) is the top view. The transmission lines in both layers, e.g., chip and board layers, are coplanar waveguides (CPW). They are connected by vias of width L and length H_2. For simplicity, the vias are assumed to be of square shape. The substrates of the upper and lower layers are the same, of dielectric constant $\varepsilon_{r1}=\varepsilon_{r3}$, while the transition happens in free space, i.e., $\varepsilon_{r2}=1$. It is worthy mentioning that the flip-chip connection requires no via hole, no wafer thinning process, and no backside processing of the wafer. In the simulation, the metals are assumed perfect conductors (PEC) and of negligible thickness. To discuss the circuit performance of the transition, the numerical method of FDTD combined with PML is applied here to extract the scattering parameters, and the results are shown in the following section.

III. Numerical Results

A) Conventional Design

Transition property of flip-chip interconnects has been investigated in the literature, e.g., the survey paper [6]. The configuration is shown in Fig.1. The solid curve in Fig.2 shows the calculated return loss (RL) versus frequency by using FDTD. The calculated results with solid line are in excellent
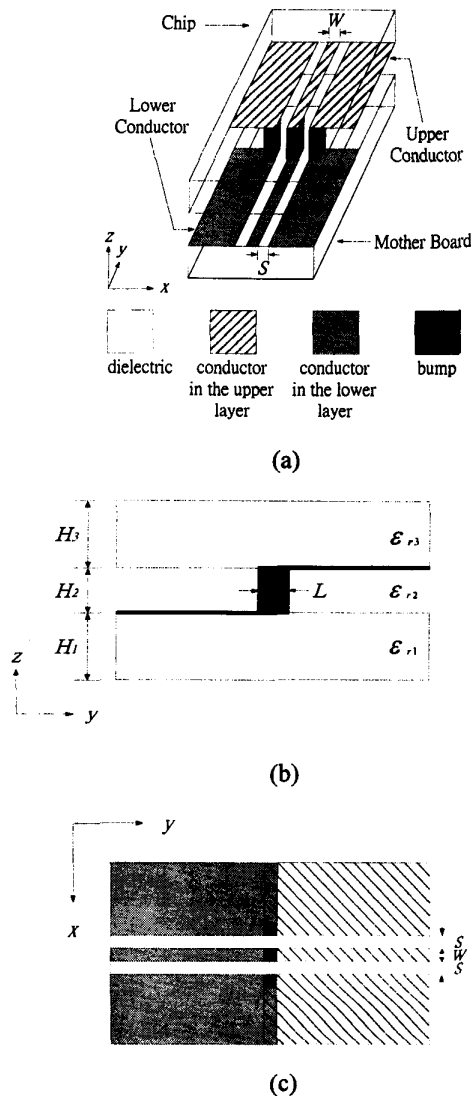
(a)

(b)

(c)

Fig.1 The configuration of traditional flip-chip transition. (a) three-dimensional view (b) side view and (c) top view. $H_1=H_3=0.36mm$, $H_2=0.12mm$, $W=S=L=0.12mm$, $\varepsilon_{r1}=12.9$, $\varepsilon_{r2}=1$, $\varepsilon_{r3}=12.9$.

agreement with those reprinted from [6]. As shown in Fig.2, it can be seen the RL becomes larger as the frequency increases. The traditional transition design suffers from larger reflection in the high frequency range.

B) Staggered Design
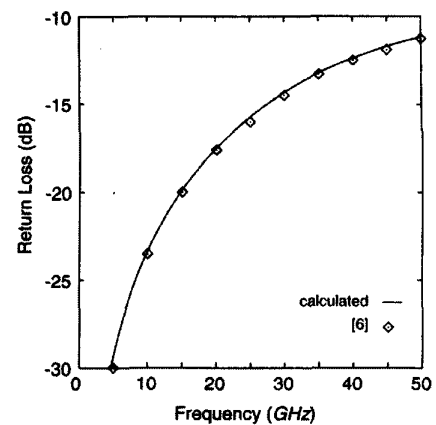
A staggered structure of flip-chip transition

Fig.2 Frequency response of return loss in the conventional flip-chip design.

is proposed to overcome the high reflection in the high frequency range [5]. Fig.3(a) displays the top view of the staggered structure, where other parameters are the same as Fig.1. Fig.3(b) shows the calculated RL versus frequency with staggered length L_{stg} as a parameter. The results with solid and dashed lines are calculated by the present analysis, while the dots are reprinted from [5] and included for comparison. Although the results calculated by the two methods show noticeable discrepancy, the staggered design can improve the transition property at high frequencies. For the present case, it seems that $L_{stg}=0.24mm$ can yield the best transition in 60-70 *GHz* range. However, it is hard to obtain a concise rule for the choice of the best staggered length at an arbitrary desired frequency band.

C) Single Resonance Design

A new design of flip-chip transition, which adopts the idea of resonance, is presented in this paper. The top view of the structure is shown in Fig. 4(a). One salient feature distinguished from the staggered design is the presence of two via connections along the signal line. The scattering from the two vias will interfere with each other and optimum transition may be achieved when the two vias are in suitable resonant separation.
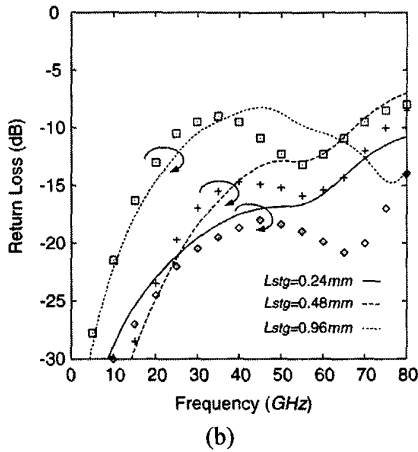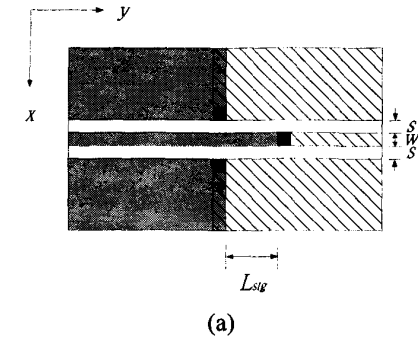
Fig.4(b) shows the frequency response of

(a)

Frequency (GHz)

(b)

Fig.3 The staggered flip-chip transition design. (a) top view (b) return loss versus frequency with staggered length L_{stg} as a parameter.

(a)

Frequency (GHz)

(b)

Fig.4 The single resonance flip-chip transition design. (a) top view (b) return loss versus frequency with L_{stg} as a parameter.

the return loss with different lengths of L_{stg} while all other parameters are the same as Fig.1. A good pass band can be noticed in the figure with the center frequency (first notch) f_0 varying with the length L_{stg}. The relative bandwidth over which the return loss is smaller than –20dB, or the 20dB BW in brief, is about 20~30%.

Similar procedure can be employed to calculate the insertion loss versus frequency with the lengths L_{stg} considered in Fig.4(b). Although not shown in this paper, the insertion loss is less than –1.5dB in the 20dB pass band, and –0.8dB at f_0 no matter what length L_{stg} is. This can be compared with the insertion loss in staggered design with an optimum L_{stg} of 0.24mm, which is –2dB.
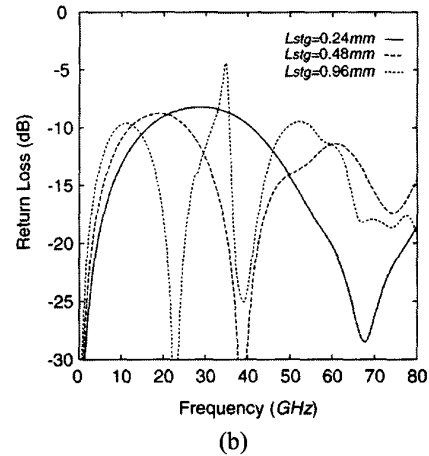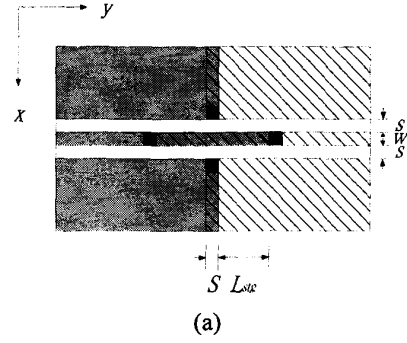
Fig.5 displays the half free space wavelength $\lambda_0/2=c*f_0/2$ versus the resonance length ($L_{stg}*2+S$). A nearly linear relationship between $\lambda_0/2$ and ($L_{stg}*2+S$) verifies that this occurrence of optimum transition is a resonance phenomenon. Given the desired operating frequency f_0, the figure can be employed to determine the via separation for the optimum transition design.

D) Dual Structure

Another design of flip-chip transition, which is dual to the single resonance design, is shown in Fig.6(a). Fig.6(b) shows the calculated RL versus frequency with staggered length L_{stg} as a parameter. The results also reveal a slight resonance phenomenon. A more detailed
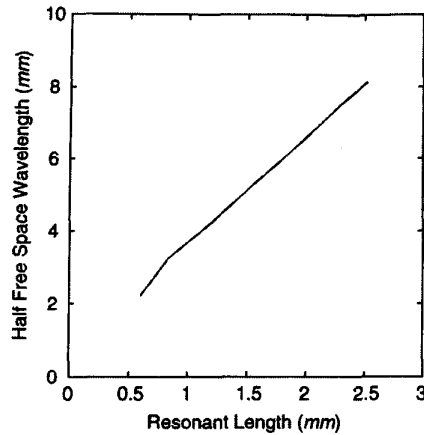
Fig.5 Half free space wavelength $\lambda_0/2=c^*f_0/2$ versus optimum via separation (L_{sig}^*2+S) for the single resonance flip-chip transition design.
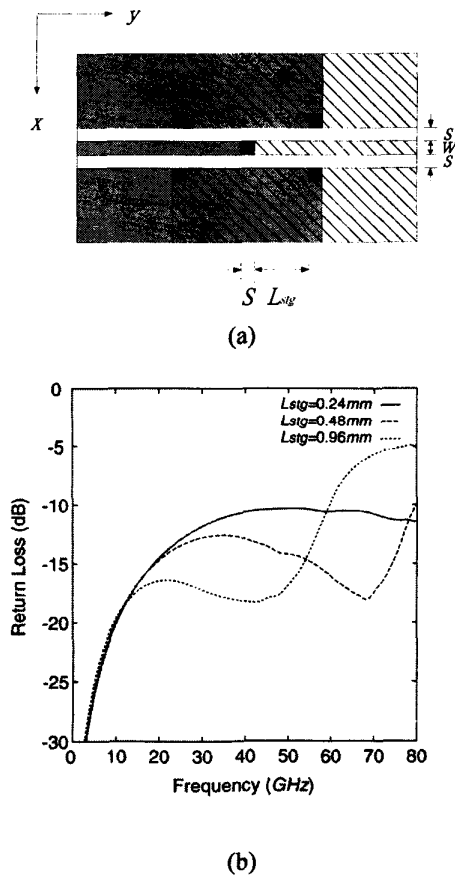

(a)

(b)

Fig.6 The dual structure flip-chip transition design (a) top view (b) return loss versus frequency with L_{sig} as a parameter.

analysis will be presented at the symposium.

IV. Conclusion

To sum up, a concise rule can be found for the design of the new flip-chip transition. We can control the frequency of pass band by adjusting the separation between the via connections. Simulation results demonstrate that the proposed structure can achieve a good transition design of 20~30% bandwidth over which the return loss is smaller than −20dB and the insertion loss is less than −1.5dB.

Reference:

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