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DC CHARACTERIZATION OF GaInP/GaAs TUNNELING EMITTER BIPOLAR TRANSISTORS

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Introduction

Xu and Shur[1] in 1986 proposed a novel device-the tunneling emitter bipolar transistor (TEBT). This structure has a thin tunneling barrier sandwiched between the n-type emitter and p-type base of a normal homo-junction bipolar transistor. The enhancement of emitter injection efficiency is achieved by taking advantage of a very large difference in the tunneling probabilities for electrons and holes in the barrier layer. Najjard[2] et. al. in 1987 fabricated successfully the first AlGaAs/GaAs TEBT. They observed the electron-to-hole preferential tunneling. Later, Berthold[3] et. al. in 1988 found non-equilibrium electron transport in the base of the AlAs/GaAs TEBT, which helps reduce the emitter size effect on current gain and improve the microwave performance as observed by Levi[4] et. al. in 1989. In AlGaAs/GaAs TEBT devices, the conduction band discontinuity ΔE_C is greater than valence band discontinuity ΔE_V. To fully utilize the preferential tunneling, a material system which has much larger ΔE_V than ΔE_C is necessary. It has been recently demostrated the $Ga_{.51}In_{.49}P$/GaAs system has the desired properties[5-11] ($\Delta E_C = 0.03$-0.22eV, $\Delta E_V = 0.24$-0.46eV). Therefore, we would like to study the dc performance of the GaInP/GaAs TEBT with different barrier thicknesses (50Å and 100Å) at different temperatures (77°K and 300°K).It was found that a very high current gain of 214 and a very small offset voltage of 40mV were achieved without the need of grading. The gain of the thick barrier device at 77°K was almost the same as that at 300°K while that of the thin barrier device increased when the temperature was lowered.

Experiment

$Ga_{.51}In_{.49}P$/GaAs TEBT structures were grown by gas source molecular beam epitaxy on semi-insulating (001) oriented GaAs substrates. The schematic band diagram of a typical TEBT used in our study under active bias is illustrated in Figure 1.

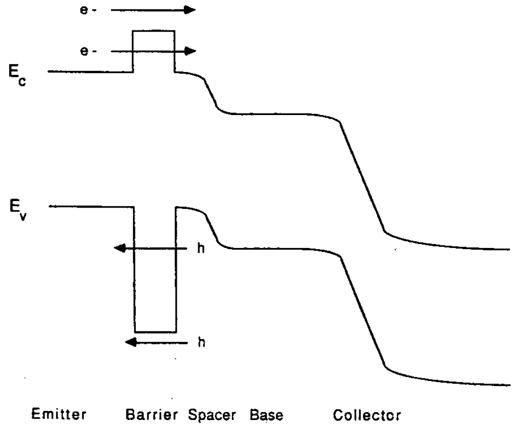

Fig. 1 The schematic band diagram of a TEBT.

Electrons in the n-type (4×10^{17} cm^{-3}, Si doped) GaAs emitter can tunnel through or be thermionically emitted over the GaInP barrier (50Å or 100Å) into a 1000Å-wide p-type (1×10^{19} cm^{-3}, Be doped) GaAs base. There is a 175Å undoped spacer between the barrier layer and the base. On the other hand, holes in the base have less probability to tunnel through or be thermionically emitted over the larger barrier. After traversing the base, electrons flow through the 0.5µm-thick n-type (5×10^{16} cm^{-3}, Si doped) collector region and are then collected in the 0.5µm thick n+ (2×10^{18} cm^{-3}, Si doped) sub-collector contact layer.

The wafers were fabricated into three mesa structures by standard photolithographic and wet chemical etching techniques. Emitter mesa was defined by selective wet etching. The etching solution was H_2O_2 adjusted with NH_4OH to have a 8.4 pH. This solution etched GaAs (~500Å/second, room temperature) but not GaInP. The GaInP layer was then removed selectively by HCl to expose the GaAs base for the AuZn evapration. Ohmic contacts to emitter and collector were fabricated by traditional NiGeAu evaporation and lift-off technique. To study the functional dependence of electron-to-hole preferential tunneling on GaInP barrier thickness, transistors with 50Å and 100Å tunneling barrier were fabricated. The current-voltage characteristics of the transistors were measured by a HP4145B at room temperatue and liquid nitrogen temperature.

Results and Discussions

The common-emitter current-voltage (I-V) characteristics of a typical TEBT structure (100Å) with emitter size of 2.3x10^{-5}cm^2 is shown in Figure 2.

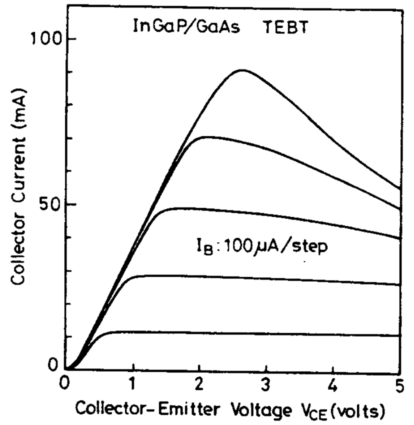

Fig. 2 The common-emitter current-voltage characteristics of a typical TEBT with 100Å GaInP barrier.

The 50Å barrier TEBT has similar I-V characteristics except that the current gain is lower. It can be seen that a very high current gain (214) and a very small offset voltage (40mV) were achieved as shown in Fig.2. These results were significant because it means that high current gain and small offset voltage can be maintained without any grading and suface passivation in GaInP/GaAs TEBT with similar base dopings and thicknesses. The current gain obtained was comparable to the results of graded emitter-base junction HBT[12] and was, to our knowledge, the best reported value to date in GaInP/GaAs HBT or TEBT. For the ease of probing, large emitter size (2.8x10^{-4}cm^2) devices were used for low temperature (77°K) measurement. Therefore, the later results we are going to address to are all referred to the large emitter size devices. The current gain (h_{fe}) versus collector current characteristics of large area devices with different barrier thicknesses at different temperatures are shown in Figure 3.

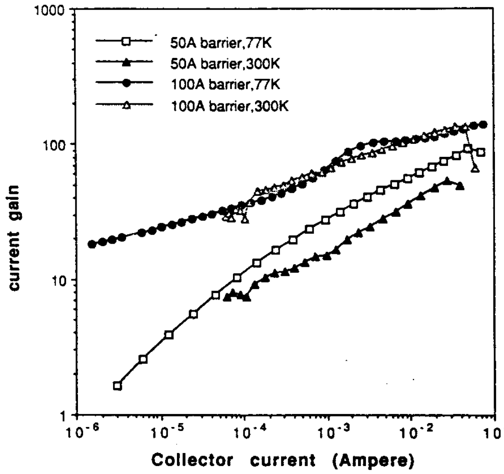

Fig. 3 The small-signal current gain versus collector current of TEBT's with different barrier thicknesses at different temperatures.

As can be seen clearly from Fig. 3, the gain of a homojuction bipolar transistor (typically lower than 10) can be improved by inserting a tunneling barrier between the emitter and base. We found that the structure with 100Å thick $In_{.49}Ga_{.51}P$ barrier, which we called device I, had higher small signal current gain (h_{fe}) than that with 50Å $In_{.49}Ga_{.51}P$ barrier, which we called device II, both at room temperature and liquid nitrogen temperature. The highest current gain achieved with this large emitter size for device I was 141, which was lower than that of the previous smaller device. This is reasonable because higher current density can be achieved without thermal heating effect in the smaller device. The fact that the current gain of device I was greater than that of device II at room temperature implies that h_{fe} increased with increasing barrier thickness. To explain this fact, let us examine the Gummel plots of devices I and II at room temperaure as shown in Figures 4(a) and 4(b).

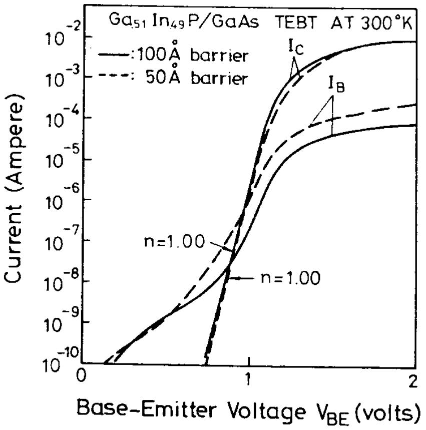

Fig. 4 The Gummel plot of TEBT's with different barrier thicknesses at room temperature.

It is clear that the collector currents (I_C) of devices I and II do not differ much. This indicates that the interfacial barrier has little effect on the electron transport. This behavior has also been observed by Najjard[3] and Lauterbach[13]. It follows that if electron tunneling through and/or thermionic emission over the barrierr takes place, it is not the limiting mode of electron transport from the emitter to the collector. However, the tunneling barrier has a much more pronounced effect on I_B than on I_C. The base current (or hole current) decreased when the barrier thickness increased from 50Å to 100Å. Such changes clearly indicate that holes are tunneling through the barrier and that tunneling is now the limiting mode of transport. The thicker barrier has smaller hole tunneling current and hence current gain is higher. Also, it is clear from Fig. 3 that the gain of device I at liquid nitrogen temperature was almost the same as that at room temperature while that of device II increased at liquid nitrogen temperature. These results were quite in contrast with the behavior of a conventional graded emitter-base junction HBT's, where the current gain decreases by a factor of 2 from 300°K to 77°K. The latter was explained by the decrease of transport factor at low temperature. However, the degradation of gain in device A was no more than 10% (in some current levels, the gain even increased) as shown in Fig. 3. The reduction of α_T from diffusion theory alone was not sufficeint to explain the experimental results. At low temperature, the thermionic emission current dominanted at room temperature was suppressed in device I. We believe that there were more energetic, non-equilibrium electrons in device I at low temperature than in conventional graded emitter HBT due to the existence of tunneling barrier between the emitter and base. The tunneling barrier could sustain a potential step before a large amount of electrons tunnels into the base as shown in Fig. 1. Tunneling injection can reduce the angular spread of a thermal distribution and the nonradiative recombination cross section, which results in the increase of carrier life time. The electrons tunneled from the barrierr can be further accelerated by the electric field in the spacer region. That is, there will be a lot of non-equilibrium, drift and hot electrons in the base instead of diffusive electrons. This point could be further supported by the results of the device B because one would expect that the current gain of the thin barrier device should increase at low temperature according to the above arguments, which was indeed the case as shown in Fig. 3. In a thin barrier, more electrons could tunnel through the barrier and accelerated by the field established between the emitter and base as illustrated in Fig. 1. In other words, there were more energetic, non-equilibrium electrons in such a device even at room temperature. As temperature was cooled down, the electrons had less probabilities to be scattered and there were more quasi-ballistic electrons. The lower the temperature, the shorter the base transit time for the those quasi-ballistic electrons to transport across the base, which results in higher current gain.

In summary, we have fabricated $\mathrm{In}_{.49}\mathrm{Ga}_{.51}$P/GaAs tunneling emitter bipolar transistors and measured the dc charateristics of them at different temperatures. A tunneling barrier of 100Å could effectively block most of the hole flow from base to emitter and a dc gain comparable to conventional graded emitter HBT was achieved at room temperature. A thinner barrier of 50Å sufferred from more hole tunneling and had lower dc gain at room temperature. However, the gain of thin barrier device increased at low temperature due to the shorter base transit time while the gain of thick barrier device was almost not changed due to the balance between the non-equilibrium and the diffusive electrons. The tunneling barrier was not only used for electron-to-hole preferential tunneling, but also a natural etching stop for easy processing.

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