Magamp application and limitation for multiwinding flyback converter

C.-C. Wen and C.-L. Chen

Abstract: A new magamp technique for multiwinding flyback converters is proposed. Ideal operating principle and analysis are presented. The practical circuit operation is limited due to the nonideal component characteristics. An analytical model for studying the phenomenon is provided. Based on the model, the mechanism of the boundary condition that causes the converter to be out of regulation is explored. Experimental verifications on a 20 W two-output flyback converter are conducted. They illustrate the effectiveness of the proposed magamp approach and the accuracy of the presented analytical model.

List of symbols

C_C	capacitance of RC clamp snubber
i_M	instantaneous current of L_M
I_{MA}	average current of L_M
I_{MPi}	peak current of L_M at the end of the ith time interval
i_P, i_1, i_2	instantaneous current of L_{KP}, L_{K1} and L_{K2}, respectively
I_{PA}, I_{1A}, I_{2A}	average currents of L_{KP}, L_{K1} and L_{K2}, respectively
I_{PPi}, I_{1Pi}, I_{2Pi}	peak currents of L_{KP}, L_{K1} and L_{K2}, respectively at the end of the ith time interval
I_0	initial current of L_M at the beginning of T_1 time interval
K_P, K_1, K_2	inductance factors where $K_p = L_M/L_{KP}$, $K_1 = L_M/L_{K1}$ and $K_2 = L_M/L_{K2} + N_2^2 L_{SR}$
L_M:	magnetising inductance of transformer
L_{SR}	saturated inductance of saturable reactor SR
N_1, N_2	turn ratios of transformer where $N_1 = n_p/n_1$ and $N_2 = n_p/n_2$
T	switching period
n_P, n_1, n_2	winding turns of transformer for primary winding, secondary winding 1 and secondary winding 2, respectively
T_i	ith time interval where i is 1–5
V_C	voltage across C_C
V_g	input DC voltage
R_C	resistance of RC clamp snubber
V_{Mi}	voltage across L_M during the ith time interval
V_1, V_2	output voltage 1 and 2 where $V_1 = N_1 \cdot V_{O1}$, $V_2 = N_2 \cdot V_{O2}$
L_{KP}, L_{K1}, L_{K2}	leakage inductances of transformer for primary winding, secondary winding 1 and secondary winding 2, respectively

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1 Introduction

Among the variety of switching-mode power converters, the flyback converter is a favourite choice: for design engineers in low power applications. The major merits of the flyback converter are: low part count, effective cost, quick dynamic response and simple multi-output structure. In industrial design of the multi-output flyback converter, a weighted voltage control scheme is often used to maintain regulation for all outputs. However, it does not reduce the total output error by adjusting the weighting factors. It only shifts the error to the other outputs [1]. Another disadvantage is that it is hard to arrange the transformer structure to make the output voltage be in the centre of regulation. Some previous papers [2, 3] have improved the cross-regulation of the multi-output flyback converter. However, in some applications, such as the onboard power supply of TFT-LCD monitor, stringent regulation is required to prevent the interference effect on the display panel. A postregulator is added to meet the regulation requirements. Among the different postregulation approaches, the magnetic amplifier (magamp) regulator has been popular for years. Compared with other postregulation schemes, the magamp postregulator is one of the most reliable, efficient and cost-effective solutions.

In recent decades, the magamp approach has mostly been applied in forward-type converters. Research on the use of the magamp for forward converters has also been widely reported, including: resetting methods, design guidelines and limitations [4–6]. There has been little research on the use of the magamp for flyback converters. A magamp technique for the flyback converter is presented in [7]. The main drawback is that the main output for the PWM feedback is restricted to the output with higher voltage, even with light rated output current. In this paper, a new magamp technique for flyback converters with multiple output windings is proposed [8]. The feedback loop and winding turn ratio can be chosen. This feature provides

more freedom to achieve optimum performance. For a practical design, the operating condition is limited due to the nonideal characteristics of the components.

2 Basic operation principle

Figure 1 shows the diagram of the multiwinding flyback converter with a magamp output. For simplicity, a two-output flyback converter is presented. As we know, in forward converter, the secondary outputs of the main transformer can be viewed as voltage sources and transfer energy to each output simultaneously. However, in the flyback converter, the operating principle is completely different. The flyback transformer can be viewed as a current source. The current time-sharing technique is applied. Figure 2 shows some waveforms in continuous current mode assuming ideal components. The basic operations are described as follows.

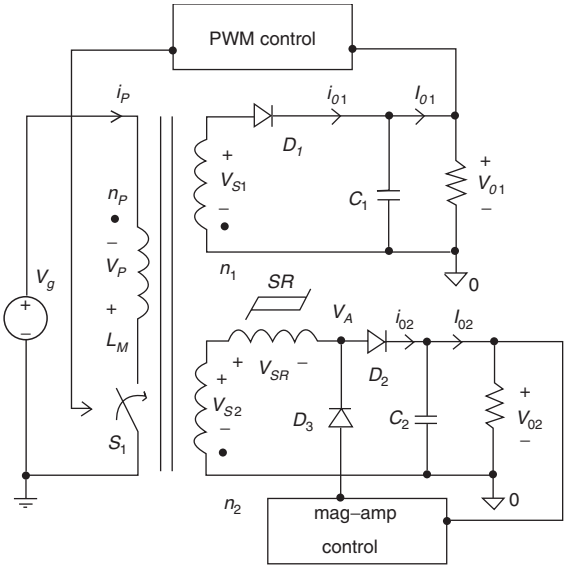

Fig. 1 *Diagram of multiwinding flyback converter with a magamp output*

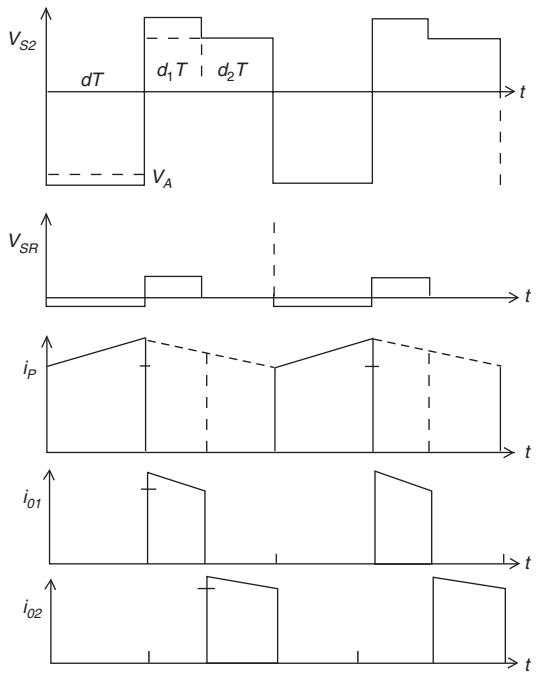

Fig. 2 *Some key waveforms in flyback converter with a magamp regulator*

In the time period dT, the main switch S_1 is on and the input voltage V_g charges the magnetising inductance L_M, where d is the turn-on duty cycle and T is the switching period. In the flyback converter, the main transformer is not only a common transformer but also an inductor to supply the energy to the outputs. At this period, the saturable reactor SR is reset by the voltage difference between the reverse secondary winding voltage V_{S2} and the magamp controlled voltage V_A.

During the time period d_1T, the switch is turned off and the energy in the magnetising inductance is released to the output V_{O1}. In this period, the diode D_1 is on and the secondary winding voltage V_{S1} is clamped at the output voltage V_{O1}. The saturable reactor SR is in the blocking state and is set with the voltage difference between the secondary winding voltage V_{S2} and the output voltage V_{O2}. Ideally the stored energy in the main transformer is only supplied to the output V_{O1}.

As soon as the saturable reactor SR is saturated, the diode D_2 comes on and the secondary winding V_{S2} is clamped at the output voltage V_{O2}. Since the reflected voltage on the winding voltage V_{S1} is lower than the output voltage V_{O1}, the diode D_1 becomes reverse bias and is turned off. As a result, ideally the stored energy of the main transformer is only transferred to the output V_{O2} during the time period d_2T. At the end of the switching period, the main switch is turned on again and the saturable reactor SR is reset ready for next switching period.

According to the above descriptions, the following equation is needed to be satisfied to ensure the magamp set operation:

$$\frac{V_{O1}}{n_1} > \frac{V_{O2}}{n_2} \tag{1}$$

For the volt–sec and balance rule of the main transformer, we may have

$$V_g \cdot d = \frac{n_P}{n_1} \cdot V_{O1} \cdot d_1 + \frac{n_P}{n_2} \cdot V_{O2} \cdot d_2 \tag{2}$$

$$d + d_1 + d_2 = 1 \tag{3}$$

where n_P, n_1 and n_2 are winding turns for primary winding, output winding 1 and output winding 2, respectively.

To achieve continuity of magnetising current when the current flowing through output V_{O1} is switched to V_{O2}, the following equation is satisfied:

$$\frac{I_{O1} \cdot \frac{n_1}{n_P}}{d_1} = \frac{I_{O2} \cdot \frac{n_2}{n_P}}{d_2} + \frac{1}{2} \cdot \frac{V_g \cdot d \cdot T}{L_M} \tag{4}$$

where I_{O1} and I_{O2} are the average current of output 1 and output 2, respectively.

Substituting (2) and (3) into (4) yields

$$d^3 + p \cdot d^2 + q \cdot d + r = 0 \tag{5}$$

where $p = -(\frac{V_1}{V_g+V_1} + \frac{V_2}{V_g+V_2})$

$$q = \frac{2 \cdot L_M}{T} \cdot \frac{(V_2 - V_1)}{V_g} \cdot \left[\frac{I_1}{V_g + V_2} + \frac{I_2}{V_g + V_1}\right] + \frac{V_1 \cdot V_2}{(V_g + V_1)(V_g + V_2)}$$

$$r = -\frac{2 \cdot L_M}{T} \cdot \frac{(V_2 - V_1) \cdot (I_1 \cdot V_1 + I_2 \cdot V_2)}{V_g \cdot (V_g + V_1) \cdot (V_g + V_2)}$$

$$V_1 = \frac{n_P}{n_1} \cdot V_{O1},\ V_2 = \frac{n_P}{n_2} \cdot V_{O2},$$

$$I_1 = \frac{n_1}{n_P} \cdot I_{O1},\ I_2 = \frac{n_2}{n_P} \cdot I_{O2}$$

To solve the root d of the third-order (5), one may follow the procedure in the Appendix (Section 7). As soon as d is found, it would be easy to find d_1 and d_2 from (2) and (3). Figure 3 shows the relations of duty cycles versus load conditions that are applied to the example in Section 4.

Since it is hard to find a root of the third-order equation or a higher-order equation, approximation could be made by assuming that the current ripples are negligible. The approximate equation can be obtained from (4) by neglecting the last item

$$\frac{I_P}{d} = \frac{I_1}{d_1} = \frac{I_2}{d_2} = I_{MA} \tag{6}$$

where I_{MA} is the average magnetising current of transformer.

From (6), we find that the relations between duties and input/output depend on the average currents. This is a very interesting feature. In most topologies of switching mode power supplies, the relations are dominated by voltages rather than currents.

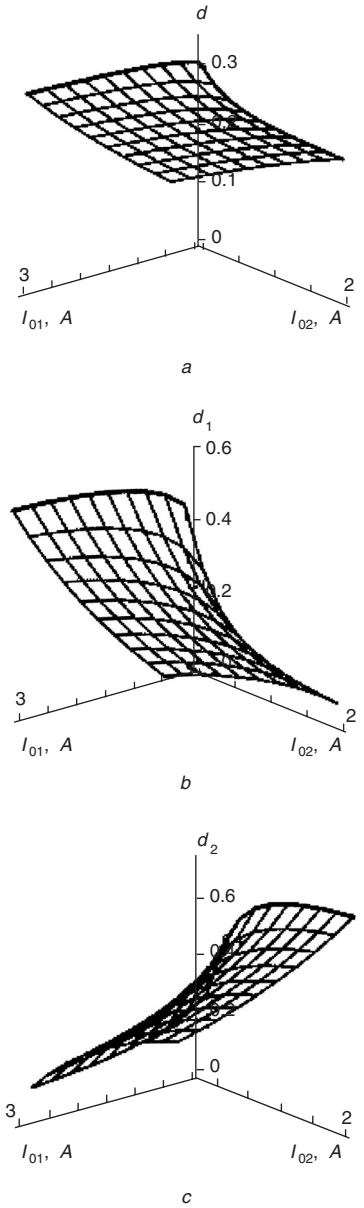

Fig. 3 *Duty cycles plotted against load conditions*
$V_g = 20$ V, $V_{O1} = 3.3$ V, $V_{O2} = 5$ V, $I_{O1} = 0$–3 A, $I_{O2} = 0$–2 A
a duty d
b duty d_1
c duty d_2

3 Analytical model with nonideal characteristics of components

In practical design, the performance of the flyback converter with magamp application is limited by the nonideal characteristics of the components. Since the energy delivery for each output depends on the current sharing principle, some parasitic parameters such as leakage inductance and saturated inductance may limit the rate of current flow. These will not only constrain the number of outputs, but also the operating area under extreme load conditions.

An analytical model is now proposed to explore the internal mechanism and to investigate the critical factors that affect proper operation.

3.1 Circuit analysis of proposed analytical model

To simplify the analysis, some reasonable assumptions are made: first, when the main switch and the diodes are turned on, they are considered as short circuits. The voltage drop of onresistance (Rds,on) of the main switch is negligible compared with the input voltage V_g. In the low output voltage application, the drops of the diodes could be lumped with the output voltages. Under the off state, they are represented as an open circuit.

Secondly, the main transformer can be represented as an ideal transformer with a magnetising inductance L_M and equivalent leakage inductances, L_{KP}, L_{K1} and L_{K2}, corresponding to primary winding, secondary winding 1 and secondary winding 2, respectively. The voltage drops of the winding resistances are small enough compared with the input voltage V_g and output V_{O1} and V_{O2}. They are neglected in the model.

Thirdly, the output capacitances C_1, C_2 and the capacitance of the clamp snubber C_C are sufficiently large that the voltages across these capacitances could be considered to be constant during the switching cycle.

Finally, the behaviour of the saturable reactor SR can be modelled as an inductance L_{SR} when saturated. During block operation, it could be viewed as an open circuit. The core loss due to the hysteresis characteristics is sufficiently small so that it can be neglected.

The equivalent circuit model of Fig. 1 is shown in Fig. 4 where all secondary quantities have been referred to the primary side. A typical RC clamp snubber circuit is added on the primary side to prevent high voltage stress due to the energy stored in the leakage inductance L_{KP}.

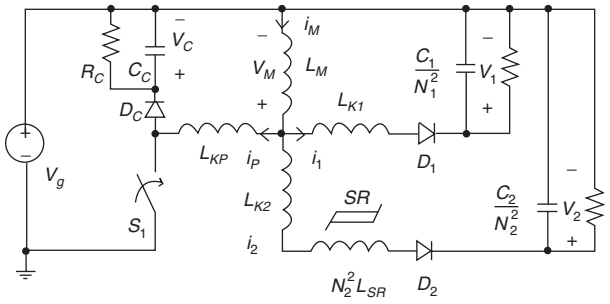

Fig. 4 *Equivalent circuit model of Fig. 1*

Figure 5*a* shows the key waveforms that are simulated by the proposed equivalent model in normal continuous current mode. It would be easy to indicate that some current transition periods are inserted among every duty period in the previous ideal case. In particular, the time

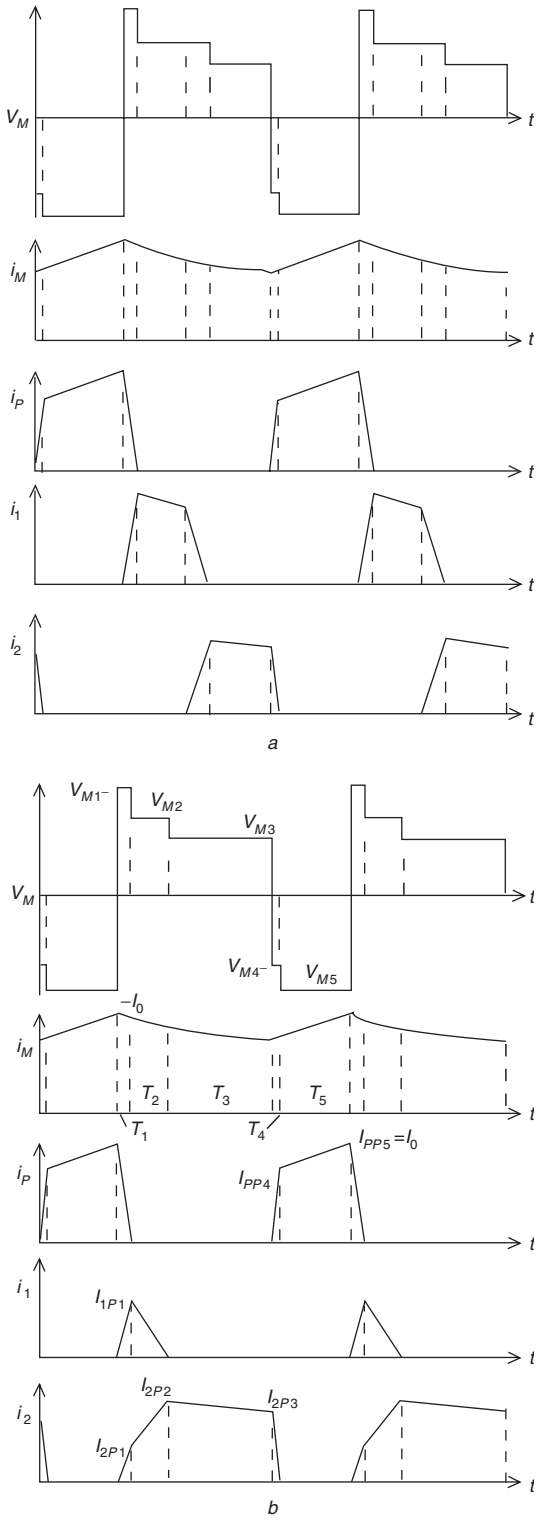

Fig. 5 *Key waveforms that are simulated by the proposed equivalent model*
a normal condition
b boundary condition

interval in which diodes D_1 and D_2 are on is the most evident in real applications and deserves attention. As the load of output 2 increases the duty for output 2 also increases but the blocking time of the saturable inductor decreases. Under the extreme load condition, the blocking time becomes a minimum. Since the current rise time is limited by the leakage inductance and the saturated inductance, output 2 cannot obtain enough energy and becomes nonoperational. Figure 5*b* shows the key waveforms under extreme load conditions.

3.1.1 T_1 time interval: At the beginning of the T_1 time interval, the main switch S_1 is turned off. The magnetising current starts to charge outputs 1 and 2. At the same time the energy stored in the leakage inductance L_{KP} is absorbed by the capacitor of the RC clamp snubber. The equivalent circuit during the T_1 interval is represented as that shown in Fig. 6*a*. Thus, one can obtain the following equations:

$$i_M = i_P + i_1 + i_2 \tag{7}$$

$$i_M(t) = -\frac{V_{M1}}{L_M} \cdot t + I_0 \tag{8}$$

$$i_P(t) = \frac{(V_{M1} - V_C)K_P}{L_M} \cdot t + I_0 \tag{9}$$

$$i_1(t) = \frac{(V_{M1} - V_1)K_1}{L_M} \cdot t \tag{10}$$

$$i_2(t) = \frac{(V_{M1} - V_2)K_2}{L_M} \cdot t \tag{11}$$

Substituting (8)–(11) into (7), we obtain

$$\begin{aligned} -V_{M1} =& (V_{M1} - V_C)K_P \\ &+ (V_{M1} - V_1)K_1 + (V_{M1} - V_2)K_2 \end{aligned} \tag{12}$$

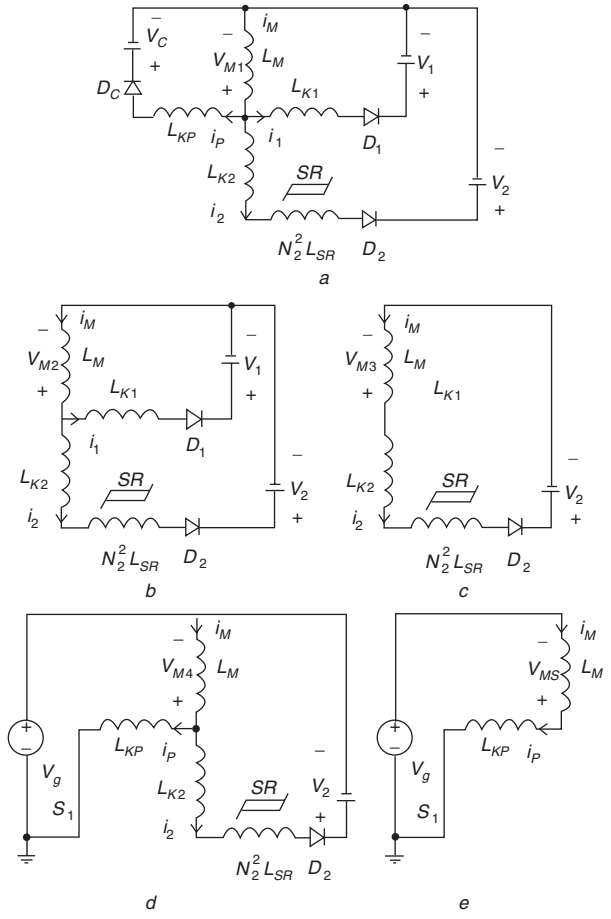

Fig. 6 *Equivalent circuit for different time intervals*
a T_1 time interval
b T_2 time interval
c T_3 time interval
d T_4 time interval
e T_5 time interval

Solving (12) for V_{M1} yields

$$V_{M1} = \frac{K_1V_1 + K_2V_2 + K_PV_C}{1 + K_1 + K_2 + K_P} \tag{13}$$

At the end of the T_1 interval, T_1 is obtained from (9) by letting $i_P(T_1) = 0$.

$$T_1 = \frac{L_MI_0}{K_P} \cdot \frac{1 + K_1 + K_2 + K_P}{V_C + K_1V_C + K_2V_C - K_1V_1 - K_2V_2} \tag{14}$$

Substituting T_1 and V_{M1} into (10) and (11), the peak currents of i_1 and i_2 at the end of T_1 are, respectively

$$I_{1P1} = \frac{K_1}{K_P} \cdot \frac{K_2V_2 + K_PV_C - V_1 - K_2V_1 - K_PV_1}{V_C + K_1V_C + K_2V_C - K_1V_1 - K_2V_2} \cdot I_0 \tag{15}$$

$$I_{2P1} = \frac{K_2}{K_P} \cdot \frac{K_1V_1 + K_PV_C - V_2 - K_1V_2 - K_PV_2}{V_C + K_1V_C + K_2V_C - K_1V_1 - K_2V_2} \cdot I_0 \tag{16}$$

In this period, the energy stored in the leakage L_{KP} had been transferred to the RC clamp snubber. Assuming the voltage V_C is constant, the energy will be dissipated by the resistance R_C. The total power loss of snubber can be derived as follows:

$$\begin{aligned} P_{RC} &= \frac{1}{T}\int_0^{T_1} V_C \cdot i_P(t) \cdot dt \\ &= \frac{L_MI_0^2}{2T} \cdot \frac{(1 + K_1 + K_2 + K_P)V_C}{K_P(V_C + K_1V_C + K_2V_C - K_1V_1 - K_2V_2)} = \frac{V_C^2}{R_C} \end{aligned} \tag{17}$$

Solving (17), the voltage of the snubber capacitor C_C is

$$V_C = \frac{(K_1V_1 + K_2V_2) + \sqrt{(K_1V_1 + K_2V_2)^2 + \frac{2L_MR_CI_0^2(1+K_1+K_2+K_P)(1+K_1+K_2)}{T \cdot K_P}}}{2(1 + K_1 + K_2)} \tag{18}$$

3.1.2 T_2 time interval:

As the current of L_{KP} decreases to zero, the diode D_C is reverse biased and the operation enters the T_2 time interval. The equivalent circuit model is given in Fig. 6*b*. Similarly, the following equations can be obtained:

$$i_M = i_1 + i_2 \tag{19}$$

$$i_M(t) = -\frac{V_{M2}}{L_M} \cdot t + I_{1P1} + I_{2P1} \tag{20}$$

$$i_1(t) = \frac{(V_{M2} - V_1)K_1}{L_M} \cdot t + I_{1P1} \tag{21}$$

$$i_2(t) = \frac{(V_{M2} - V_2)K_2}{L_M} \cdot t + I_{2P1} \tag{22}$$

Similarly, V_{M2} can be found as

$$V_{M2} = \frac{K_1V_1 + K_2V_2}{1 + K_1 + K_2} \tag{23}$$

T_2 is also obtained from (21) by letting $i_1(T_2) = 0$.

$$T_2 = \frac{L_MI_0}{K_P} \cdot \frac{1 + K_1 + K_2}{V_1 + K_2V_1 - K_2V_2} \cdot \frac{K_2V_2 + K_PV_C - V_1 - K_2V_1 - K_PV_1}{V_C + K_1V_C + K_2V_C - K_1V_1 - K_2V_2} \tag{24}$$

Substituting (16), (23) and (24) into (22), we can obtain the peak current I_{2P2}

$$I_{2P2} = \frac{K_2(V_1 - V_2)}{V_1 + K_2V_1 - K_2V_2} \cdot I_0 \tag{25}$$

3.1.3 T_3 time interval:

When the current of diode D_2 decays to zero, the T_3 time interval begins. Only L_M and L_{K2} have current through it. The equivalent circuit model during T_3 is shown in Fig. 6*c*. Similarly to the T_1 and T_2 intervals, we have

$$i_M = i_2 \tag{26}$$

$$i_M(t) = -\frac{V_{M3}}{L_M} \cdot t + I_{2P2} \tag{27}$$

$$i_2(t) = \frac{(V_{M3} - V_2)K_2}{L_M} \cdot t + I_{2P2} \tag{28}$$

Solving (26)–(28), V_{M3} can be derived as

$$V_{M3} = \frac{K_2V_2}{1 + K_2} \tag{29}$$

Substituting (25) and (29) into (28), the peak current of i_2 at the end of T_3 is

$$I_{2P3} = \frac{-K_2V_2}{L_M(1 + K_2)} \cdot T_3 + \frac{K_2(V_1 - V_2)}{V_1 + K_2V_1 - K_2V_2} \cdot I_0 \tag{30}$$

3.1.4 T_4 time interval:

At the beginning of the T_4 interval, the main switch turns on again and then the input starts to charge L_M. Figure 6*d* shows the equivalent circuit model in the T_4 interval. As in the previous process, we have

$$i_M = i_P + i_2 \tag{31}$$

$$i_M(t) = -\frac{V_{M4}}{L_M} \cdot t + I_{2P3} \tag{32}$$

$$i_P(t) = \frac{(V_{M4} + V_g)K_P}{L_M} \cdot t \tag{33}$$

$$i_2(t) = \frac{(V_{M4} - V_2)K_2}{L_M} \cdot t + I_{2P3} \tag{34}$$

Solving (31)–(34), V_{M4} is

$$V_{M4} = \frac{K_2V_2 - K_PV_g}{1 + K_2 + K_P} \tag{35}$$

T_4 is obtained from (34) by letting $i_2(T_4) = 0$.

$$T_4 = \frac{L_M}{K_2} \cdot \frac{1 + K_2 + K_P}{V_2 + K_PV_2 + K_PV_g} \cdot \left(\frac{-K_2V_2}{L_M(1 + K_2)} \cdot T_3 + \frac{K_2(V_1 - V_2)}{V_1 + K_2V_1 - K_2V_2} \cdot I_0\right) \tag{36}$$

And the peak current of i_P at the end of T_4 can be found by substituting (35) and (36) into (33)

$$I_{PP4} = \frac{K_P}{K_2} \cdot \frac{V_g + K_2V_g + K_2V_2}{V_2 + K_PV_2 + K_PV_g} \cdot \left(\frac{-K_2V_2}{L_M(1 + K_2)} \cdot T_3 + \frac{K_2(V_1 - V_2)}{V_1 + K_2V_1 - K_2V_2} \cdot I_0\right) \tag{37}$$

3.1.5 T_5 time interval:

As long as the current i_2 drops to zero, the diode D_2 is off and the current loop through L_M and L_{KP} only exists on the primary side. The equivalent circuit model is presented in Fig. 6*e*. Similarly, one may obtain

$$i_M = i_P \tag{38}$$

$$i_M(t) = -\frac{V_{M5}}{L_M} \cdot t + I_{PP4} \tag{39}$$

$$i_P(t) = \frac{(V_{M5} + V_g)K_P}{L_M} \cdot t + I_{PP4} \tag{40}$$

Solving (38)–(40) for V_{M5} yields

$$V_{M5} = \frac{-K_P V_g}{1 + K_P} \tag{41}$$

Substituting (37) and (41) into (40), the peak current I_{PP5} is expressed by

$$I_{PP5} = \frac{K_P V_g}{L_M(1 + K_P)} \cdot T_5 + \frac{K_P}{K_2} \cdot \frac{V_g + K_2 V_g + K_2 V_2}{V_2 + K_P V_2 + K_P V_g} \cdot \left[\frac{-K_2 V_2}{L_M(1 + K_2)} \cdot T_3 + \frac{K_2(V_1 - V_2)}{V_1 + K_2 V_1 - K_2 V_2} \cdot I_0 \right] \tag{42}$$

Due to the continuity of the inductor current in steady state operation, the following equation is satisfied:

$$I_{PP5} = I_0 \tag{43}$$

Substituting (43) into (42), one can obtain

$$T_5 - A \cdot T_3 = B \cdot I_0 \tag{44}$$

where

$$A = \frac{V_2(1 + K_P)(V_g + K_2 V_g + K_2 V_2)}{V_g(1 + K_2)(V_2 + K_P V_2 + K_P V_g)}$$

$$B = \frac{L_M V_2(1 + K_P)(V_1 + K_2 V_1 - K_2 V_2 + K_P V_1 + K_P V_g)}{K_P V_g(V_2 + K_P V_2 + K_P V_g)(V_1 + K_2 V_1 - K_2 V_2)}$$

For a switching period T, we have

$$T = T_1 + T_2 + T_3 + T_4 + T_5 \tag{45}$$

Substituting (14), (24) and (36) into (45) yields

$$T_5 + C \cdot T_3 = T - D \cdot I_0 \tag{46}$$

where

$$C = \frac{K_P(V_g + K_2 V_g + K_2 V_2)}{(1 + K_2)(V_2 + K_P V_2 + K_P V_g)}$$

$$D = \frac{L_M(V_1 + K_2 V_1 - K_2 V_2 + K_P V_1 + K_P V_g)}{(V_2 + K_P V_2 + K_P V_g)(V_1 + K_2 V_1 - K_2 V_2)}$$

T_3 and T_5 can be obtained by solving (44) and (46)

$$T_3 = \frac{V_g(1 + K_2)}{V_g + K_2 V_g + K_2 V_2} \cdot T - \frac{L_M(1 + K_2)}{K_P} \cdot \frac{(V_1 + K_2 V_1 - K_2 V_2 + K_P V_1 + K_P V_g)}{(V_g + K_2 V_g + K_2 V_2)(V_1 + K_2 V_1 - K_2 V_2)} \cdot I_0 \tag{47}$$

$$T_5 = \frac{V_2(1 + K_P)}{V_2 + K_P V_2 + K_P V_g} \cdot T \tag{48}$$

3.2 Analytical expression of boundary condition

Based on the above analysis, the average currents of outputs 1 and 2 under the boundary condition are calculated as follows:

$$I_{1A} = \frac{1}{2T} \cdot I_{1P1} \cdot (T_1 + T_2) = \frac{K_1 L_M I_0^2}{2K_P T} \cdot \frac{(K_2 V_2 + K_P V_C - V_1 - K_2 V_1 - K_P V_1)}{(V_C + K_1 V_C + K_2 V_C - K_1 V_1 - K_2 V_2)(V_1 + K_2 V_1 - K_2 V_2)} \tag{49}$$

$$I_{2A} = \frac{1}{2T} \cdot [I_{2P1}(T_1 + T_2) + I_{2P2}(T_2 + T_3) + I_{2P3}(T_3 + T_4)] = E \cdot I_{1A} + \frac{1}{2T} \cdot [I_{2P2}(T_2 + T_3) + I_{2P3}(T_3 + T_4)] \tag{50}$$

where $E = \frac{K_2(K_1 V_1 + K_P V_C - V_2 - K_1 V_2 - K_P V_2)}{K_1(K_2 V_2 + K_P V_C - V_1 - K_2 V_1 - K_P V_1)}$

The solution of (50) can be obtained easily by substituting each individual item that has already been derived before. However, it is trivial and too complex to analysis the relation between I_{1A} and I_{2A}. To obtain an analytical expression of the boundary condition, some reasonable assumptions could be made. First, since T_2 and T_4 are transition periods, they could be neglected compared with T_3. Secondly, the magnetising inductance L_M is large enough, so that the can decay can be neglected during T_3, i.e. $I_{2P2} \approx I_{2P3} \approx I_0$. Finally, the leakage inductances L_{K1}, L_{K2}, L_{KP} and the saturated inductance L_{SR} are much smaller than the magnetising inductance L_M, such that K_1, K_2 and $K_P >> 1$.

Equation (50) can be approximated by

$$I_{2A} \approx E \cdot I_{1A} + \frac{I_0 \cdot T_3}{T} \tag{51}$$

Equation (47) can be also approximated by

$$T_3 \approx \frac{V_g}{V_g + V_2} \cdot T - I_0 \left[\frac{L_{KP}}{V_g + V_2} + \frac{(L_{K2} + N_2^2 L_{SR})(V_g + V_1)}{(V_1 - V_2)(V_g + V_2)} \right] \tag{52}$$

Substituting (52) into (51) yields

$$I_{2A} \approx E \cdot I_{1A} + \frac{V_g}{V_g + V_2} I_0 - \frac{I_0^2}{T} \left[\frac{L_{KP}}{V_g + V_2} + \frac{(L_{K2} + N_2^2 L_{SR})(V_g + V_1)}{(V_1 - V_2)(V_g + V_2)} \right] \tag{53}$$

Equation (53) will help us to understand the factors that affect the boundary condition in Section 4.

4 Experimental results

To illustrate the effectiveness of the previous analysis, some experimental results are given below. A 20 W two-output flyback converter is constructed having the following parameters:

input range V_g	$20 - 30\,V$
output V_{O1}	$3.3\,V/0 - 3\,A$
output V_{O2}	$5\,V/0 - 2\,A$
switching period T	10 μS
turn number $n_P/n_1/n_2$	10/3/8
leakage inductance $L_{KP}/L_{K1}/L_{K2}$	0.95/0.96/0.94 μH
magnetising inductance L_M	70 μH
saturated inductance L_{SR}	0.45 μH

The core number of the main transformer is EI33 from TDK corporation. The saturable reactor has eight turns and the core number is MP1506 from Allied Signal. The common used current reset scheme is applied to reset saturable reactor. The clamp snubber capacitance and resistance are 0.1 uF and 1 kΩ, respectively. The output diode D_1 is a Schottky diode SBL840 from Transys Electronics Limited and the diode D_2 is a fast diode SF1004G from Taiwan Semiconductor

Co. Ltd. Since both output voltages are low, the voltage drops of diodes are taken into account in the simulations. The voltage drops of D_1 and D_2 under boundary load conditions are 0.1 V and 0.9 V, respectively.

Figure 7 shows some experimental waveforms under: (a) half load; (b) full load; (c) boundary load conditions. In Fig. 7, V_P is the voltage across the primary winding of the transformer as shown in Fig. 1 and i_{O1}, i_{O2} are the instantaneous currents of outputs 1 and 2, respectively. Figure 8 shows the boundary condition for the average output currents I_{O1} and I_{O2} with both the analytical model and experimental results. It is obvious that the experimental results are in good agreement with the proposed analytical model. We can find the boundary conditions when the output current I_{O2} is a heavy load and I_{O1} is a light load. On the left side of the boundary line, output 2 becomes out of regulation. The results also verify the effectiveness of (50). However, (50) is complex and trivial. The simplified (53) is more comprehensive and analytical. In (53), output currents I_{1A} and I_{2A} are a function of I_0 which depends on the load condition. The only nonideal factors that affect the boundary (53) are the leakage inductances L_{KP}, L_{K2} and

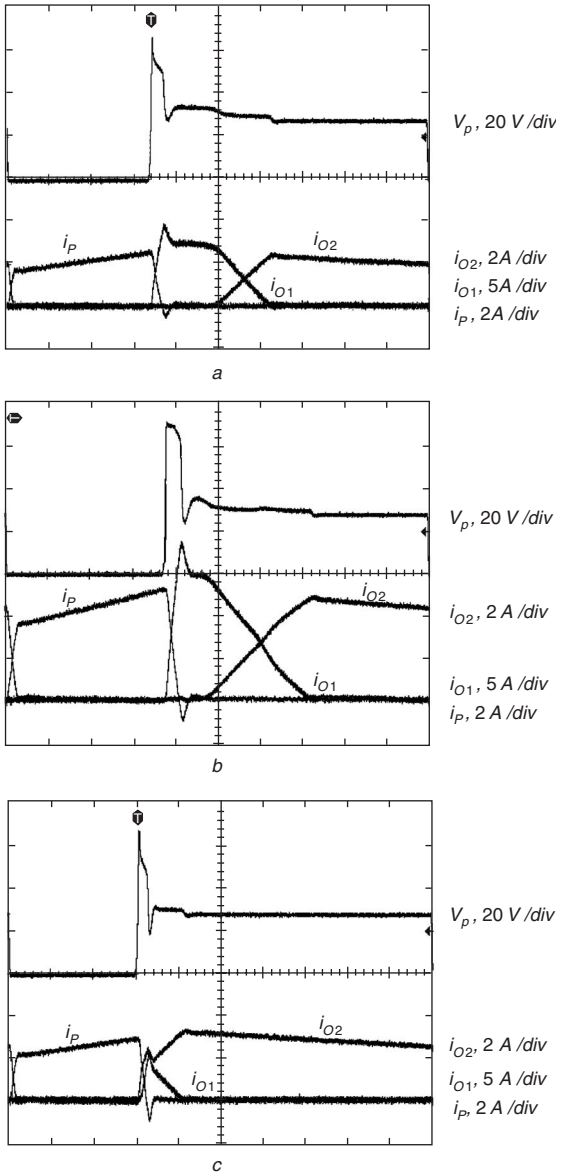

Fig. 7 *Some experimental waveforms time scale is 1 μs/div*
a half load: $V_g = 20$ V, $I_{O1} = 3$ A, $I_{O2} = 2$ A
b full load: $V_g = 20$ V, $I_{O1} = 1.5$ A, $I_{O2} = 1$ A
c boundary load: $V_g = 20$ V, $I_{O1} = 0.249$ A, $I_{O2} = 2$ A

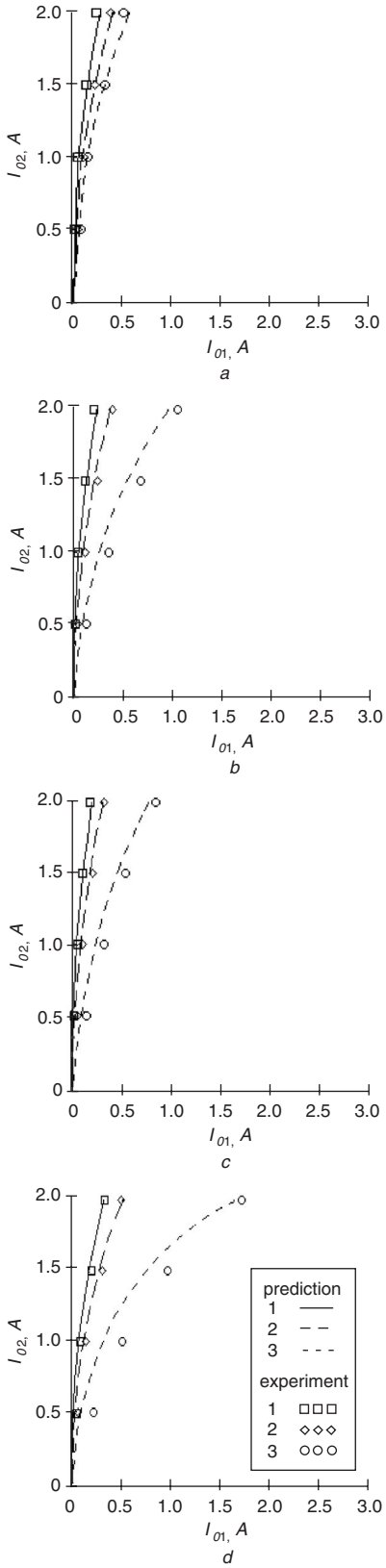

Fig. 8 *Experimental results with different design conditions*
a under $V_g = 20$ V, $T = 10$ μs and $n_2 = 8$ T
condition: 1 $L_{SR} = 0.45$ μH, 2 $L_{SR} = 0.7$ μH, 3 $L_{SR} = 1$ μH
b under $V_g = 20$ V, $T = 10$ μs and $L_{SR} = 0.45$ μH
condition: 1 $n_2 = 8$ T, 2 $n_2 = 7$ T, 3 $n_2 = 6$T
c under $V_g = 30$ V, $T = 10$ μs and $L_{SR} = 0.45$ μH
condition: 1 $n_2 = 8$ T, 2 $n_2 = 7$ T, 3 $n_2 = 6$ T
d under $V_g = 20$ V, $T = 6.67$ μs and $L_{SR} = 0.45$ μH
condition: 1 $n_2 = 8$ T, 2 $n_2 = 7$ T, 3 $n_2 = 6$ T

the saturated inductance L_{SR}. The current rise time is limited by these factors. Hence, the magnetising inductance L_M cannot supply enough energy to output 2 beyond the boundary. The other factors of (53) are designed parameters such as the switching period T, input voltage V_g, output voltages V_1, V_2, turn ratio N_2 and the turns of the saturable reactor. Figure 8*a–d* show the effectiveness of the designed factors with different values compared to the original design.

In Fig. 8*a*, three different turns of saturable reactor are provided: condition 1 is the original value: 8 turns and $L_{SR} = 0.45\,\mu H$, condition 2 is 10 turns and $L_{SR} = 0.7\,\mu H$ and condition 3 is 12 turns and $L_{SR} = 1\,\mu H$. It can be seen that the boundary lines move toward the right with increasing turns of the saturable reactor. This complies with the conclusion of (53) that the larger the leakage inductances and the saturated inductance are, the worse the boundary condition is. It seems that fewer turns of the saturable reactor are preferred. However, the side effects should be considered to reduce the saturated inductance. More reset current from the controller is needed when the turns of the saturable reactor are decreased. On the other hand, it reduces the volt–second blocking range of the saturable inductor.

Since the output voltages V_{O1} and V_{O2} are defined by the specification, the actual designed factors are the turn ratios for V_1 and V_2. The turn ratio N_1 for the main output V_1 can be designed by the traditional approach. However, the turn ratio N_2 for the magamp output V_2 becomes a critical factor affecting the boundary. Figure 8*b* shows the effect with three different turns for winding 2 i.e. condition 1 is the original value: $n_2 = 8$ turns, condition 2: $n_2 = 7$ turns and condition 3: $n_2 = 6$ turns. As the winding turns of output 2 decrease, the voltage difference between V_1 and V_2 will be reduced. It can be observed from (53) that the third item in the right-hand side of the equation will be increased and the boundary lines are shifted to the right. The major reason is that reducing the voltage difference V_1–V_2 across L_{K2} will increase the current rise time. This factor becomes significant when the voltage difference is too small. To prevent this, one should increase the winding turns. However, this will increase the voltage stress on the output diode.

As the input voltage V_g is changed to a high line voltage ($V_g = 30\,V$), all the boundary lines with the same conditions as in Fig. 8*b* are shifted to the left. This is because higher input voltage can speed up the current rise time. The effect is shown in Fig. 8*c*. This also means that the worse case condition is under the low line condition.

In Fig. 8*d*, the switching frequency is increased to 150 kHz, i.e. the switching period ($T = 6.67\,\mu S$) becomes two-thirds of the original value. The boundary lines with the same conditions as in Fig. 8*b* are moved further towards the right. This is because the time period for the current distribution is further limited. This can be also explained by (53), that decreasing the switching period will also be increase the third item.

From the above discussions, the design becomes a trade-off problem. One should design the parameters carefully to obtain the optimum performance. However, under any condition, the minimum load requirement on output 1 is necessary to keep regulation. A simple and cost effective way to solve this issue is to add a preload on output 1. In this example, a 1 W preload is placed to meet the 1% regulation requirement. Figure 9 shows the cross-regulation of output V_{O1} and V_{O2} (without and with magamp, respectively). Output V_{O1} is controlled by the PWM feedback loop. The cross-regulation of output V_{O1} meets

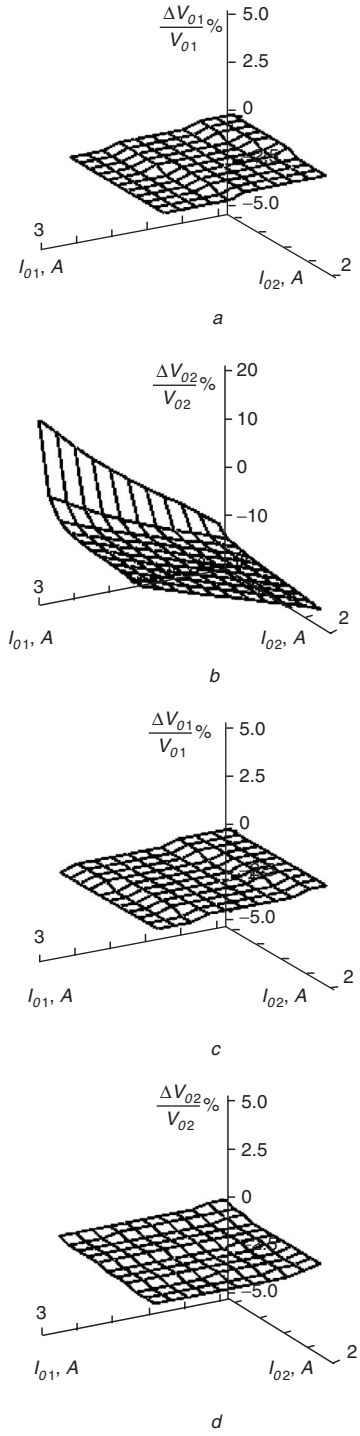

Fig. 9 *Cross-regulation of output V_{O1}, V_{O2}*
a output V_{O1} without magamp
b output V_{O2} without magamp
c output V_{O1} with magamp
d output V_{O2} with magamp

the 1% (0.3–0.3%) regulation requirement for with and without magamp condition. On the other hand, the cross-regulation of output V_{O2} without magamp control is varied from 16.9–16.9%. As the saturable reactor is added and the magamp feedback loop is enabled, the cross-regulation of output V_{O2} is well under 1% (0.4–0.4%) regulation requirement.

5 Conclusions

We have investigated the operation of the magamp postregulator in flyback converters with multiple output

windings. The circuit of the magamp regulator looks similar to that of the forward converters. But the operating principle is totally different. The output of the main transformer in the flyback converter is viewed as a current source. The energy is supplied to each output winding by the time-sharing approach. Due to the leakage inductances and the saturated inductance, the current rise time is limited so that some transition periods are inserted. The proposed analytical model effectively explains the mechanism of the regulation boundary. The experimental results matched the predicted boundary conditions. A simple analytical expression is derived to explain the factors that affect the boundary lines, such as: leakage inductance, saturated inductance, switching frequency and input voltage. To maintain the regulation, a minimum load is required. Finally, the experimental example shows the effective of applying the magamp in the flyback converter. Both output regulations are excellent with a 1 W preload on output 1.

6 References

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7 Appendix

For a cubic equation

$$d^3 + p \cdot d^2 + q \cdot d + r = 0 \tag{54}$$

One may reduce (54) to the form by substituting for d with the value, $x - p/3$.

$$x^3 + a \cdot x + b = 0 \tag{55}$$

where $a = (1/3)(3q - p^2)$ and $b = (1/27)(2p^3 - 9pq + 27r)$.

Equation (54) with $ab \neq 0$ can be always solved by transforming it to the trigonometric identity. Let $x = m \cos\theta$, then

$$x^3 + ax + b = m^3 \cos^3\theta + am\cos\theta + b = 4\cos^3\theta - 3\cos\theta - \cos(3\theta) = 0 \tag{56}$$

Hence

$$\frac{4}{m^3} = -\frac{3}{am} = \frac{-\cos(3\theta)}{b} \tag{57}$$

from which it follows that:

$$m = 2\sqrt{-\frac{a}{3}} \tag{57}$$

$$\cos(3\theta) = \frac{3b}{am} \tag{58}$$

Any solution θ_1, which satisfies (59), will also have the solutions

$$\theta_1 + \frac{2\pi}{3} \text{ and } \theta_1 + \frac{4\pi}{3}$$

The roots of (55) are

$$2\sqrt{-\frac{a}{3}}\cos\theta_1, 2\sqrt{-\frac{a}{3}}\cos\left(\theta_1 + \frac{2\pi}{3}\right), 2\sqrt{-\frac{a}{3}}\cos\left(\theta_1 + \frac{4\pi}{3}\right)$$

Hence, the roots of (54) are

$$2\sqrt{-\frac{a}{3}}\cos\theta_1 - \frac{p}{3}, 2\sqrt{-\frac{a}{3}}\cos\left(\theta_1 + \frac{2\pi}{3}\right) - \frac{p}{3}, 2\sqrt{-\frac{a}{3}}\cos\left(\theta_1 + \frac{4\pi}{3}\right) - \frac{p}{3}$$