Low-voltage CMOS four-quadrant multiplier based on square-difference identity

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Abstract: A low-voltage CMOS four-quadrant multiplier based on the square-difference identity ($[a + b]^2 - a^2 - b^2$) is presented. This circuit has been implemented in a 0.8μm single-poly double-metal *n*-well CMOS process. Experimental results show that for a power supply of ±1.5V, the linear input range of this multiplier is within ±0.5V with the linearity error less than 1%. The total harmonic distortion is less than 1% with input range up to ±0.5V. The −3dB bandwidth of this multiplier is measured to be about 1MHz. Moreover, it can operate satisfactorily regardless of the transistor body connection. This circuit is expected to be useful in low-voltage analogue signal-processing applications.

1 Introduction

The reduction of the minimum feature size of an MOS transistor for digital VLSI circuits has been ongoing for the past few decades. As the channel length is scaled down into deep-submicrometre dimensions, the lower power supply voltage is required to ensure the device reliability [1]. To be compatible with digital VLSI technologies, analogue integrated circuits, which can operate at low supply voltages, are also receiving significant attention. A four-quadrant analogue multiplier is a very useful building block in many circuits such as adaptive filters, frequency doublers and modulators. Recently, some four-quadrant multipliers suitable for low-voltage operation have been developed [2–5]. Several of these multipliers exploited MOS transistors in the triode region. Although triode-based multipliers have the better harmonic performance than saturation-based ones for operating in low supply voltages [2], the frequency response of the triode-based multipliers is limited and additional level-shift circuits for the input signals are required. In this paper a low-voltage CMOS four-quadrant multiplier using transistors operating in the saturation region is presented. This circuit has been implemented in a 0.8μm single-poly double-metal CMOS process. Experimental results demonstrate the feasibility of the proposed multiplier.

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2 Circuit description

To realise the proposed multiplier the basic idea is based on the square-difference identity ($[a + b]^2 - a^2 - b^2 = 2ab$) [6–9]. Moreover, low-voltage designs must avoid stacking two or more transistors in series and the output must be taken from the drains of transistors to create a full-swing output signal. The proposed CMOS multiplier is shown in Fig. 1. The drain current I_D of an NMOS device can be described by

$$I_D = K(V_{GS} - V_T)^2 \quad (1)$$

where K is the transconductance parameter, V_{GS} is the gate-to-source voltage and V_T is the threshold voltage, respectively. Assume that the transistors, M_1 to M_7, are perfectly matched with the identical parameters K and V_T. Assume that all the MOS devices in Fig. 1 were biased in saturation. Let the aspect ratio of M_{10} be twofold that of M_9 and those of M_{11} and M_{12} be equal, too. The drain current of M_9 is equal to a half sum of currents of M_1 through M_6. Since the current of M_{11} (M_{12}) is equal to that of M_{10} (i.e. twice current of M_9), so the current mirrors consisting of M_9 through M_{12} will force the current I_a to zero. This positive feedback loop technique has been used to design operational transconductance amplifiers and active resistors [10, 11]. The working principle of the proposed multiplier is described as follows.

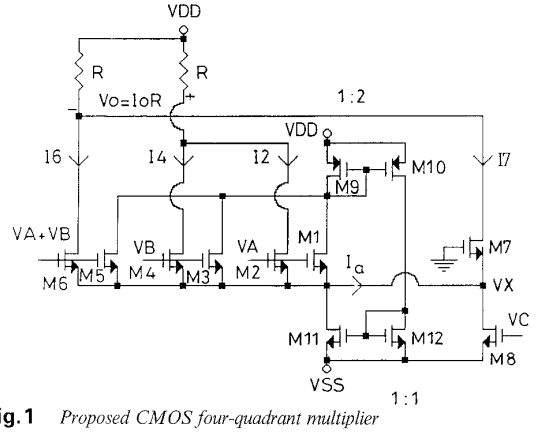

Fig. 1 *Proposed CMOS four-quadrant multiplier*

The current I_7 that flows through M_7 can be expressed by

$$I_7 = K(-V_X - V_T)^2 \quad (2)$$

The same current I_7 that flows through M_8 can be given as

$$I_7 = K_8(V_C - V_{SS} - V_{T8})^2 \quad (3)$$

where K_8 and V_{T8} is the transconductance parameter and threshold voltage of the device, M_8.

According to eqns. 2 and 3, the following relation can be obtained:

$$V_X = \sqrt{\frac{K_8}{K}}(V_{SS} - V_C) - V_T + \sqrt{\frac{K_8}{K}}V_{T8} \quad (4)$$

Furthermore, the drain currents of the devices M_2, M_4 and M_6 can be expressed as

$$I_2 = K(V_A - V_X - V_T)^2 \quad (5)$$

$$I_4 = K(V_B - V_X - V_T)^2 \quad (6)$$

$$I_6 = K(V_A + V_B - V_X - V_T)^2 \quad (7)$$

Thus, the output current, I_o, of this multiplier can be defined and expressed as

$$I_o = I_7 + I_6 - I_2 - I_4 = 2KV_AV_B \quad (8)$$

To guarantee linear operation for this circuit, the following constraints should be satisfied:

$$\min(V_A, V_B, V_A+V_B) > \sqrt{\frac{K_8}{K}}(V_{SS}-V_C)+\sqrt{\frac{K_8}{K}}V_{T8} \quad (9)$$

Because the devices M_1 to M_7, are biased with equal source-to-substrate voltages, they need not be built in individual wells, which will result in a saving of chip area. Moreover, the simple structure of this multiplier will be suitable for low supply voltages.

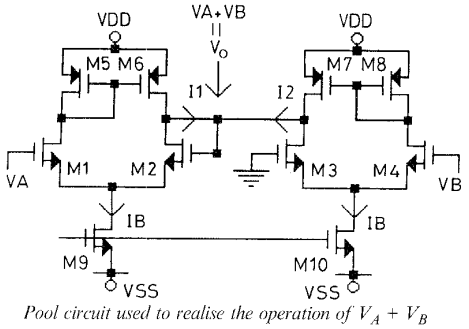

Fig. 2 *Pool circuit used to realise the operation of $V_A + V_B$*

The operation of $V_A + V_B$ can be realised using the circuit in Fig. 2. This circuit is called pool circuit [12–14]. Assume that the transistors in Fig. 2 are biased in the saturation region. The currents I_1 and I_2 in Fig. 2 can be expressed as

$$I_1 = K(V_A - v_o)\sqrt{\frac{2I_B}{K} - (V_A - v_o)^2} \quad (10)$$

$$I_2 = KV_B\sqrt{\frac{2I_B}{K} - V_B^2} \quad (11)$$

Therefore, at the equilibrium state,

$$v_o = V_A + V_B \quad (12)$$

Using the circuit in Fig. 2 to realise the operation $V_A + V_B$, a four-quadrant multiplier can be achieved. The linear input range of this multiplier is limited once both the magnitudes of V_A and V_B are positive or negative. The magnitude of $V_A + V_B$ approaching to the supply voltage will degrade the operation of the pool circuit and the proposed multiplier.

Table 1: Aspect ratios for all devices in Figs. 1 and 2

Fig. 1	Device	M_1–M_7	M_8, M_{11}, M_{12}	M_9	M_{10}
	$W\mu m/L\mu m$	5/20	20/5	10/5	20/5
Fig. 2	Device	M_1–M_4	M_5–M_8	M_9, M_{10}	
	$W\mu m/L\mu m$	8/5	5/5	20/5	

3 Experimental results

This circuit has been implemented in a 0.8μm single-poly double-metal *n*-well CMOS process. The layout photograph for the multiplier in Fig. 1 is shown in Fig. 3. The aspect ratios for all devices in Figs. 1 and 2 are listed in Table 1. The power supply voltages are ±1.5V and V_C = –0.5V. The measured transfer curves of the multiplier are shown in Fig. 4. The circuit has a nonlinearity error less than 1% over ±0.5V input range. The total harmonic distortion was less than 1% for $|V_A| < 0.5$V and V_B = 0.5V. A typical spectrum of the output waveform of the multiplier is shown in Fig. 5 where V_A is a 0.1 V_p, 30kHz sinusoidal signal and V_B = 0.5V. Fig. 6 shows the modulation application with V_B (the upper trace, 50mV/div) is a 0.04 V_p sinusoidal signal of 10kHz and V_A (the middle trace, 500mV/div) is a 0.6 V_p sinusoidal signal of 1kHz. The –3dB bandwidth was measured to be about 1MHz.

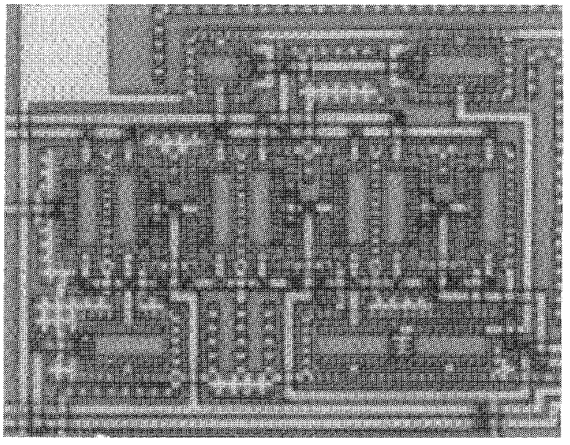

Fig. 3 *Layout photograph for the multiplier in Fig. 1*

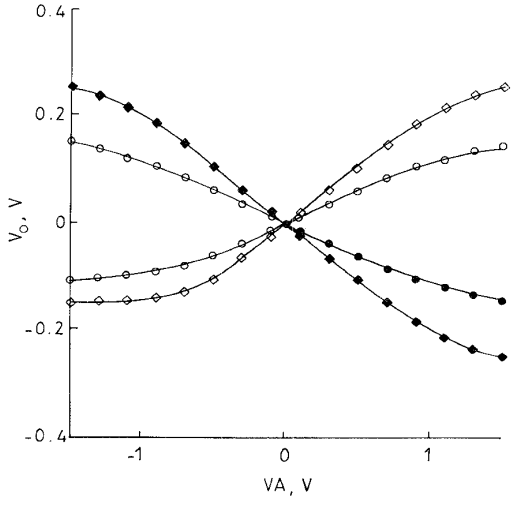

Fig. 4 *Measured transfer curves of the proposed multiplier in Fig. 1*
V_C = –0.5V
V_B is ±0.645V and ±0.327V
V_A changes from 1.5 to 1.5V
◇ V_B = 0.645V
○ V_B = 0.372V
● V_B = –0.372V
◆ V_B = –0.645V

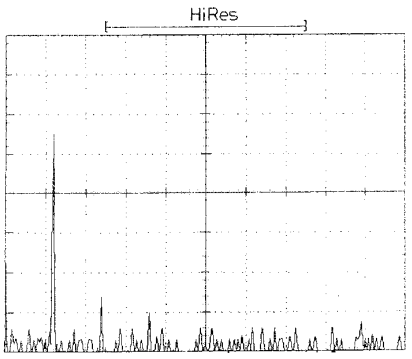

Fig. 5 *A typical spectrum of the output waveform of Fig. 1*
V_A is a 0.1 V_p sinusoidal signal of 30kHz and V_B = 0.5V
Vertical scale: 10dBm/div
Horizontal scale: 25kHz/div

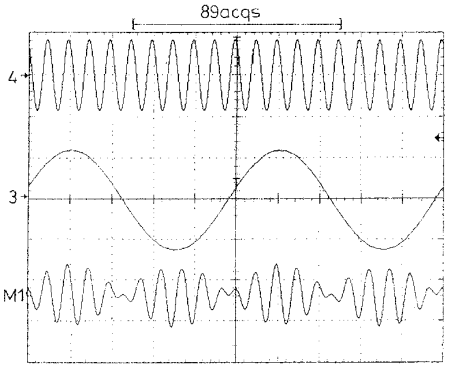

Fig. 6 *Measured modulator application of the multiplier*
V_B (the upper trace, 50mV/div) is a 0.04 V_p sinusoidal signal of 10kHz
V_A (the middle trace, 500mV/div) is a 0.6 V_p sinusoidal signal of 1kHz
Modulated output (the lowest trace) is 50mV/div
Horizontal scale is 0.2ms/div

4 Conclusions

In this paper, a new low-voltage CMOS four-quadrant multiplier has been proposed. It has been fabricated in a 0.8μm single-poly double-metal *n*-well CMOS process. This multiplier is expected to be useful in low-voltage analogue-signal processing applications.

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