

# A 10.8-mW Low-Noise Amplifier in 0.35- $\mu$ m SiGe BiCMOS for UWB Wireless Receivers

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**Abstract** — A UWB low-power and low-noise amplifier is proposed. The UWB LNA achieves better than 14.5-dB gain with 10.8-mW power consumption. The measured minimum noise figure is 3.1 dB and lower than 5.4 dB in the desired band. This MMIC is implemented in a commercial 0.35- $\mu$ m SiGe BiCMOS technology and occupies total chip size of only 0.74 mm<sup>2</sup> including all testing pads.

**Index Terms** — RFIC, low power, Silicon, SiGe BiCMOS, UWB, LNA.

## I. INTRODUCTION

UWB system is a new wireless technology capable of transmitting data over a wide spectrum of frequency bands with very low power and high data rates [1]-[3]. Although the UWB standard (IEEE 802.15.3a [2]) has not been completely defined, most of the proposed applications are allowed to transmit in a band between 3.1-10.6 GHz.

In recent years, narrow-band LNA designs have employed inductive source degeneration to achieve good input matching [4]-[7]. This technique also yields nearly optimal noise figure at the resonance frequency of the input network. Some low-noise amplifiers have been demonstrated for wideband applications [8]-[19]. A 30-mW high-gain LNA using LC-ladder matching network was proposed and implemented in 0.18- $\mu$ m SiGe HBT technology [8]. A 3.4-6.9-GHz LNA with inductive source degeneration consumes 3.5 mW for applications of low-end UWB radio spectrum [9]. A DC-7.8 GHz LNA using 0.25- $\mu$ m SiGe BiCMOS process was demonstrated for UWB and optical communication [10]. A Chebyshev matching CMOS LNA provides good input return loss with the noise figure from 4 to 9 dB in the desired band [12]. A conventional CMOS distributed amplifier (DA) can cover full-band UWB with low NF, but consumes high dc power [11]. A modified low-power distributed amplifier was proposed and demonstrated in [13]. Recently, two UWB LNA with resistive feedback technique were also demonstrated [14]-[15]. An LNA in 180-GHz SOI SiGe technology can operate at 14.5 mW

and only 2.7-3.9-dB NF, but the input return loss is only better than 2 dB [14]. The other demonstrates high gain and good NF performance in 150-GHz SiGe HBT process, but the dc power consumption is about 42.5 mW [15].

In this paper, a wideband low-noise amplifier in a low-cost process is demonstrated. The input impedance matching is achieved by multi-section structure in conjunction with cascode cell, which is terminated by inductive peaking and Darlington cascode configuration. The supply voltage is 1.8 V and consumes 6 mA. This MMIC can achieve a high gain and low noise figure performance with low power consumption even it is implemented in a 0.35- $\mu$ m SiGe BiCMOS technology.

## II. CIRCUIT DESIGN AND IMPLEMENTATION

The UWB LNA was implemented using TSMC commercial 0.35- $\mu$ m 3P3M SiGe BiCMOS technology, which provides three poly layers for the emitters and bases of the SiGe HBT and the gates of the CMOS transistors; three metal layers for interconnection. The HBT can offer  $f_{max}$  of 57 GHz. This process with low-resistivity substrate ( $\sim 10$  S/m) provides monolithic inductors with quality factor below 10.

One popular way to achieve a 50 ohm input resistance of an LNA is by inductive emitter degeneration as shown in the schematic diagram of Fig. 1. The use of the emitter degeneration can enhance the linearity and provide the input resistance, which is necessary for input matching. The implementation of the matching network can be easily derived as:

$$\begin{aligned} Z_{in}(s) &= \frac{1}{sC_{be}} + s(L_b + L_e) + \frac{g_m L_e}{C_{be}} \\ &= \frac{s^2 C_{be} (L_b + L_e) + s g_m L_e + 1}{s C_{be}} \end{aligned}$$

The emitter degeneration inductance  $L_e$  can transform the input impedance to a real part, generally designed to 50 ohm. The imaginary part of the input impedance can

be resonated with base and emitter inductance ( $L_b$  and  $L_e$ ). However, this impedance matching scheme is only suitable for narrow band application. Fig. 1 shows the simulated input impedance of the HBT transistor ( $0.3 \times 20.3 \mu\text{m}^2$ ) with emitter inductive degeneration ( $L_e$ ) and series base inductance ( $L_b$ ). According to the first order equation for input matching, the emitter degeneration can be determined by the transistor's transconductance ( $g_m$ ) and intrinsic base-emitter capacitance ( $C_{be}$ ). The selected  $L_e$  is about 0.2 nH for increasing the input resistance to match system impedance. Since our design goal is to achieve low input return loss, the input matching resistance of  $40 \Omega$  is selected to achieve better than 10-dB input return loss, which is determined by the value of  $L_e$  and trade off with small-signal gain. The series base inductance ( $L_b$ ) can be used to compensate the intrinsic base-emitter capacitance ( $C_{be}$ ). The zero crossing point of imagine part at 8 GHz can also be observed in Fig. 1, which means input impedance matching is only achieved around 8 GHz. For UWB band (3.1–10.6 GHz) application, the conventional impedance matching is difficult to meet the specification.

According to the above-mentioned analysis, more complex matching network is required to fulfill the UWB specifications. Another matching solution, shown in Fig. 2, expands the use of an inductively degenerated common-emitter amplifier by embedding the input network of the amplifying device in a multi-section reactive network so that the overall input reactance is resonated out over a wider bandwidth, which was first implemented in CMOS technology [12].

Since the input reactance of the conventional matching network shown in Fig. 1 is capacitive at lower frequency and inductive at higher frequency, the additional elements should compensate the reactance and maintain the resistance over the wide frequency band. Since the original matching is set at about 8 GHz, a shunt LC element is also set to be resonance at 8 GHz and provides inductive/capacitance at low/high frequency. This can potentially cancel the reactance of frequency response in Fig. 1. Fig. 3 illustrates the resistance and reactance of the compensated response. The reactance at 3–4 GHz is still difficult to be canceled. The series LC provides low-frequency capacitance to cancel out the reactance over 3–4 GHz, as shown in Fig. 3. The overall simulated input return losses from 3.1–10.6 GHz are all better than 10 dB.

The overall circuit schematic is shown in Fig. 4. The input active gain cell ( $Q_1$  and  $Q_2$ ) is cascode configuration. The load of the cascode cell ( $R_{L1}$  and  $L_{L1}$ ) is inductive peaking to extend operation bandwidth. The following stage is Darlington cascode configuration ( $Q_3$ ,  $Q_4$ , and  $Q_5$ )

to achieve higher gain performance and directly coupled to the first stage to reduce circuit complexity and chip size. However, the stability of the Darlington cascode configuration is also an important issue. The emitter inductive degeneration ( $L_{e2}$ ) can improve the stability. The output load is also inductive peaking ( $R_{L2}$  and  $L_{L2}$ ) for bandwidth extension and output matching, which is associated with  $L_3$ ,  $L_4$  and  $C_3$ . The supply voltage is 1.8 V and consumes total current of 6 mA.

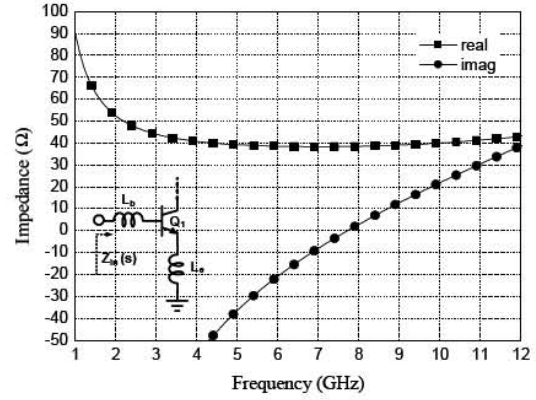


Fig. 1. Real and imaginary parts of input impedance of the HBT transistor with emitter inductive degeneration and series base inductance ( $L_b$ ).

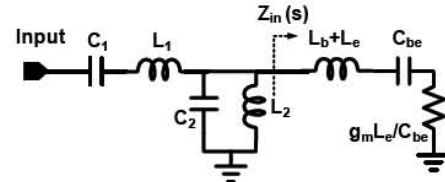


Fig. 2. Schematic of the LNA input network.

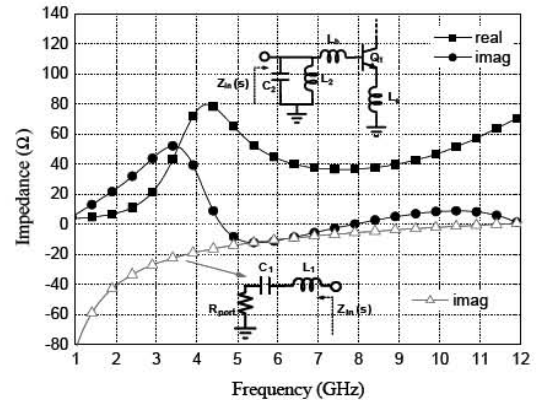


Fig. 3. Simulated input impedance.

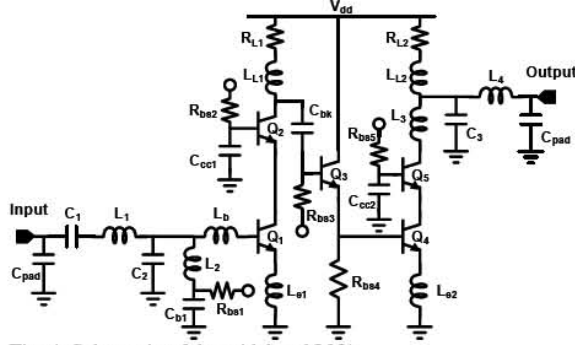


Fig. 4. Schematic of the wideband LNA.

### III. MEASUREMENT RESULTS

Fig. 5 shows chip photograph of the UWB LNA with chip size of only  $0.93 \text{ mm} \times 0.76 \text{ mm}$ . The UWB LNA was measured using on-wafer probing with GGB ground-signal-ground (GSG) probes. Fig. 6 shows the measured power gain and input/output return losses at 1.8-V supply and 6 mA. The power gain is better than 14.5 dB from 3 to 10.6 GHz while consuming 10.8 mW dc power. The input return loss is better than 7 dB and the output return loss is better than 10 dB in the entire desired band. The measured noise figure (NF) is also shown in Fig. 6. The noise figure is lower than 5.4 dB from 3.1 to 10.6 GHz. The lowest NF is 3.1 dB at 4.3 GHz.

The measured output  $P_{\text{ldB}}$  are between  $-14 \sim -12 \text{ dBm}$  from 3.1-10.6 GHz. The measured input third-order intercept points (IIP3) is about  $-19 \text{ dBm}$  from 3.1-10.6 GHz.

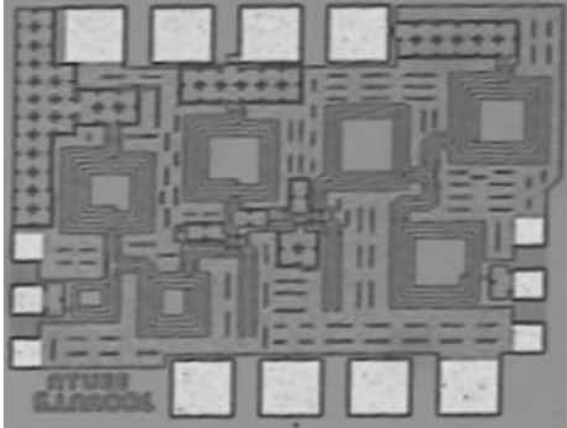


Fig. 5. Chip photograph of the multi-section UWB LNA (size:  $0.93 \text{ mm} \times 0.79 \text{ mm}$ ).

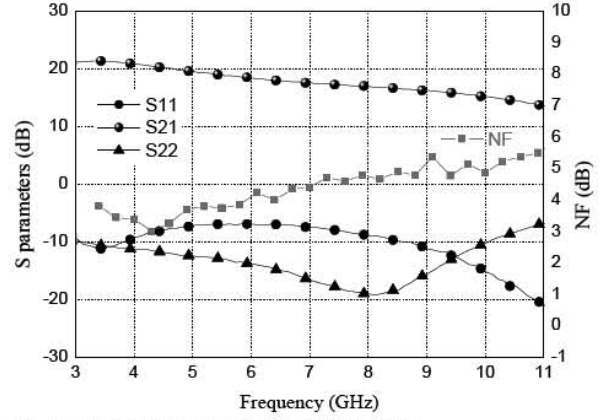


Fig. 6. Measured S parameters and noise figure.

### IV. CONCLUSION

A low-power and low-noise amplifier for 3.1-10.6-GHz ultra-wideband radio systems is demonstrated in this paper. The broadband amplifier is based on multi-section input impedance matching and Darlington cascode configuration. The inductive peaking is also used to improved bandwidth performance. The MMIC achieves better than 14.5-dB gain with 10.8-mW power consumption. The I/O return losses are better than 7 and 10 dB, respectively. The measured noise figures are 3.1 to 5.4 dB from 3.1 to 10.6 GHz. The chip size is only  $0.74 \text{ mm}^2$  including all testing pads. Table I summarizes the recently reported LNAs for UWB applications. This MMIC can achieve a high gain and low noise figure performance with low power consumption even it is implemented in low-cost  $0.35\text{-}\mu\text{m}$  SiGe BiCMOS technology.

### ACKNOWLEDGEMENT

This work is supported in part by the MediaTek Fellowship and National Science Council of Taiwan, R.O.C. (NSC 93-2219-E-002-016, NSC 93-2219-E-002-024, NSC 93-2213-E-002-033, and NSC 93-2752-E-002-002-PAE). The chip is fabricated by Taiwan Semiconductor Manufacturing Company (TSMC) through National Chip Implementation Center (CIC) of Taiwan, R.O.C.

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Table I  
RECENTLY REPORTED PERFORMANCES OF UWB LOW NOISE AMPLIFIERS.

Process	Freq. (GHz)	Gain (dB)	NF (dB)	I/O RL (dB)	Chip Size (mm <sup>2</sup> )	Total P <sub>dd</sub> (mW)	Topology	Ref.
0.18 $\mu$ m SiGe HBT	3 ~ 10	21	< 4.2	< -9	1.8	30*	LC-ladder match	ISSCC04 [8]
0.25 $\mu$ m SiGe HBT	3.4 ~ 6.9	10	< 5	< -6	1.39	3.5	Narrow-band L degeneration	MWCL04 [9]
0.25 $\mu$ m SiGe BiCMOS	DC ~ 7.8	10.6	< 4.4	< -7.8	0.45	6.5	Input active match	IMS04 [10]
0.18 $\mu$ m CMOS	0.5 ~ 14	10.6	< 5.4	< -11	1.6	54*	Conventional DA	VLSI03 [11]
0.18 $\mu$ m CMOS	2.3 ~ 9.2	9.3	< 9.5	< -10	1.1	9*	Band-pass Chebychev match	ISSCC04 [12]
0.35 $\mu$ m SiGe BiCMOS	3.1 ~ 10.6	10	< 6.4	< -7	0.47	5.4	Modified low-power DA	RFIC05 [13]
0.25- $\mu$ m SOI SiGe HBT	3 ~ 10	22	< 3.9	< -2 / < -10	0.49	13.2	Resistive FB and CB	RFIC05 [14]
Advanced SiGe HBT	3 ~ 10	20	< 4.5	< -10 / < -8	0.52	42.5	Resistive FB	RFIC05 [15]
0.35 $\mu$ m SiGe BiCMOS	3.1 ~ 10.6 <sup>#</sup>	> 14.5	3.1 - 5.4	< -7 / < -10	0.74	10.8	Multi-section match, Darlington Cascode	This Work

+: Bias by off-chip Bias-T. \*: excluding power consumption of output stage for output matching.

#: defined by gain of better than 14.5 dB