V_{ds}. For $V_{gs} > 1.7$V, the characteristics exhibit an abrupt drop in drain current I_d at a voltage V_{ds2} in the forward sweep direction, and an abrupt increase in I_d at a voltage V_{ds1} in the reverse sweep. The switching voltages V_{ds1} and V_{ds2} differ, with $V_{ds2} > V_{ds1}$, leading to hysteresis in the drain characteristics. Also, V_{ds1} and V_{ds2} increase with V_{gs}. The transitions, referred to as switchup and switchdown, and the hysteresis result from the feedback loop from gate to source [1].

The drain characteristics of the BISFET were also measured for fixed V_{gs}, with a range of negative voltages V_{cs} applied to the collector. The results are shown in Fig. 2 for both the forward and reverse sweep directions, for $V_{gs} = 1.91$V and V_{cs} ranging from zero to –0.3V. The off-state trajectories in the two directions track each other closely. In the forward sweep, increasing the collector bias has two effects on the switchdown transition. First, it causes the off-state current to decrease, leading to an increase in the switching ratio to almost 2 from ~1.5. Secondly, it causes the transition to move to higher V_{ds}. In the reverse sweep, increasing the magnitude of the collector bias appears to have little effect on the switchup transition itself, though it reduces the off-state current.

The reduced off-state current results from an increase in the width of the depletion layer adjacent to the conduction channel in the active region as the magnitude of the collector bias is increased from zero. This leads to a reduction in carrier density in the channel in the off state, which in turn reduces the drain current, I_d. In the on state, increasing V_{cs} actually increases I_d, albeit slightly. This is a result of injection of electrons from the collector layer into the active region in the on state. These electrons flow into the channel and lead to an increase in I_d. They also turn the feedback loop on more forcefully. Thus, the on- and off-state currents move in opposite directions as V_{cs} is increased, leading to the significant improvement in the switching ratio. By comparison, increasing V_{gs} causes the currents in the two states to increase in tandem, so that any improvement in switching ratio is limited.

The electrons injected by the collector are also believed to be responsible for the shift of the transition to higher V_{ds}. The injection of additional current into the gate-source feedback loop makes it more difficult to turn off, so that higher drain voltage is required to make the device switch. A similar increase in V_{ds2} results from increasing V_{gs}. The lack of any significant effect on the switchup transition is a result of the general insensitivity of the transitions in the ohmic region of the characteristics [5].

The effect of V_{cs} on the hysteresis in the drain characteristics of the BISFET is illustrated in Fig. 3, which gives the full hysteresis loop for $V_{gs} = 1.91$V and $V_{cs} = 0$V and –0.3V. For comparison, the hysteresis loop is shown in the inset for two different values of V_{gs} and fixed $V_{cs} = 0$V to illustrate the effect of gate voltage. The hysteresis loop grows in size when either V_{gs} or V_{cs} is increased. However, a substantial vertical improvement results from the change in V_{cs} compared with that from increasing V_{gs}.

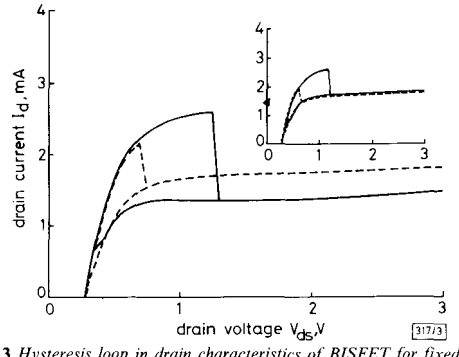

Fig. 3 *Hysteresis loop in drain characteristics of BISFET for fixed V_{gs} = 1.91V, with V_{cs} = 0 and –0.3V*

– – – – $V_{cs} = 0$V
——— $V_{cs} = -0.3$V
Inset: Hysteresis loop for fixed $V_{cs} = 0$V, with
– – – – $V_{gs} = 1.90$V
——— $V_{gs} = 1.93$V

The dramatic increase in the switching ratio resulting from application of a negative collector voltage suggests that the switching ratio could be improved by *designing* the device to have lower off-state current. This could be achieved by designing the threshold gate voltage to be closer to the threshold for bistability, so that little or no current flows when the device is in the off state. This is believed to be a very important result, as the prospect of a considerably-improved (perhaps even arbitrarily large) switching ratio dramatically enhances the potential of the BISFET in a wide range of practical applications.

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Piezoelectric field effect transistor (PEFET) using $In_{0.2}Ga_{0.8}As/Al_{0.35}Ga_{0.65}As/In_{0.2}Ga_{0.8}As/GaAs$ strained layer structure on (111)B GaAs substrate

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Indexing terms: Field effect transistors, Piezoelectric devices, 2-D electron gas

A novel electronic device using a two dimensional electron gas produced by the strain-induced electric field in a [111] growth-axis $In_{0.2}Ga_{0.8}As/Al_{0.35}Ga_{0.65}As/In_{0.2}Ga_{0.8}As/GaAs$ strained layer structure without modulation doping is reported. Two dimensional electron gas densities greater than 10^{11} cm^{-2} were observed both at room temperaure and 77°K. A field effect transistor using this strain-layer structure was fabricated successfully.

Introduction: Smith predicted [1] that large polarisation fields can be generated by the piezoelectric effect in strained-layer heterostructures made from zinc blende materials grown along the [111] axis. A strain-induced two-dimensional electron gas in a [111] growth-axis strained-layer structure was then proposed by Snow *et al.* [2]. They have shown that the induced polarisation charges can be used in field-effect transistor (FET) structures to produce large carrier densities without modulation doping. Later, an FET using the piezoelectric effect was fabricated by Li *et al.* [3]. However, in the Li devices, there was still a heavily doped region in the barrier layer and a GaAs cap layer was used. In this Letter, we report the results of a piezoelectric field effect transistor (PEFET) without any doped region in the AlGaAs barrier layer and an InGaAs cap layer instead of GaAs was used in our device structure so that the Snow theory could be applied and compared with the experimental data. Because no Si doped layer was used in the AlGaAs bar-

rier layer of the PEFET, DX related problems, such as the persistent photoconductivity effect, current-voltage (I-V) collapse phenomenon at low temperature etc., were not observed, which is the advantage of this novel device compared to the traditional modulation doped field effect transistor (MODFET).

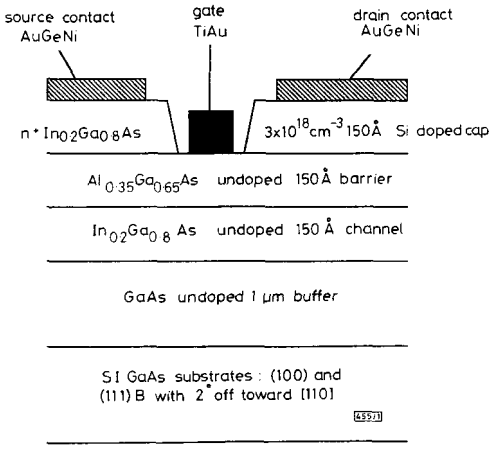

Fig. 1 *Schematic diagram of detailed layer structure and finished device of a piezoelectric field effect transistor (PEFET)*

Device technology: The schematic diagram of the detailed layer structure and the finished device of a piezoelectric field effect transistor (PEFET) is shown in Fig. 1. The device layer structure was grown by a VG semicon V-80H Mark II molecular beam epitaxy (MBE) machine. The strains, caused by the lattice mismatch between the thick GaAs buffer layer and the $In_{0.2}Ga_{0.8}As$ channel layer and the mismatch between the $Al_{0.35}Ga_{0.65}As$ barrier layer and the $In_{0.2}Ga_{0.8}As$ cap layer, are accommodated in the $In_{0.2}Ga_{0.8}As$ channel layer and the $In_{0.2}Ga_{0.8}As$ cap layer, respectively. That is, the strain-induced fields exist in the $In_{0.2}Ga_{0.8}As$ channel and the cap layers. Note that the heterostructure was grown on two different semi-insulating GaAs substrates for contrast: one is (100) oriented (sample A, the controlled sample) and the other is (111) oriented but with 2° off toward [110] (sample B). We found that many tiny pyramid-like structures formed on the epitaxial layer of the (111) substrate if the growth temperature was kept below 620°C. That is, a smooth surface could be obtained if the growth temperaure was higher than 620°C. Traditional mesa type and gate recess FET technologies were used to fabricate the devices. The gate length and width are 2 and 70μm, respectively. Hall data of the epitaxial layers and I-V characteristics of the devices were measured both at room temperature and at 77°K.

Table 1: Hall data for strained-layer heterostructures grown on GaAs substrates of different crystal orientations

Samples	Hall data at room temperature		Hall data at 77°K	
	Mobility	Electron density	Mobility	Electron density
	cm^2/Vs	$1/cm^2$	cm2/Vs	$1/cm^2$
Heterostructure on (100) substrate (sample A)	3800	6.5×10^{10}	10400	6.6×10^{10}
Heterostructure on (111) B substrate with 2° off toward [100] (sample B)	3800	3.4×10^{11} (2.7×10^{11})*	15700	2.1×10^{11}

* Number in parentheses is value calculated by the Snow equations in [2]

Results and discussion: The Hall mobilities and 2-D electron gas densities of the two samples at room temperature and 77°K are given in Table 1 for comparison. Note that the electron density

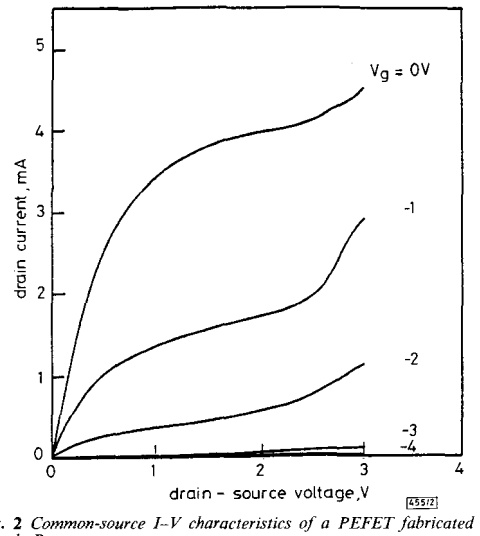

Fig. 2 *Common-source I–V characteristics of a PEFET fabricated on sample B*

(3.4×10^{11} cm^{-3}) of sample B at room temperature was very close to the theoretical prediction ($2.7 \times 10^{11}cm^{-3}$) by the Snow equations [2]. From Table 1, it is clear that the two dimensional (2-D) electron gas density of sample B is about 5 times and 3 times of that of sample A at room temperature and 77°K, respectively. That is, the 2-D electron gas density in the heterostructure grown on (111)B substrate with 2° off toward [110] (sample B) is greater than that in the heterostructure grown on (100) substrate (sample A). These results unequivocally demonstrate that large carrier densities are indeed induced by the piezoelectric field due to the internal strain produced by the $In_{0.2}Ga_{0.8}As/Al_{0.35}Ga_{0.65}As$ and $In_{0.2}Ga_{0.8}As/GaAs$ interfaces because there is no doping layer in the high bandgap $Al_{0.35}Ga_{0.65}As$ barrier layer. A field effect transistor was fabricated on sample B and the common-source current-voltage characteristics at room temperature are shown in Fig. 2. Excellent pinched-off characteristics was observed. Comparison of the I-V characteristics at different temperatures (77°K and room temperature) of another device are shown in Fig. 3. It is clear that the drain current was increased when the temperature was decreased from room temperature to 77°K and no current collapse was observed. This is in contrast with the normal behaviour of conventional high aluminum composition MODFETs at low temperature. This result means that no DX centre related problem exists in this device, which is reasonable because the $Al_{0.35}Ga_{0.65}As$ barrier layer is undoped.

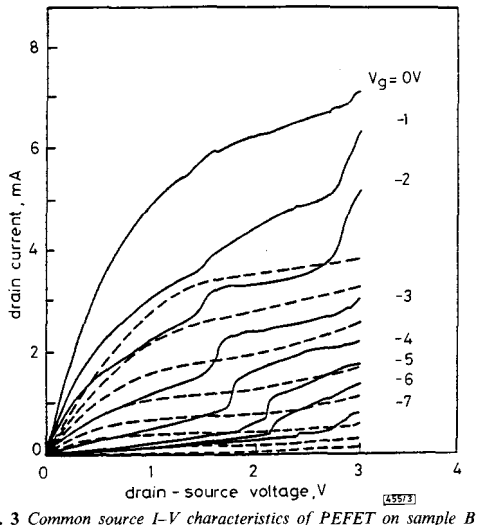

Fig. 3 *Common source I–V characteristics of PEFET on sample B at room temperature and 77°K*

Conclusions: A strain-induced 2-D electron gas due to the piezoelectric field effect in a strained heterostructure made from zinc blende materials grown along the [111] axis without any modulation doped layer is demonstrated. A piezoelectric field effect transistor (PEFET) was fabricated. It was also found that no DX centre related current collapse phenomenon was observed.

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Temperature dependence of current gains in high C-doped base HBTs

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Indexing terms: Heterojunction bipolar transistors, Electron-hole recombination

The temperature dependencies of current gain are investigated in both AlGaAs/GaAs and InGaP/GaAs HBTs. Various *Npn* HBT structures with high C-doped bases, grown by MOCVD, have been fabricated with identical processing steps. Measured results show that base bulk recombination current plays an important role in maintaining the current gain at high temperature. In addition it is shown that both space-charge and surface recombination currents are the cause of current gain reduction with temperature.

Introduction: AlGaAs/GaAs HBTs are the most widely investigated and have demonstrated excellent device and circuit performance. However, this structure has many well-known disadvantages. An alternative is the aluminium-free InGaP/GaAs HBT which has recently attracted considerable attention due to the favourable energy band line-up and the selective etching properties [1]. Recently we reported high C-doped base InGaP/GaAs HBTs with improved characteristics showing current gain greater than unity at very low collector current [2, 3]. We also reported the temperature dependence of current gain in InGaP/GaAs and AlGaAs/GaAs HBTs and showed that the former device exhibits near constant current gain with temperature in the range 300–600K [2]. There has also been a recent report [4] on the temperature dependence of current gain in InGaP/GaAs and a comparison of this with abrupt AlGaAs/GaAs HBTs. These results agree with our previous findings. The data in [4] have been explained by considering the emitter injection efficiency. However, our results presented in this Letter cannot be explained by just considering the emitter injection efficiency. In general the emitter injection efficiency for an abrupt emitter-base junction is exponentially proportional to the valence band offset (ΔW_v), whereas for a graded HBT this is exponentially proportional to the emitter and base bandgap difference (ΔW_g). A graded AlGaAs/GaAs HBT has similar ΔW_g compared with the ΔW_v of an InGaP/GaAs HBT. Thus we would expect a constant current gain with temperature for a graded AlGaAs/GaAs HBT as obtained for InGaP/GaAs HBTs. In this Letter, we show experimentally that base bulk, space-charge and surface recombination currents also have a significant effect in controlling the gain of HBTs with temperature and present an explanation for the insensitivity of the current gain with temperature.

Experimental details: Large geometry HBT devices were fabricated on materials grown by MOCVD at Epitaxial Products International Ltd. The layer structure and processing technology for both graded $Al_{0.3}GaAs_{0.7}$/GaAs and $In_{0.5}Ga_{0.5}P$/GaAs HBTs have been reported earlier [3]. The fabricated devices have the same geometry and fabrication steps. The DC characteristics were measured using an HP4145B semiconductor parameter analyser in conjunction with a computer controlled system for data analysis.

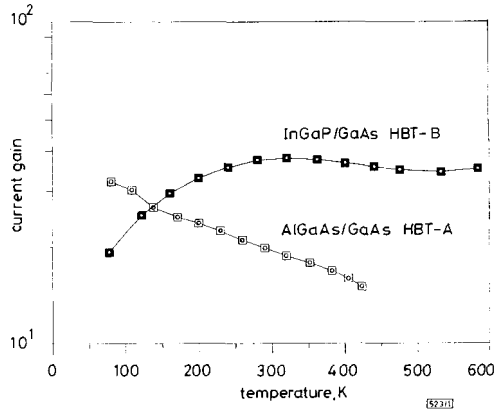

Fig. 1 *Temperature dependence of current gain for InGaP/GaAs and AlGaAs/GaAs HBTs measured at $V_{ce} = 3V$ and $I_c = 100mA$*

Emitter diameter of transistor is 100μm

Results and discussion: Typical variation of current gain β with temperature for InGaP/GaAs and AlGaAs/GaAs HBTS is shown in Fig. 1. It is seen from this Figure that the current gain of the InGaP/GaAs HBT increases with increasing temperature and remains relatively constant over the temperature range 300–600K, while for the AlGaAs/GaAs HBT the gain reduces continuously with increasing temperature. At low temperature the decrease of current gain with reducing temperature for the InGaP/GaAs HBT is due to the reduction of base minority carrier lifetime [5]. To investigate the mechanisms causing gain variations with temperature, we have investigated several C-doped base HBTs having different base recombination currents. The normalised current gains as a function of temperature are plotted and these are given in Fig. 2. The base structure and ideality factors for each device are shown in Table 1. For comparison, the data for the InGaP/GaAs HBT are also included.

Table 1 Base structures and emitter/base ideality factors for the devices shown in Fig. 2

Devices	Emitter type	Base doping	Base thickness	Base ideality factor
		cm^{-3}	Å	
A	$Al_{0.3}Ga_{0.7}As$	1×10^{19}	1200	2.1
EET-A	$Al_{0.3}Ga_{0.7}As$	1×10^{19}	1200	2.4
B	$In_{0.5}Ga_{0.5}P$	3×10^{19}	800	1.1
C	$Al_{0.3}Ga_{0.7}As$	2×10^{19}	900	1.2

We have found that the collector ideality factors in these devices were near unity whereas the base ideality factors varied. We also note that above room temperature the base ideality factors remained fairly constant with temperature, suggesting that the same base recombination current is dominating throughout the temperature range measured.