Composite Effects of Reflections and Ground Bounce for Signal Line through a Split Power Plane

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Abstract

The signal propagating along a microstrip line over a slot on the power plane will suffer from composite effects of reflected noise by a discontinuity in signal return path and ground bounce between power/ground planes. A new equivalent circuit model is proposed and simulations are performed for a three-layer structure to characterize ground bounce coupling.

1 Introduction

In a multi-layer printed circuit board (PCB) or multi-chip module (MCM), it is common practice to cut a slot in ground or power plane. For example, cutting a power plane into several areas provides multiple power distribution. Another is an isolated power or ground plane area, called island, to isolate a noisy or sensitive circuit from other circuits. However, signal lines have to cross the slots in order to communicate between different areas. Hence incurred are two major signal integrity concerns; the reflection due to the discontinuity in signal return path and the ground bounce which is the voltage fluctuations between power and ground planes.

Traditionally considered to be mainly due to the electric current along vias, the ground bounce can be caused as well by the equivalent magnetic current flowing through the slot on the power or ground planes. As ground bounce noise generated either by other vias or slots in power/ground planes propagate across the slots, it will in turn induce noise voltage on slot and then couple into signal lines. To accurately model the propagation characteristics of signal traces over slot, the composite effects of signal reflection and ground bounce must be taken into account in view of the increasing complexity of the routing and the necessity of multiple power distribution.

The isolation of island has been discussed using the three-dimensional finite-difference time-domain (FDTD) method [1], but signal lines are not included and this method need long computation time and large computer memory. In another point of view, the microstrip/slot coupled has been discussed using transmission line model and mode conversion [2], but neglecting the presence of ground bounce between power and ground planes. This paper proposed a new efficient analysis scheme which consists of the two-dimensional FDTD method for the propagation of ground bounce, the transmission line theory for the signal propagation along microstrip and slot line, and especially, an equivalent circuit for the coupling between the ground bounce and signals along the slot. The 2D FDTD and transmission line simulations can be performed separately and linked together at each computation time step. The effects of the slot on signal propagation are thus characterized.

2 Theory and Circuit Modelling

Consider a multi-layer structure shown in Fig. 1 in which the power plane is cut with a finite slot. The whole structure can be divided into two parts, region 1: the microstrip line and slotline, and region 2: the parallel plates with a split on one plane. Since the separation between two metal planes is typically much smaller than the wavelength and the size of the planes, the fields between the two metal planes can be assumed to be uniform along the vertical direction. Consequently, the electromagnetic fields between

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two metal planes are two-dimensional and consist of E_z, H_x, and H_y only. They can be solved by the two-dimensional FDTD method.

Microstrip line and slotline can be modelled as transmission lines. Given the propagation constant and characteristic impedance, they are approximated by equivalent LC ladder circuits and the signal propagation is simulated by telegrapher's equation using central difference discretization. Without loss of generosity, assume that the slotline is positioned along $x = (i_0 + \frac{1}{2})\Delta x$ while the microstrip line is along $y = j_0 \Delta y$.

At region 1, the equivalent circuit at the cross section of microstrip line and slotline is similar to that described in [2], as shown in Fig. 2, i.e.,

$$\begin{cases} C_{\mu\text{strip}} \Delta x \dfrac{\partial}{\partial t} V_{\mu\text{strip}}(i\Delta x, t) = I_{\mu\text{strip}}((i - \frac{1}{2})\Delta x, t) - I_{\mu\text{strip}}((i + \frac{1}{2})\Delta x, t) & \text{(1a)} \\ L_{\mu\text{strip}} \Delta x \dfrac{\partial}{\partial t} I_{\mu\text{strip}}((i + \frac{1}{2})\Delta x, t) = V_{\mu\text{strip}}(i\Delta x, t) - V_{\mu\text{strip}}((i+1)\Delta x, t) - V_{\text{slot}}(j_0 \Delta \mathrm{y}, \mathrm{t})\delta_{i,i_0} & \text{(1b)} \end{cases}$$

Under the consideration of ground bounce coupling, the telegrapher's equation for slotline can be written as

$$\begin{cases} C_{\text{slot}} \Delta y \dfrac{\partial}{\partial t} V_{\text{slot}}(j\Delta y, t) \cong -H_y((i_0 + \frac{1}{2})\Delta x, j\Delta y, t)\Delta y - I_{\text{slot}}((j + \frac{1}{2})\Delta y, t) + I_{\text{slot}}((j - \frac{1}{2})\Delta y, t) & \\ \qquad\qquad + I_{\mu\text{strip}}(i_0 \Delta x, t)\delta_{j,j_0} & \text{(2a)} \\ L_{\text{slot}} \Delta y \dfrac{\partial}{\partial t} I_{\text{slot}}((j + \frac{1}{2})\Delta y, t) = V_{\text{slot}}(j\Delta y, t) - V_{\text{slot}}((j+1)\Delta y, t) & \text{(2b)} \end{cases}$$

Here, L_{slot} and C_{slot} are the per-unit-length inductance and capacitance of slotline in the presence of power/ground planes, I_{slot} and V_{slot} are the current and voltage on slotline, and H_y is the magnetic field in y direction under slotline in the power/ground planes. Similar definitions hold for $L_{\mu\text{strip}}$, $C_{\mu\text{strip}}$, $I_{\mu\text{strip}}$, and $V_{\mu\text{strip}}$.

At region 2, the FDTD mesh inclusive of slotline is shown in Fig. 3. The voltage on slotline will couple into power/ground plane so that the updating for magnetic field in y direction must be rewritten as

$$\mu \frac{\partial}{\partial t} H_y((i + \tfrac{1}{2})\Delta x, j\Delta y, t)\Delta x \cdot d = [E_z((i+1)\Delta x, j\Delta y, t) - E_z(i\Delta x, j\Delta y, t)]d + V_{\text{slot}}(j\Delta y, t)\delta_{i,i_0} \quad (3)$$

The time marching can be briefly described as follows. The voltages $V_{\mu\text{strip}}$ and V_{slot} can be updated from $I_{\mu\text{strip}}$, I_{slot}, and H_y by (1a) and (2a). In the next half time step, $I_{\mu\text{strip}}$, I_{slot}, and H_y can be updated from $V_{\mu\text{strip}}$, V_{slot}, and E_z with the help of (1b), (2b), and (3). Hence, the coupled effects between slotline and power/ground planes is addressed. The composite effects of reflection and ground bounce among the whole structure can be modelled.

3 Simulation Results

Take the structure of a 10cm x 10cm PCB shown in Fig. 1 as an example,. The heights of signal layer and power/ground planes are 635 μm and 150 μm, respectively, and the dielectric constant is both 9.7. The widths of microstrip line and slotline are 570 μm and 50 μm, respectively, and the length of slotline is 4cm. The signal voltage source is a Gaussian pulse generator in series with an internal resistance of 50ohm. On the other end of the signal line is connected a matched load. The top view of Fig. 1 is shown in Fig. 4.

The voltages at points A and B are monitored and the waveforms are shown in Fig. 5(a), while the voltages at points a, b, and c in Fig 5(b) and the ground bounce beneath slotline in Fig. 5(c). In Fig. 5(b), as the voltage propagates along the slot, it decays continually due to the energy coupling onto power/ground planes. At late time, the ground bounce that reflected by edge couples into slotline and then causes small noise on microstrip line as shown in Fig. 5(a). Now, the separation of power/ground planes is changed to 300 μm and 500 μm and voltage at point A are shown in Fig. 6. As the separation increases, energy coupled into power/ground planes will decrease and the noise on microstrip line will increase.

4 Conclusions

In this paper, a new model is proposed to simulate a signal line flowing above a split power or ground plane. Although ground bounce caused by slot coupling is only 5% of input signal, the effects can not be ignored as multi-trace signal flows through the slot simultaneously.

References

[1] Daniel De Zutter, "The FDTD-method for EMC-problems with application to electrostatic discharge and delta-I noise calculations", *IEEE International Symposium on Electromagnetic Compatibility*, 1997, pp. 226 -230.

[2] H. J. Liaw and H. Merkelo, "Signal integrity issues at split ground and power planes," *Proceedings of 46th IEEE Electronic Components and Technology Conference,* 1996, pp. 752 -755.

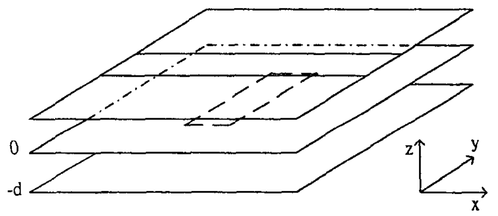

Fig. 1 A simple a multi-layer structure with split power plane.

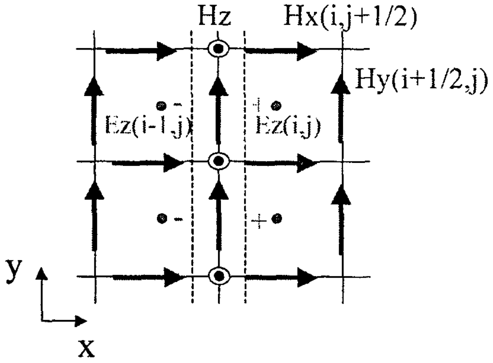

Fig. 3 FDTD mesh inclusive of slotline

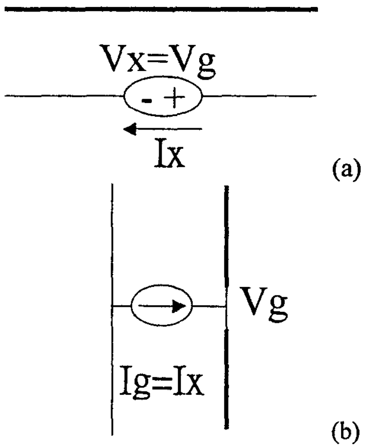

Fig. 2 Equivalent circuit at cross section of microstrip line and slotline.

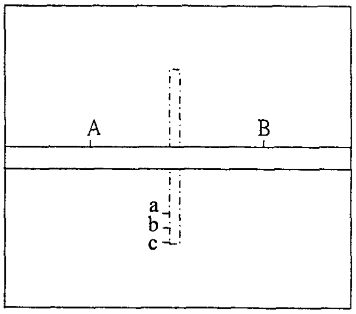

Fig. 4 Top view of Fig. 1

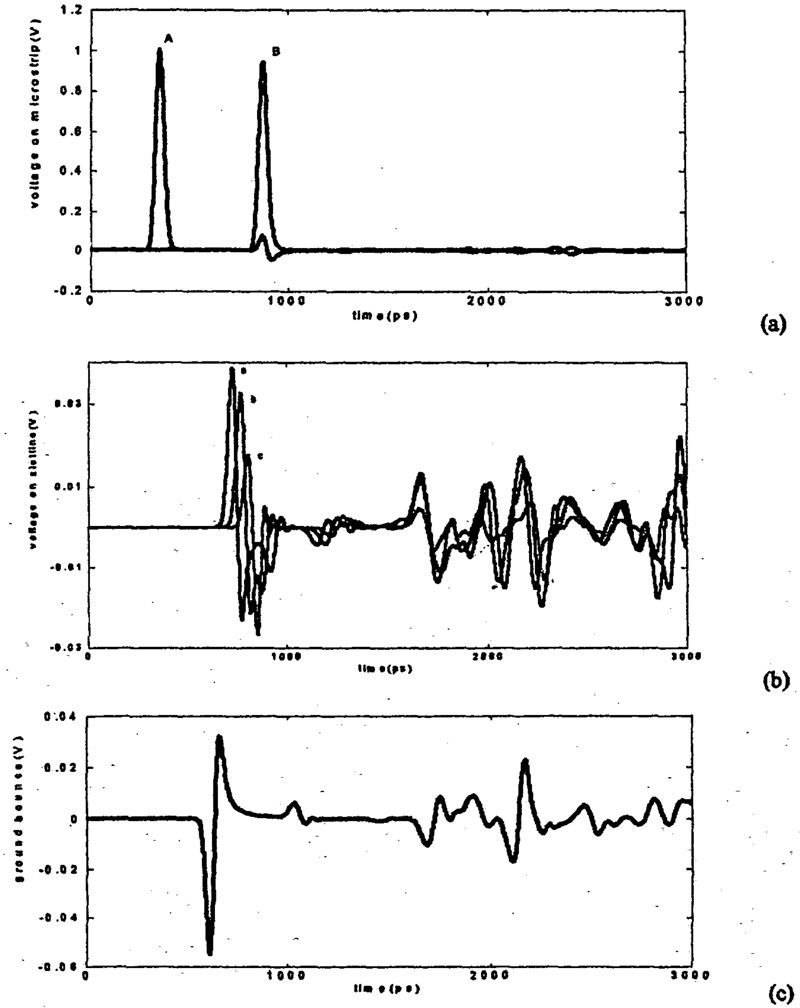

Fig. 5(a) Voltages at A, B, (b) voltages at a ,b, c, and (c) ground bounce near slotline

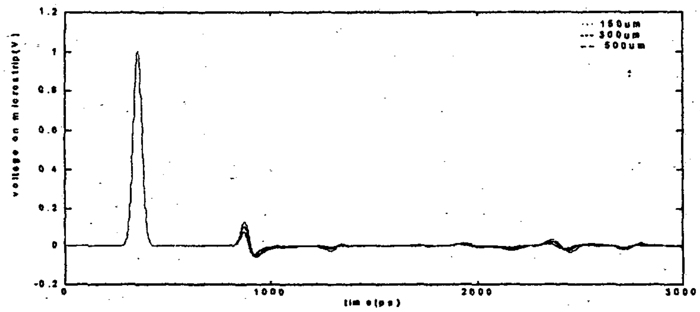

Fig. 6 Comparison of voltage at A with different separation of power/ground planes.