Selective Metal Parallel Shunting Inductor and Its VCO Application

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Abstract

For a planar inductor, the maximal quality factor, Q_{max}, is located at the specified frequency, f_{Qmax}. In this paper, a method called selective metal parallel shunting (SMPS) is proposed to move f_{Qmax} onto the desired frequency without additional processing steps. For a given planar inductor, a customized program is developed to find all the possible SMPS inductors and predict their Q_{max} and f_{Qmax}. Three sets of planar, all metal parallel shunting (AMPS), and SMPS inductors have been implemented in a 1P4M 0.35μm CMOS process to verify the proposed method. The prediction errors of Q_{max} and f_{Qmax} are less than 13% and 10%, respectively, between the simulated and measured ones. Moreover, three 2.3-2.4GHz VCOs using planar, AMPS, and SMPS inductors, respectively, have also been realized. The phase noise of the VCO using SMPS inductors can be improved by 9.3dB and 6dB, respectively, compared to the VCOs using planar and AMPS inductors at 100KHz offset frequency. The figure-of-merit (FOM) performance of the VCO using SMPS inductors can be comparable to the state-of-the-art publications.

I. Introduction

Monolithic inductors have been widely used in many RF circuits such low-noise amplifier, voltage-controlled oscillator, and power amplifier. Although they suffer from the poor quality factor on the lossy silicon substrate, the mainstream still focuses on integrating the monolithic inductor to achieve the minimal external component.

Until now there are many methodologies have been proposed to improve the low quality factor problem. They have included higher conductivity metal layers to reduce the metal loss, highly resistive substrates to reduce the substrate loss, thick oxide layer to separate the inductor from the substrate, etching away the lossy substrate below the inductor, etc. Since these approaches are primarily of process improvement and post-process steps [1], it will increase fabrication cost.

By selecting different metal layers to parallel each turn in a given planar inductor, one can move f_{Qmax} onto the desired frequency with no additional process steps. Applying this method to optimizing the spiral inductors in a VCO, the phase noise performance of the VCO using SMPS inductors can be improved by 9.3dB and 6dB, compared to that of VCOs using planar and AMPS inductors, respectively, at 100kHz offset frequency.

II. How to Move f_{Qmax} Onto the Desired Frequency

A. *Basic Behavioral Description*

The monolithic spiral inductor can be regarded as wounded transmission lines. Including the losses in the conductors and in the dielectric material, the transmission line can be modeled as Fig. 1.

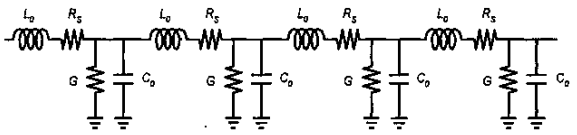

Fig. 1 Model of a lossy transmission line.

Thus the characteristic impedance can be expressed as

$$Z_0 = \sqrt{\frac{j\omega L_0 + R_S}{j\omega C_0 + G}} = \alpha + j\beta \quad (1)$$

, where α and β denote attenuation factor and phase constant, respectively. The signal propagation in the lossy transmission line can be shown as

$$V(t,x) = V_0 \exp(-\alpha x)\cos(\frac{2\pi}{T}t - \beta x) \quad (2)$$

, where α and β can be expressed as

$$\alpha \approx \frac{1}{2}(R_S\sqrt{\frac{C_0}{L_0}} + G\sqrt{\frac{L_0}{C_0}}), \quad \beta \approx \omega\sqrt{L_0 C_0} \quad (3)$$

The above equation can be abbreviated as

$$V(x) = V_0 \exp(-\alpha x)\exp(-j\beta x) \quad (4)$$

, where the time dependence is not shown and only the real part of $V(x)$ is of our concern in our calculations. In reality, the total length of an inductor is about several hundred microns, $\alpha \sim 0.0496\text{mm}^{-1}$ and $\beta \sim 10^{-4}$, i.e., $\alpha x \ll 1$, and $\beta x \to 0$. Therefore, eq. (4) can be approximated as

$$V(x) = V_0 \cdot (1 - \alpha x) \quad (5)$$

That is why the inductor's voltage profile can be linear [2].

B. *Voltage Profile of Monolithic Inductors*

Suppose that a planar inductor has inner radius r, metal width w, and n turns in the m-th metal layer. First, the lengths of each turn are defined as l_1, $l_2 \ldots l_n$, respectively, and the total length is defined as $l_{tot}=l_1+l_2+\ldots+l_n$. Each track area is defined as A_1, $A_2 \ldots A_n$, respectively, from 1st turn to n-th one. For each track, the DC resistance can be calculated as $R_k=R_{unit}*l_k/w$, thus $R_{tot}= R_1 + R_2 +\ldots+ R_n$.

From eqs. (3) and (5), the beginning voltage $V(k)_{beg}$ and the ending voltage $V(k)_{end}$ of the k-th turn in an inductor can be expressed as

$$V(k)_{beg} = V_0(1 - (r_1 + r_2 + \ldots + r_{k-1})) \quad (6)$$

$$V(k)_{end} = V_0(1 - (r_1 + r_2 + \ldots + r_{k-1} + r_k)) \quad (7)$$

, where $r_k \equiv (R_k / R_{tot})$. The voltage of the k-th turn in the m-th metal layer can be averaged as

$$V(k) = \frac{1}{2}[V(k)_{beg} + V(k)_{end}] = \frac{1}{2}V_0[2 - d(k-1) - d(k)] \quad (8)$$

,where $d(k) \equiv r_1 + r_2 + ... + r_{k-1} + r_k$. As described by eq. (8), the voltage profile of a planar inductor without metal parallel shunting is linear as shown in Fig. 2. For an SMPS inductor, every metal track in top layer can be selectively shunted with lower metal layers, the voltage profile can be piecewise linear as shown in Fig. 3.

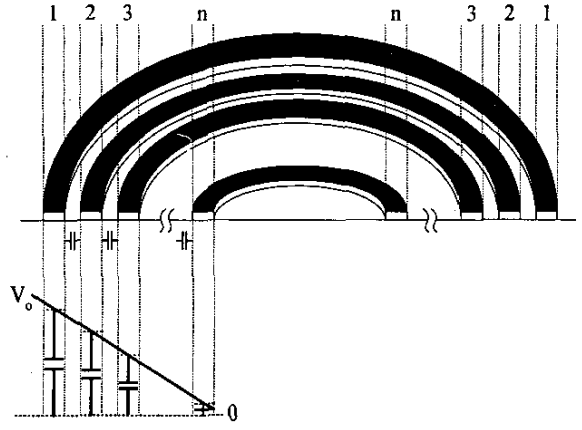

Fig. 2 Voltage profile of the n-turn planar inductor.

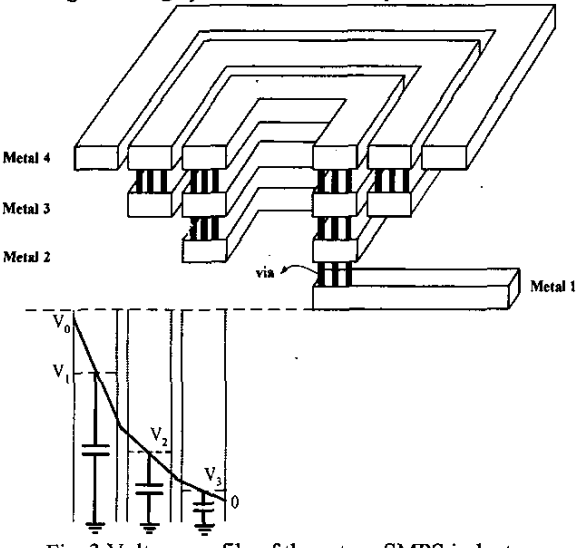

Fig. 3 Voltage profile of the n-turn SMPS inductor.

The electrical energy stored in the equivalent capacitors of the inductor is simply divided into two parts: one is in metal-to-metal capacitors and the other is in metal-to-substrate capacitors, and it can be derived as

$$\begin{aligned} E_{c,total} &= \frac{1}{2} C_p V_0^2 + \frac{1}{2} C_{sub} V_0^2 \\ &= E_{c,metal-metal} + E_{c,metal-sub} \\ &= \sum_{k=1}^{n-1} E_{c,mm}(k) + \sum_{k=1}^{n} E_{c,ms}(k) \end{aligned} \quad (9)$$

Based on eq. (9), the equivalent capacitance, C_p and C_{sub}, of an inductor can finally be expressed as

$$\begin{aligned} C_p &= \sum_{k=1}^{n-1} \frac{1}{4} C_{mm} t_k [d(k+1) - d(k-1)]^2 \\ C_{sub} &= \sum_{k=1}^{n} \frac{1}{4} C_{ms} A_k [2 - d(k-1) - d(k)]^2 \end{aligned} \quad (10)$$

For different metal shunting configurations, the voltage profile will be different, thus their equivalent capacitance and DC resistance will be different. Table I lists the properties of different metal shunting configuration in a 0.35μm 1P4M CMOS process. Metal parallel shunting does not change the unit inductance or dielectric conductance very much but DC resistances and equivalent capacitances will change for different configurations. The mechanism to move f_{Qmax} onto the desired frequency can be illustrated as Fig. 4. By appropriately selecting metal parallel shunting to modify DC resistance and equivalent capacitances, one can move f_{Qmax} onto the desired frequency and make Q maximized at the desired frequency. By fully understanding the modification of voltage profile, a customized program is developed to predict f_{Qmax} and Q_{max} of all possibe configurations.

TABLE I.
Properties of Different Metal Shunting Configurations in TSMC 0.35μm 1P4M CMOS Process

Configuration	R_{unit} (Ω)	C_{unit} (fF)
M4	0.05	6.3
M43 (parallel M4 and M3)	0.031	8.4
M432 (parallel M4, M3 and M2)	0.022	13.3

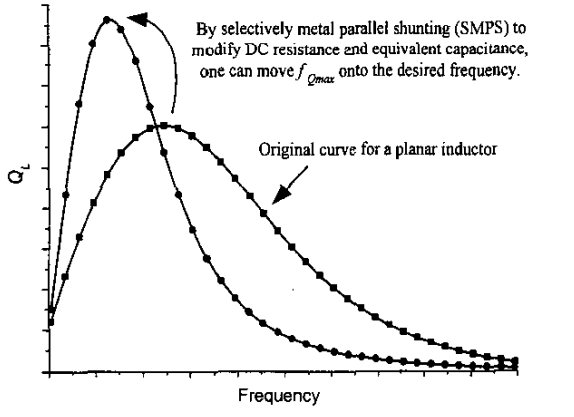

Fig. 4 Illustration of the mechanism to move f_{Qmax} onto the desired frequency.

III. Experimental Results

A prototype chip including three sets of planar, SMPS and AMPS inductors, and three VCOs have been implemented in a 0.35μm 1P4M CMOS process as shown in Fig. 5. The S parameters were measured by Network Analyzer HP8510C and Cascade Microtech Probe Station using coplanar ground-signal-ground probes.

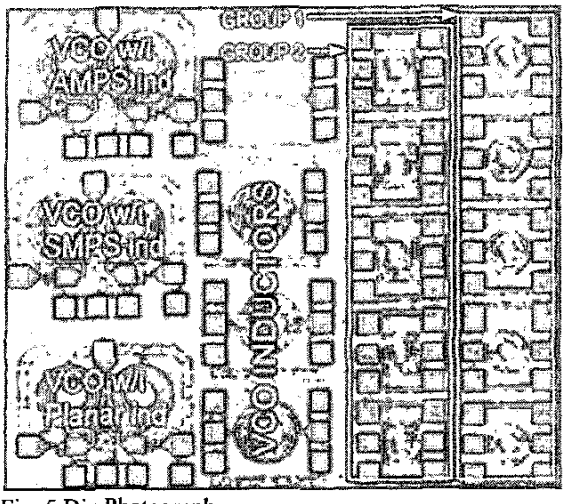

Fig. 5 Die Photograph.

Table II lists the measured f_{Qmax}s and Q_{max}s of the inductors in Group1 and Group2 and simulated ones by the developed program. The prediction errors of f_{Qmax} and Q_{max} are less than 13% and 10%, respectively. The inductors' geometric sizes for every 4-turn inductor are r=50um, w=10um, *spacing*=1um, and r=70um, w=10um, *spacing*=1um in Group1 and Group2, respectively. Fig. 6 shows the measured Qs of the inductors in Group1, and Fig. 7 shows the measured ones in Group2. The experimental results demonstrate that the f_{Qmax} in Group1 can be moved from 4.4GHz to 2.6GHz by the proposed method, and the f_{Qmax} in Group2 can be moved from 3.5GHz to 2.1GHz.

IV. Circuit Application: VCO

Phase noise in an *LC*-tank oscillator can be expressed as the Leeson-Culter equation:

$$L(\Delta\omega) = 10 \cdot \log\left[\frac{1}{2}\cdot\frac{FkT}{P_2}\cdot\left\{1+\left(\frac{\omega_0}{2Q\Delta\omega}\right)\right\}^2\left(1+\frac{\Delta\omega_{1/f^3}}{|\Delta\omega|}\right)\right] \quad (13)$$

, where F is an empirical factor, ω_0 is the oscillation frequency, $\Delta\omega$ is the offset frequency, and Q is the quality factor of the tank. To improve the phase noise, the tank Q should be large as possible at the operating frequency. Since higher Q yields the larger swing amplitude in the same bias, it can introduce the quadratic improvement for phase noises. However, in a fully integrated oscillator, the tank Q is limited by inductor's poor quality factor Q_L.

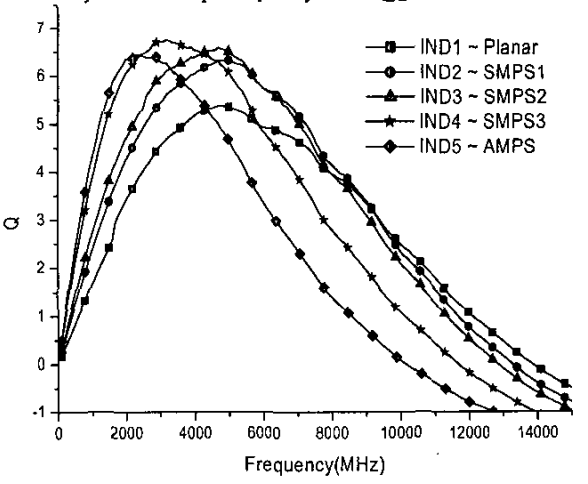

Fig. 6 Measured Qs for the Inductors in Group 1.

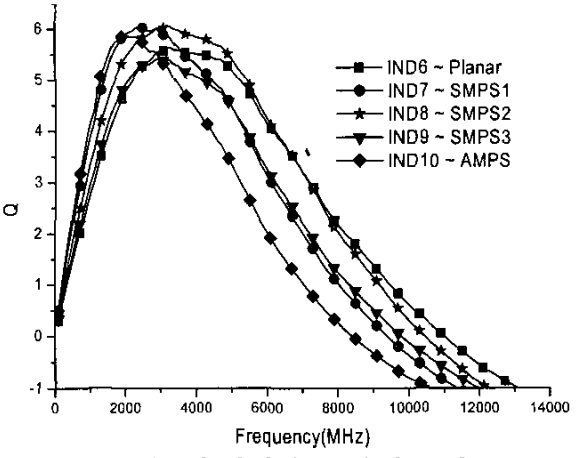

Fig. 7 Measured Qs for the Inductors in Group 2.

TABLE II. Simulated and Measured f_{Qmax}s and Q_{max}s of inductors in a 0.35μm 1P4M CMOS process

Group	Name	Configuration (from the outmost turn to the innermost turn)	L(nH)	Sim. f_{Qmax} (GHz)	Mea. f_{Qmax} (GHz)	f_{Qmax} Error	Sim. Q_{max}	Mea. Q_{max}	Q_{max} Error
1	IND1	M4→M4→M4→M4	4.0	4.4	4.7	6.4%	5.7	5.36	6.3%
1	IND2	M4→M4→M43→M432	3.9	4.2	4.6	8.6%	6.6	6.31	4.6%
1	IND3	M4→M43→M43→M432	3.8	4.0	4.5	11.1%	6.9	6.58	4.8%
1	IND4	M43→M43→M432→M432	3.8	3.3	3.2	3.1%	7.4	6.75	9.6%
1	IND5	M432→M432→M432→M432	3.7	2.6	2.4	8.3%	7.0	6.45	8.5%
2	IND6	M4→M4→M4→M4	4.5	3.5	3.3	6.1%	5.2	5.62	7.5%
2	IND7	M43→M432→M432→M432	4.4	2.5	2.7	7.4%	6.2	5.90	5.1%
2	IND8	M4→M43→M432→M432	4.4	3.2	2.9	10.3%	5.9	6.10	3.3%
2	IND9	M43→M43→M43→M43	4.4	2.8	3.2	12.5%	5.8	5.39	7.4%
2	IND10	M432→M432→M432→M432	4.3	2.1	2.0	5%	6.1	5.85	4.1%

Utilizing the proposed methodology and the developed program, the on-chip inductor used in a VCO is optimized and make f_{Qmax} at the operating frequency to improve phase noise. The measured Q_L of three kinds of inductors is shown in Fig. 8, and it demonstrates that f_{Qmax} can be moved onto 2.3GHz from 3.4GHz, and Q is maximized to 7.4 from 5.3.

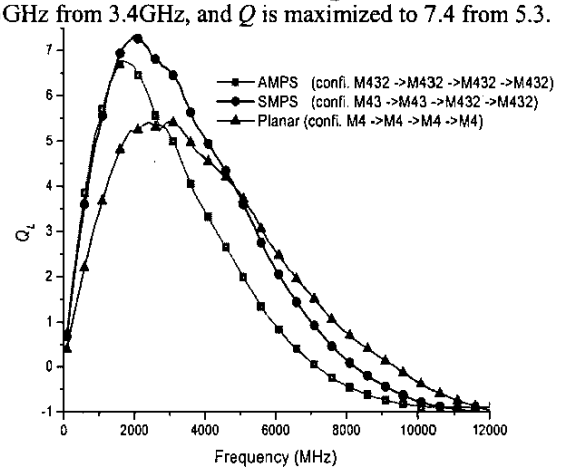

Fig. 8 Measured Q_L in a VCO with Planar, SMPS, and AMPS Inductors.

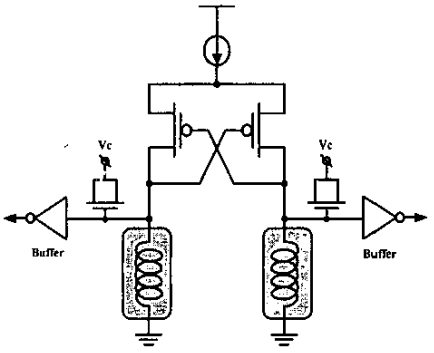

Fig. 9 The Simplified Schematic of the VCO Using Planar, SMPS, and AMPS Inductors.

An LC VCO in Fig. 9 is designed to oscillate at 2.3-2.4GHz. It utilizes PMOS as a cross-coupled pair, and A-mode varactors. The open-drain output buffers are used for measurements. The tank draws 3.2mA from a 3.3V supply voltage. The measured output phase noises of the VCOs are shown in Fig. 10 by Agilent E5500 Phase Noise Measurement System. The measured phase noise performance at 100kHz offset frequency of the three VCOs are -92dBc/Hz, -95.3dBc/Hz, and -101.3dBc/Hz, respectively, with the same power consumption. The phase noise performance of the VCO using the SMPS inductor can be improved by 9.3dB and 6dB compared to that of VCOs using planar and AMPS inductors, respectively. Table III shows the comparison between the VCO using SMPS inductors and the state-of-the-art publications. After the inductors' modification, the FOM of the VCO using SMPS inductors can be comparable to the state-of-the-art publications.

V. Conclusion

In this paper, a selective metal parallel shunting method is proposed to move f_{Qmax} onto the desired frequency. The method does not need any additional processing steps. Applying the method to optimize VCO's inductors, the measured phase noise can be improved by 9.3dB and 6dB compared to VCOs using planar and AMPS inductors, respectively. The FOM of VCO after inductor optimization can be comparable to the state-of-the-art publications. The method can not only be applicable to VCO but also other RF circuits, such as LNA and PA, etc.

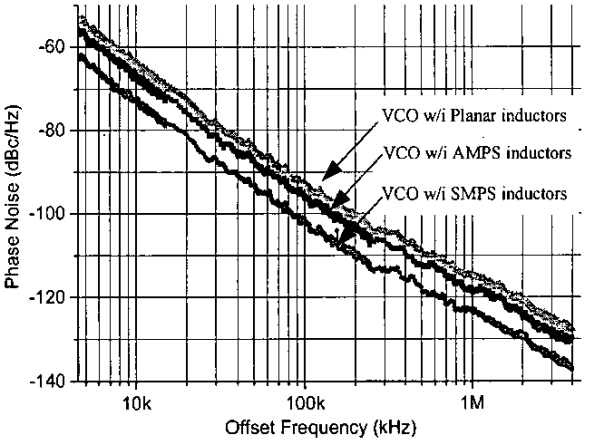

Fig. 10 The Measured Phase Noises of the VCOs.

Table III
Comparison with the state-of-the-art publication (f_o: GHz, P_d: mW)

Reference	Process	f_o	P_d	Phase noise	FOM
B. Razavi ISSCC'97	CMOS	1.8	7.6	-100dBc/Hz @500kHz	162.3
M. Zannoth ISSCC'98	Bipolar	1.96	32.4	-102dBc/Hz @100kHz	172.4
P. van de Ven VLSI'2001	BiCmos	4.9	21	-85dBc/Hz @100kHz	168
C. Samori CICC'2001	CMOS	5	13.7	-94dBc/Hz @100kHz	176.6
M. Straayer ISSCC'2002	BiCmos	1.7	11.3	-117dBc/Hz @100kHz	177.4
R. Aparicio ISSCC'2002	BiCmos	1.8	10	-102dBc/Hz @100kHz	177.1
P. Andreani ISSCC'2002	CMOS	1.8	25	-107dBc/Hz @100kHz	178.2
This Work VCO(SMPS)	**CMOS**	**2.34**	**10.5**	**-101dBc/Hz @100kHz**	**178.4**

VI. References

[1]. C. P. Yue, and S. S. Wong, "On-Chip Spiral Inductors with Patterned Ground Shields for Si-Based RF IC's," *IEEE J. Solid-State Circuits*, vol. 33, no. 51, pp. 743-752, May 1998.

[2]. A. Zolfaghari, A. Chan, and B. Razavi, "Stacked Inductors and Transformers in CMOS Technology," *IEEE J. Solid-State Circuits*, vol. 36, no. 4, pp. 620-628, Apr. 2001.