A Wide-range and Fixed Latency of One Clock Cycle Delay-Locked Loop

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ABSTRACT

A wide-range delay-locked loop (DLL) with a fixed latency of one clock cycle is proposed. The phase selection circuit and the start-controlled circuit are used for this DLL to enlarge the operating frequency range and eliminate the harmonic locking problems. The operating frequency range of the DLL can be from $1/T_{Dmin}$ to $1/(N \times T_{Dmax})$, where T_{Dmin} and T_{Dmax} are the minimum and maximum delay of a delay cell, respectively, and N is the number of delay cells used in the delay line theoretically. The prototype chip is fabricated in a 0.35-um 1P3M CMOS process. The measurement results exhibit the proposed DLL can operate from 6 MHz to 130 MHz and the latency of this DLL is just one clock cycle. From the entire operating frequency range, the maximum rms jitter doesn't exceed 25 ps. The DLL occupies an active area of 880-um×515-um and consumes a maximum power of 132 mW at 130 MHz.

1. INTRODUCTION

The continuing scaling of CMOS technologies has led to an exponential growth of the speed and integration levels of digital IC's. However, the synchronization problem between IC modules is undoubtedly important and becomes one of the bottlenecks for high performance systems.

Phase-locked loops (PLLs) [1] and Delay-locked loops (DLLs) [2-3] have been typically employed for the purpose of synchronization. Due to the difference of their configuration, the DLLs are preferred for their unconditional stability and faster locking time than PLLs. Additionally, a DLL offers better jitter performance than a PLL because noise in the voltage-controlled delay line (VCDL) does not accumulate over many clock cycles.

Conventional DLLs, as shown in Fig. 1, may suffer from harmonic locking over wide operating range. If the DLLs want to operate at lower frequency without harmonic locking, the number of delay stages must be increased to let the maximum delay of the delay line equal to the period of the lowest frequency. However, the maximum operating frequency of a DLL will be limited by the minimum delay of the delay line.

If the delay different from an integer of clock periods is detected, the closed loop will automatically correct it by changing the delay time of the VCDL. However, the conventional DLL will fail to lock or falsely lock to two or more periods, T_{clk}, of the input signal if the initial delay of the VCDL is shorter than 0.5 T_{clk} or longer than 1.5 T_{clk} as shown in Fig. 2. Therefore, if the DLL is desired to lock a delay which it is just one clock cycle of input reference signal, the initial delay of VCDL needs to be located between 0.5 T_{ref} and 1.5 T_{ref} no matter what the initial voltage of the loop filter is. If the maximum and minimum delay of the VCDL are T_{VCDL_max} and T_{VCDL_min}, respectively. As a result, the period of input signal should satisfy the following inequality [4]:

$$\text{Max}\left(T_{VCDL\_min},\ 2/3 \times T_{VCDL\_max}\right) < T_{CLK} < \text{Min}\left(T_{VCDL\_max},\ 2 \times T_{VCDL\_min}\right) \quad (1)$$

However, if T_{VCDL_max} ?3×T_{VCDL_min}, there is no range of T_{CLK} that can satisfy eq. (1) and the DLL is prone to the false locking problem. It is difficult to design a VCDL in which T_{VCDL_max} is just equal to 2×T_{VCDL_min} when process variations are taken into account. Thus, some solutions [4]~[8] have been proposed to overcome this problem.

In this work, an approach using the phase selection circuit to automatically decide what number of delay cells should be used. It can enable the DLL to operate in the wide frequency range Meanwhile, a new start-controlled circuit is presented for the DLL to solve false locking problems and keep the latency of one clock cycle. Its duty cycle is not necessary to be exact 50%.

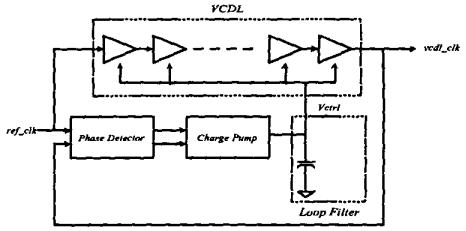

Fig.1 Block diagram of the conventional analog DLL

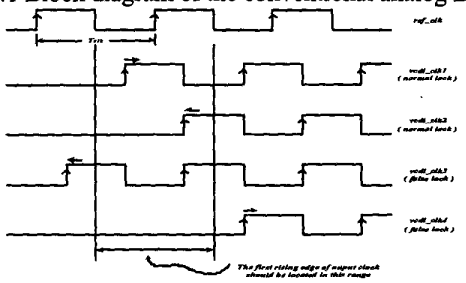

Fig.2 The DLL in normal lock and false lock conditions

2. The architecture of the proposed DLL

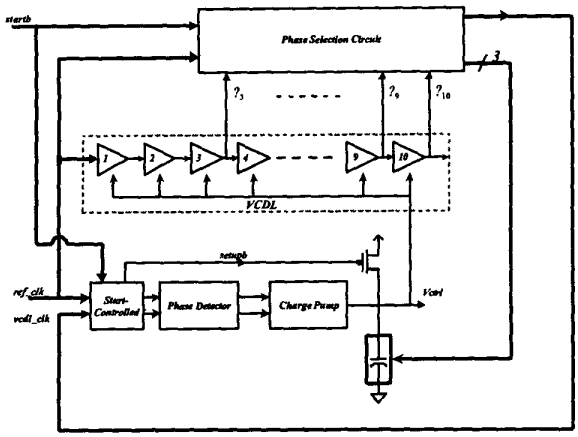

Fig.3 System architecture of the proposed DLL

The architecture of the proposed DLL is shown in Fig. 3. It is composed of a conventional analog DLL, a phase selection circuit and a start-controlled circuit. Before the DLL begins to lock, the phase selection circuit will choose an appropriate delay cell to be a feedback signal (vcdl_clk) according to different frequencies of input signal. In other words, the number of the delay cells may change at different input frequencies. The minimum delay, T_{Dmin}, of the delay line is determined by one unit-delay cell. The maximum delay is decided by $N \times T_{Dmax}$ where N is the number of unit-delay cells. Thus, the operating frequency range of the DLL can be from $1/T_{Dmin}$ to $1/(N \times T_{Dmax})$. As the input frequency is higher, the phase selection circuit will select the smaller number of delay cells and the gain of the VCDL which is proportional to the number of delay cells will become smaller. In order to have an adequate loop bandwidth for the DLL, the capacitances used in the loop filter must become smaller. In this work, 3-bits control signals generated from the phase selection circuit will switch the number of capacitors in the loop filter depending on the selected phase.

After the vcdl_clk is decided, the DLL will start the locking process which is controlled by the start-controlled circuit. First, the delay between input and output of the VCDL is initially set to the minimum value and then let the *down* signal of the PFD output activate, supposed that the VCDL's delay increases with control voltage decreasing. Therefore, the delay between input and output of the VCDL will increase until it reaches one clock period of the input signal. Thus, the DLL will not fall into false locking and the latency is fixed to one clock cycle no matter how long delay the VCDL can provide.

3. Circuit description

3.1 Phase section circuit

The phase selection circuit consists of two blocks: an edge detector and a multiplexer with a decoder, as shown in Fig. 4. The schematic and timing diagram of the edge detector are shown in Fig. 5 and Fig. 6, respectively. At initial state, the signal *startb* is set to low to reset the edge detector outputs (i.e., d3 ~ d10) and the delay of the VCDL is set to its minimum value. When the signal *startb* goes high, the edge detector will detect the rising edge of input signals in sequence during the next two rising edge of ref_clk. Referring to Fig. 6(a), suppose that the signals (phase 3 ~ phase 10) are all have rising edges in sequence during one clock cycle, therefore, the outputs (d3 ~ d10) are all high and the multiplexer will select the phase 10 as the output signal, vcdl_clk. However, if the input frequency is higher, suppose that the timing diagram is similar to Fig.6 (b). All the inputs have rising edges during one clock cycle, but only the rising edges of phases (1 ~ 4) in sequence lead the selected phase to be 4. The vcdl_clk will be low until the selected phase is chosen. After the vcdl_clk is decided, the DLL will start the locking process, which is explained later. By the decoder, signals (d3 ~ d10) are decoded to generate 3-bits control signals which switch the number of capacitors used in the loop filter for tuning the loop bandwidth.

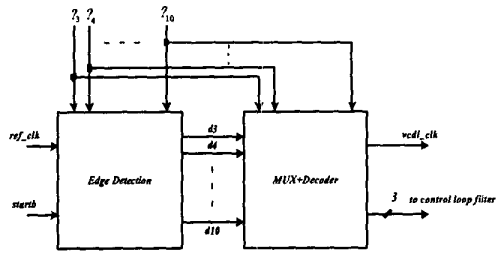

Fig.4 Block diagram of the phase selection circuit

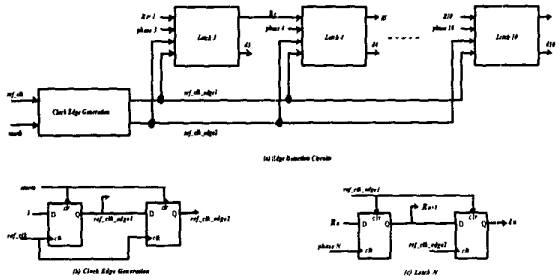

Fig.5 Schematic of edge detection circuit

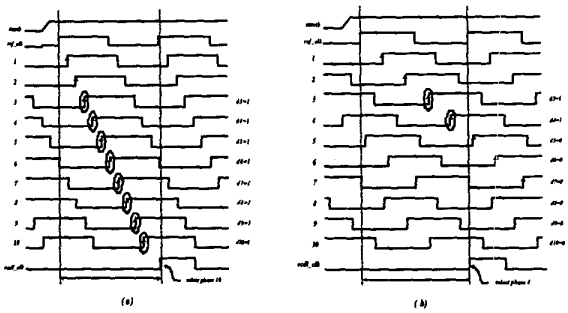

Fig.6 Timing diagram of edge detection circuit

3.2 Start-controlled circuit

The schematic of the start-controlled circuit and the associated PFD are shown in Fig. 7. It composes only of two rising edge

trigger DFFs, two NAND gates and two inverters. The timing diagram of this start-controlled circuit is shown in Fig. 8. Initially, *startb* is set to low in order to clear the two DFFs outputs. Therefore, *setupb* is low and pulls the control voltage to VDD as shown in Fig. 3 (i.e., set the VCDL delay to its minimum value). In this way, the two inputs of the PFD are in low level. When the *startb* goes to high, the *setupb* will also go to high. After two consecutive falling edges of vcdl_clk trigger the DFFs, the UP signal of the PFD will be activated and let the delay of the VCDL increase. The delay of the VCDL will increase until it is equal to one clock period of the input signal due to the nature of negative feedback architecture. In order to get equal delays for path1 and path2, some dummy loads should be added in point A. In comparison with [5], the start-controlled circuit has two advantages: one is that the proposed circuit is simple and the other is that the duty cycle of ref_clk and vcdl_clk does not require to be exact 50%.

3.3 Sub-circuits

In this work, the dynamic logic style PFD [9] is adopted to avoid the dead zone problem and improve the operating speed. To mitigate charge injection errors induced by the parasitic capacitors of the switches and current source transistors, the charge pump circuit developed in [10] is used here. The delay cell circuit is similar to [10]. The control voltage of the loop filter is directly feed to NMOS rather than PMOS. Therefore, the transfer curve of delay vs. control voltage is monotonic decreasing.

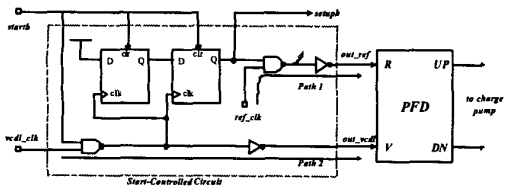

Fig. 7 Schematic of start-controlled circuit associated with PFD

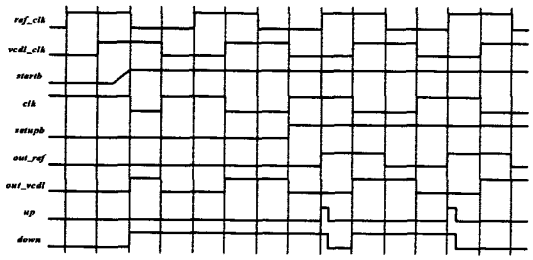

Fig.8 Timing diagram of start-controlled circuit

4. Measurement results

The prototype chip is fabricated in a 0.35-um single-ploy triple-metal standard CMOS process and the microphotograph of the chip is shown in Fig. 9. The capacitors used in the loop filter are integrated in the chip and formed by metal-to-metal capacitors. The experimental results show that the DLL can operate in the frequency range of 6 MHz ~ 130 MHz. Fig. 10 and Fig. 11 show the locking process of the DLL as the operating frequency is 6 MHz and 130 MHz, respectively. From Fig. 10 and Fig. 11, the delay between the input and output of the VCDL is just one clock period of input signal over operating frequency 6MHz ~ 130MHz. Besides, the phase error between the first rising edge of vcdl_clk and ref_clk is almost equal to the measured static error. In other words, the DLL has a fast-locking characteristic. Fig. 12 shows the jitter histogram when DLL operates in 130 MHz. Fig. 13 shows the measurement results of rms jitter over different frequencies. Table I gives the performance summary. As a result, the proposed DLL indeed have a wide-operational range and a fixed latency of one clock cycle.

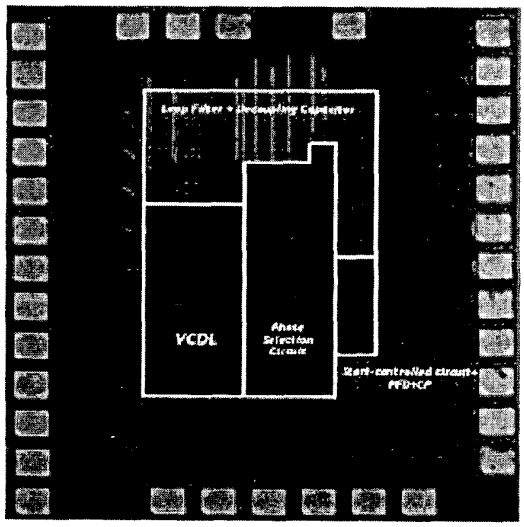

Fig.9 Microphotograph of the chip.

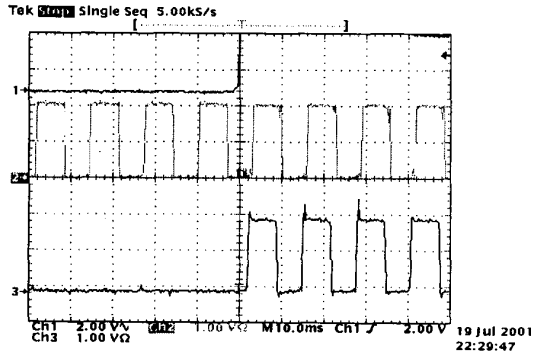

Fig.10 The DLL at initial state when operating frequency is 6MHz

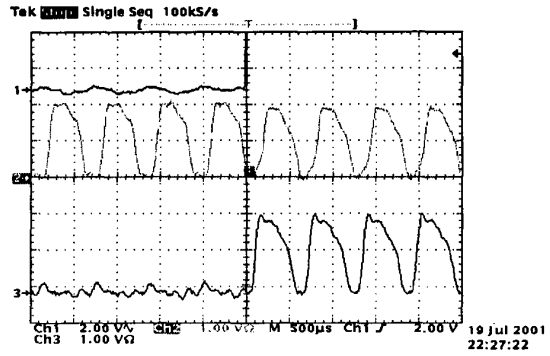

Fig.11 The DLL at initial state when operating frequency is 130MHz

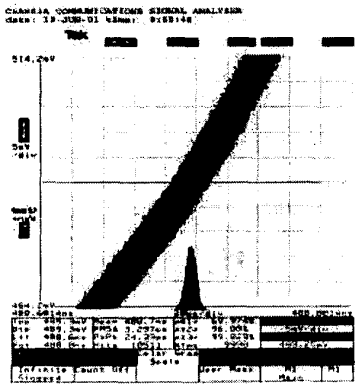

Fig.12 Jitter histogram when DLL operates at 130MHz

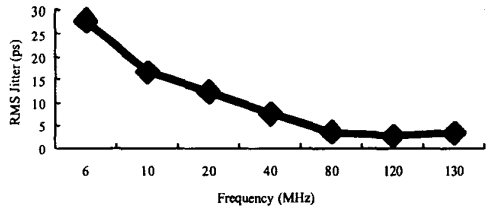

Fig.13 Measurement results of rms jitter over different frequencies

5. Conclusions

A DLL with wide-range operation and fixed latency of one clock cycle is proposed in this paper. First, the multiphase outputs of the VCDL are all send to the phase selection circuit. Then the phase selection circuit will auto matically select one of the delayed outputs to feedback. As a result, this DLL can operate over the wide range and fast locks without suffering from harmonic locking problems. Ideally, this DLL can operate from $1/(N \times T_{Dmax})$ to $1/T_{Dmin}$. The experimental results also demonstrate the functionality of the proposed DLL. Moreover, at different operating frequencies, the jitter performances are all in an acceptable range and the latency is just one clock cycle.

Table I: Performance Summary	
Process	0.35-um 1P3M TSMC CMOS process
Operating Voltage	3.3 V
Operating Frequency Range	6 MHz ~ 130 MHz
RMS Jitter	24.77 ps @ 6 MHz 3.297 ps @ 130 MHz
Peak-to-Peak Jitter	210 ps @ 6 MHz 24.3 ps @ 130 MHz
Power Dissipation	132 mW @ 130 MHz
Active Area	880-um×515-um @ without pads

6. References

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