Analysis and design of asymmetrical half bridge flyback converter

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Abstract: The detailed circuit behaviour of the asymmetrical half bridge flyback converter is analysed. The specific relationships between the duty cycle and the different types of energy in the energy storage elements are thoroughly investigated. From the analytical results, the maximum duty cycle is not bounded by 50%, which means that the converter can now be optimally used for the different applications. The zero voltage switching (ZVS) conditions of the power switches are derived. Mathematical equations and design considerations are also given. According to the presented design guidelines, the ZVS operations of the power switches can be maintained from no-load to full-load conditions. A 5 V/20 A prototype has been built to verify the analytical results under real life conditions.

List of symbols

A_e	effective cross-sectional area of the core of transformer T_X
D	duty cycle of switch S1
f_S	switching frequency of pulsewidth modulation (PWM) controller
i_{D1}	instantaneous current of output rectifier D1
I_{D1_RMS}	root mean square current of output rectifier D1
i_{Lr}	instantaneous current of resonant inductor L_r
I_M	average magnetising current of transformer
i_M	instantaneous magnetising current of transformer
ΔI_{M_pp}	peak to peak magnetising current of transformer
I_{S1_RMS}	root mean square current of S1
I_{S2_RMS}	root-mean-square current of S2
L_M	magnetising inductance of transformer
L_{lk}	leakage inductance of transformer
L_r	resonant inductor
N_P	number of turns of primary winding
n	turns ratio of transformer
P_{on_D1}	conduction loss of D1
P_{on_S1}	conduction loss of S1
P_{on_S2}	conduction loss of S2
P_{off_S1}	turn off switching loss of S1
P_{off_S2}	turn off switching loss of S2
R_{on_S1}	drain-to-source on-resistance of S1
R_{on_S2}	drain-to-source on-resistance of S2
T_S	switching period of pulsewidth modulation (PWM) controller
T_X	transformer of studied converter
V_{diode}	forward voltage drop on D1
V_C	average voltage across blocking capacitor C_b
v_C	instantaneous voltage across blocking capacitor C_b
ZVS	zero voltage switching, or more specifically, zero voltage turns on

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1 Introduction

The conventional flyback converter is attractive where multiple-output or cost-sensitive applications are concerned, thanks to its simple capacitive output filter. Nevertheless, hard switching operation of the power switch results in high switching loss, high EMI noises, and high switch voltage stress. Various kinds of soft switching techniques have been proposed for flyback converters [1–8]. Among them, the resonant converter [1, 2], the active-clamp circuit [3–5], and the asymmetrical half bridge converter are probably the most well known converters. A resonant converter can reduce switching losses and EMI noises. However, the voltage and/or current stresses increase and result in high conduction losses. The active clamp flyback converter [3–5] utilises an active clamp network to achieve ZVS operation of the power switches. However, the drawback is the high voltage stresses on the power switches.

The asymmetrical half bridge flyback converter, which can achieve ZVS operation of the power switches, is gaining popularity. The switch voltage stresses are no more than the input voltage that can be achieved. In previous works [6–8], the role of the blocking capacitor in the process of energy storage has been overlooked. When only the magnetic components are considered as the energy storage elements in the studied converter, a 50% duty cycle constraint has been derived [8]. However, in the present paper, it has been proved that the 50% duty cycle constraint does not occur. This is because the blocking capacitor also stores energy when the output rectifier is off. The specific relationships between the duty cycle and the various types of energy in the energy storage elements have been investigated in depth.

Fig. 1 shows the simplified circuit diagram of the asymmetrical half bridge flyback converter. The ZVS conditions for the power switches, S1 and S2, have not

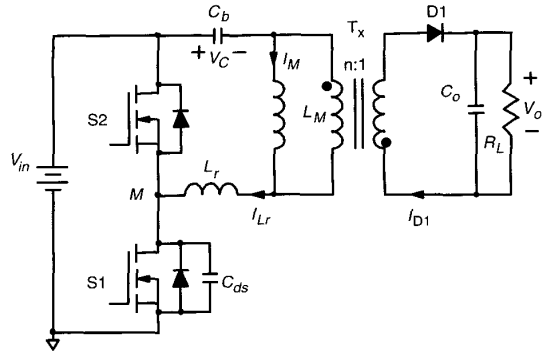

Fig. 1 *Simplified schematic of the asymmetrical half bridge flyback converter*

been discussed before. In fact, the ZVS mechanisms for them are quite different. One of them is just a linear charging process. The ZVS operation of this power switch, S2, can be maintained simply when there is a sufficiently long dead time between S1 and S2. However, the ZVS operation of the other switch, S1, is achieved only when the energy stored in the resonant inductor is greater than that of the output capacitors of these power switches.

Design considerations of the studied converter have also been investigated, according to its operational principles. Based on the presented design guidelines, the power switches can maintain ZVS from no-load to full-load situations.

2 Operational principles

Fig. 1 shows the simplified circuit diagram of the asymmetrical half bridge flyback converter. The inductor L_r denotes the combination of the leakage inductance of T_X and the external inductor. To describe the basic operational principles, several assumptions are made.

- The converter has reached steady-state operation.
- L_r is much less than L_M.
- The resonant period of C_b and L_r is much greater than the off time of S1.

To facilitate the analysis of the asymmetrical half bridge flyback converter, Fig. 2 and Fig. 3 show the seven topological stages of the converter during a switching cycle and its key waveforms, respectively. The operations of this converter can be explained as follows.

Stage 1 (t_0–t_1): At t_0, S1 is on and S2 is off. D1 is reversed biased in this stage. The DC input power source charges C_b, L_M and L_r. The charge time is brief compared with the time constant of this resonant tank, leading to an approximately linear charging characteristic. The following equations can be obtained:

$$(L_M + L_r)\frac{di_{Lr}}{dt} = V_{in} - v_C \tag{1}$$

$$C_b\frac{dv_C}{dt} = i_{Lr} = i_M \tag{2}$$

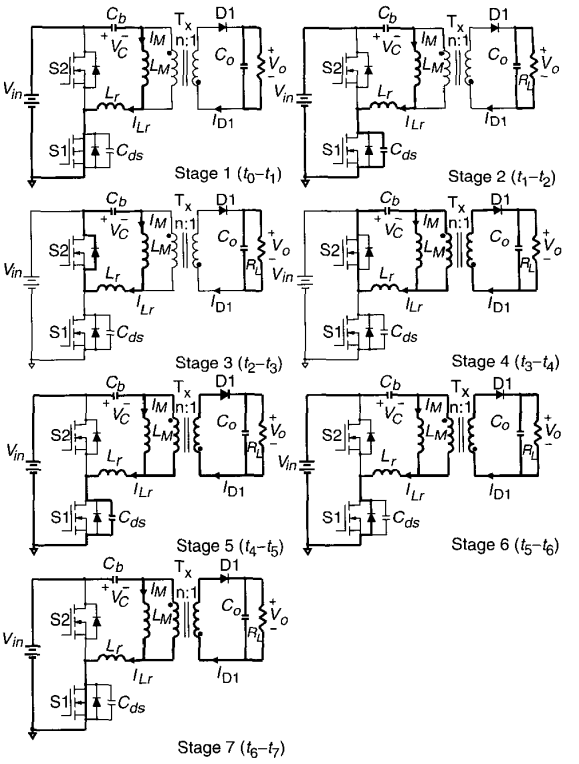

Fig. 2 *Asymmetrical half bridge flyback converter topological states*

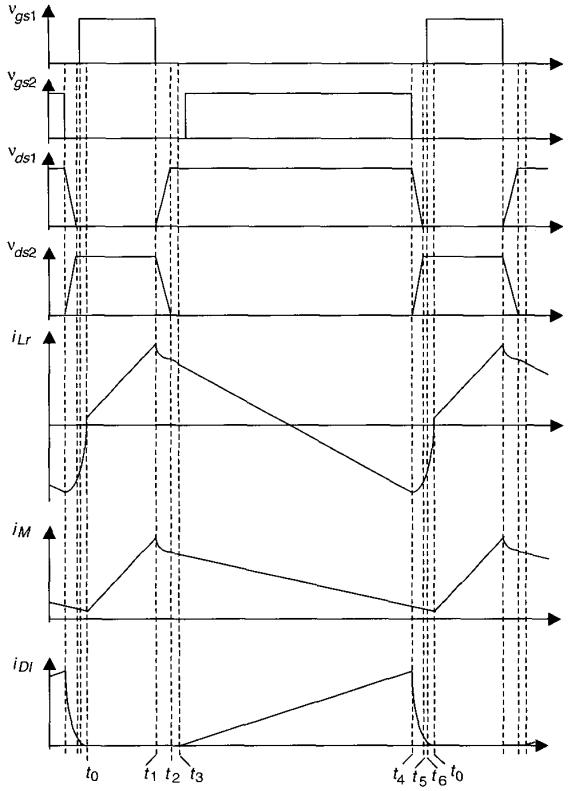

Fig. 3 *Steady state waveforms of asymmetrical half bridge flyback converter*

After solving (1) and (2), we have:

$$i_{Lr}(t) = \frac{V_{in} - v_C(t_0)}{Z_1}\sin[\omega_{r1}(t-t_0)] + i_{Lr}(t_0)\cos[\omega_{r1}(t-t_0)] \quad (3)$$

$$v_C(t) = V_{in} - [V_{in} - v_C(t_0)]\cos[\omega_{r1}(t-t_0)] + i_{Lr}(t_0)Z_1\sin[\omega_{r1}(t-t_0)] \quad (4)$$

where $Z_1 = \sqrt{\frac{L_M+L_r}{C_b}}$ and $\omega_{r1} = \frac{1}{\sqrt{C_b(L_M+L_r)}}$. This stage ends when S1 turns off.

Stage 2 (t_1–t_2): C_b, L_M, L_r, and C_{ds} form a new resonant network after S1 turns off at $t=t_1$. C_{ds}, which is the equivalent capacitance at point M, is charged by the current of L_r. In this stage, the state equations can be written as follows:

$$(L_M + L_r)\frac{di_{Lr}}{dt} = V_{in} - v_C - v_{ds} \quad (5)$$

$$C_b\frac{dv_C}{dt} = i_{Lr} = i_M \quad (6)$$

$$C_{ds}\frac{dv_{ds}}{dt} = i_{Lr} = i_M \quad (7)$$

Solving (5)–(7) gives:

$$i_{Lr}(t) = \frac{V_{in} - v_C(t_1)}{Z_2}\sin[\omega_{r2}(t-t_1)] + i_{Lr}(t_1)\cos[\omega_{r2}(t-t_1)] \quad (8)$$

$$v_C(t) = [V_{in} - v_C(t_1)]\frac{C_b//C_{ds}}{C_b}\{1-\cos[\omega_{r2}(t-t_1)]\} + \frac{i_{Lr}(t_1)}{\omega_{r2}C_b}\sin[\omega_{r2}(t-t_1)] + v_C(t_1) \quad (9)$$

$$v_{ds}(t) = [V_{in} - v_C(t_1)]\frac{C_b//C_{ds}}{C_{ds}}\{1-\cos[\omega_{r2}(t-t_1)]\} + \frac{i_{Lr}(t_1)}{\omega_{r2}C_{ds}}\sin[\omega_{r2}(t-t_1)] \quad (10)$$

where $Z_2 = \sqrt{\frac{L_M+L_r}{C_b//C_{ds}}}$ and $\omega_{r2} = \frac{1}{\sqrt{(C_b//C_{ds})(L_M+L_r)}}$. This stage ends when the antiparallel diode of S2 starts to conduct.

Stage 3 (t_2–t_3): After the antiparallel diode of S2 starts to conduct at t_2, C_b resonates with L_r and L_M. The voltage across L_M decreases. Before the current of L_r changes direction, S2 can be turned on under ZVS.

In this stage, the current of L_r charges C_b. The voltage across C_b increases due to the transfer of the energy from L_r and L_M. The state equations can be written as follows:

$$(L_M + L_r)\frac{di_{Lr}}{dt} = -v_C \quad (11)$$

$$C_b\frac{dv_C}{dt} = i_{Lr} \quad (12)$$

Solving (11) and (12), we have:

$$i_{Lr}(t) = -\frac{v_C(t_2)}{Z_1}\sin[\omega_{r1}(t-t_2)] + i_{Lr}(t_2)\cos[\omega_{r1}(t-t_2)] \quad (13)$$

$$v_C(t) = v_C(t_2)\cos[\omega_{r1}(t-t_2)] + i_{Lr}(t_2)Z_1\sin[\omega_{r1}(t-t_2)] \quad (14)$$

Stage 4 (t_3–t_4): After the output rectifier starts to conduct at t_3, i_{D1} is the difference between i_M and i_{Lr} multiplying by the turns ratio of T_X. The state equations can be written as follows:

$$L_M\frac{di_M}{dt} = -nV_o \quad (15)$$

$$L_r\frac{di_{Lr}}{dt} = -v_C + nV_o \quad (16)$$

$$C_b\frac{dv_C}{dt} = i_{Lr} \quad (17)$$

Solving (15)–(17) yields:

$$i_M(t) = i_M(t_3) - \frac{nV_o}{L_M}(t-t_3) \quad (18)$$

$$i_{Lr}(t) = \frac{nV_o - v_C(t_3)}{Z_3}\sin[\omega_{r3}(t-t_3)] + i_{Lr}(t_3)\cos[\omega_{r3}(t-t_3)] \quad (19)$$

$$v_C(t) = nV_o - [nV_o - v_C(t_3)]\cos[\omega_{r3}(t-t_3)] + i_{Lr}(t_3)Z_3\sin[\omega_{r3}(t-t_3)] \quad (20)$$

where $Z_3 = \sqrt{\frac{L_r}{C_b}}$ and $\omega_{r3} = \frac{1}{\sqrt{C_bL_r}}$.

Stage 5 (t_4–t_5): S2 turns off at t_4. The current of L_r discharges C_{ds}, and V_{ds} decreases. This stage ends when the antiparallel diode of S1 starts to conduct at t_5. The output rectifier still conducts at t_5, because the resonant inductor limits the discharging rate of i_{Lr}. The state equations can be written as follows:

$$L_M\frac{di_M}{dt} = -nV_o \quad (21)$$

$$L_r\frac{di_{Lr}}{dt} = V_{in} - v_C + nV_o - v_{ds} \quad (22)$$

$$C_b\frac{dv_C}{dt} = i_{Lr} \quad (23)$$

$$C_{ds}\frac{dv_{ds}}{dt} = i_{Lr} \quad (24)$$

Solving (21)–(24) yields:

$$i_M(t) = i_M(t_4) - \frac{nV_o}{L_M}(t-t_4) \quad (25)$$

$$i_{Lr}(t) = \frac{-v_C(t_4) + nV_o}{Z_4}\sin[\omega_{r4}(t-t_4)] + i_{Lr}(t_4)\cos[\omega_{r4}(t-t_4)] \quad (26)$$

$$v_C(t) = [-v_C(t_4) + nV_o]\frac{C_b//C_{ds}}{C_b}\{1-\cos[\omega_{r4}(t-t_4)]\} + \frac{i_{Lr}(t_4)}{\omega_{r4}C_b}\sin[\omega_{r4}(t-t_4)] + v_C(t_4) \quad (27)$$

$$v_{ds}(t) = [-v_C(t_4) + nV_o]\frac{C_b//C_{ds}}{C_{ds}}\{1-\cos[\omega_{r4}(t-t_4)]\} + \frac{i_{Lr}(t_4)}{\omega_{r4}C_{ds}}\sin[\omega_{r4}(t-t_4)] + V_{in} \quad (28)$$

where $Z_4 = \sqrt{\frac{L_r}{C_b//C_{ds}}}$ and $\omega_{r4} = \frac{1}{\sqrt{(C_b//C_{ds})L_r}}$.

Stage 6 (t_5–t_6): At t_5, V_{ds} has dropped to zero and the antiparallel diode of S1 is conducted. Before i_{Lr} changes direction, S1 can be turned on under ZVS. The equations

describing the circuit operation during this stage are as follows:

$$L_M \frac{di_M}{dt} = -nV_o \tag{29}$$

$$L_r \frac{di_{Lr}}{dt} = V_{in} - v_C + nV_o \tag{30}$$

$$C_b \frac{dv_C}{dt} = i_{Lr} \tag{31}$$

Solving (29)–(31), we can obtain:

$$i_M(t) = i_M(t_5) - \frac{nV_o}{L_M}(t - t_5) \tag{32}$$

$$i_{Lr}(t) = \frac{V_{in} - v_C(t_5) + nV_o}{Z_3}\sin[\omega_{r3}(t - t_5)] + i_{Lr}(t_5)\cos[\omega_{r3}(t - t_5)] \tag{33}$$

$$v_C(t) = [V_{in} - v_C(t_5) + nV_o]\{1 - \cos[\omega_{r3}(t - t_5)]\} + i_{Lr}(t_5)Z_3 \sin[\omega_{r3}(t - t_5)] + v_C(t_5) \tag{34}$$

Stage 7 (t_6–t_0): At t_6, S1 turns on under ZVS. The resonant inductor current i_{Lr} increases rapidly. This stage ends when this current increases to the point where the output rectifier cuts off. The DC input power source begins to charge C_b, L_r and L_M again. Another switching cycle starts.

3 Analysis

According to the above analysis, this Section will quantitatively analyse the key characteristics of this converter.

(i) Voltage transfer ratio. The voltage transfer ratio of the studied converter is proportional to the duty cycle. It can be easily derived from the flux balance in L_r and L_M. By neglecting the dead time between the conduction intervals of S1 and S2, the voltage transfer ratio can be obtained:

$$\frac{V_o}{V_{in}} = \frac{1}{n}\frac{L_M}{L_M + L_r}D \approx \frac{1}{n}D \tag{35}$$

Equation (35) indicates that the linear relationship between the input voltage and the output voltage is the same as buck-derived converters with transformer isolation.

(ii) V_C. The average voltage across the blocking capacitor depends on the duty cycle. It can be obtained when solving the voltage transfer ratio.

$$V_C = V_{in}D \tag{36}$$

(iii) I_M. The average magnetising current of T_X is affected by the load current and the turns ratio of T_X. Owing to the series connection of the blocking capacitor and T_X, the average magnetising current can be solved from the charge balance in the blocking capacitor:

$$\int_0^{T_S} i_{Lr}(t)dt = 0 \tag{37}$$

It follows that

$$I_M = \frac{I_o}{n} \tag{38}$$

(iv) Energy-storage elements. The energy-storage elements in this converter consist of the blocking capacitor, the magnetising inductor of T_X, and the resonant inductor.

Fig. 4 shows the simplified waveforms of the voltage across the blocking capacitor and the current of the resonant inductor. During the interval DT_S, the DC input power source charges C_b, L_M and L_r, causing

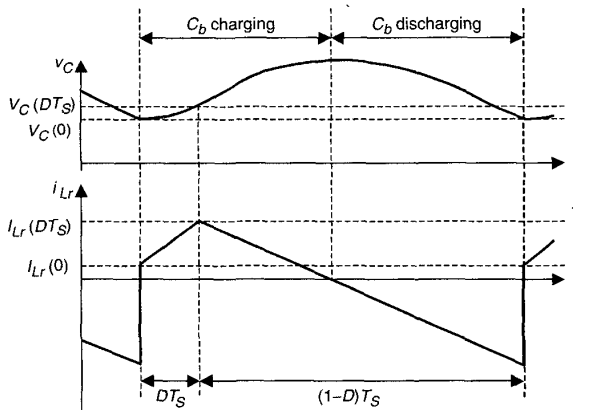

Fig. 4 *Simplified waveforms of voltage across blocking capacitor and current of resonant inductor*

increments in the voltage across C_b as well as the current of L_M and L_r. The energy stored in these elements can be expressed as:

$$E_{LM} + E_{Lr} = \frac{1}{2}(L_M + L_r)[I_{Lr}^2(DT_S) - I_{Lr}^2(0)] \tag{39}$$

$$E_{C_b} = \frac{1}{2}C_b\left[V_{C_b}^2(DT_S) - V_{C_b}^2(0)\right] \tag{40}$$

The incremental voltage across C_b for this duration can be expressed as:

$$V_{C_b}(DT_S) - V_{C_b}(0) = \frac{1}{C_b}\int_0^{DT_S} i_{Lr}(t)dt = \frac{1}{C_b}\frac{I_o}{n}DT_S \tag{41}$$

The incremental current of L_M and L_r for this duration can be written as:

$$I_{Lr}(DT_S) - I_{Lr}(0) = \frac{1}{L_M + L_r}\int_0^{DT_S}(V_{in} - v_c(t))dt = \frac{1}{L_M + L_r}\left(\frac{2V_{in} - V_{C_b}(DT_S) - V_{C_b}(0)}{2}\right) \times DT_S \tag{42}$$

Inserting (42) into (39) yields:

$$E_{LM} + E_{Lr} = \frac{1}{2}\frac{I_o}{n}DT_S[2V_{in} - (V_{C_b}(DT_S) + V_{C_b}(0))] \tag{43}$$

Combining (40) and (41), we can obtain:

$$E_{C_b} = \frac{1}{2}\frac{I_o}{n}DT_S[V_{C_b}(DT_S) + V_{C_b}(0)] \tag{44}$$

From (43) and (44), the total energy stored during the interval DT_S is

$$E_{LM} + E_{Lr} + E_{C_b} = \frac{I_o}{n}DT_S V_{in} = P_o T_S \tag{45}$$

When the voltage ripple across the blocking capacitor is neglected, (43) and (44) can be further condensed into

$$E_{LM} + E_{Lr} \approx \frac{1}{2}\frac{I_o}{n} DT_S[2V_{in} - 2V_{in}D] = P_o T_S(1 - D) \quad (46)$$

$$E_{C_b} = \frac{1}{2}\frac{I_o}{n} DT_S(2V_{in}D) = P_o T_S D \quad (47)$$

Equations (46) and (47) clearly describe the relationships between the amount of stored energy and the duty cycle.

During another interval $(1-D)T_S$, part of the energy stored in L_M and L_r transfers to the secondary side of T_X and the rest of the energy charges C_b. After the resonant inductor current changes direction, the energy stored in C_b transfers to the output capacitor via T_X.

(v) Current of L_r. The simplified current waveforms of i_{Lr}, i_M and i_{D1} are shown in Fig. 5. The positive peak current of the resonant inductor (which is equal to the peak magnetising current and peak current of S1) can be expressed as:

$$I_{Lr\_ppk} = I_M + \frac{1}{2}\frac{V_{in} - V_C}{L_M + L_r} DT_S \approx \frac{I_o}{n} + \frac{1}{2}\frac{V_{in}(1 - D)}{L_M} DT_S \quad (48)$$

In the same way, the minimum of magnetising current i_{M_valley} can be expressed as:

$$I_{M\_valley} \approx \frac{I_o}{n} - \frac{1}{2}\frac{V_{in}(1 - D)}{L_M} DT_S \quad (49)$$

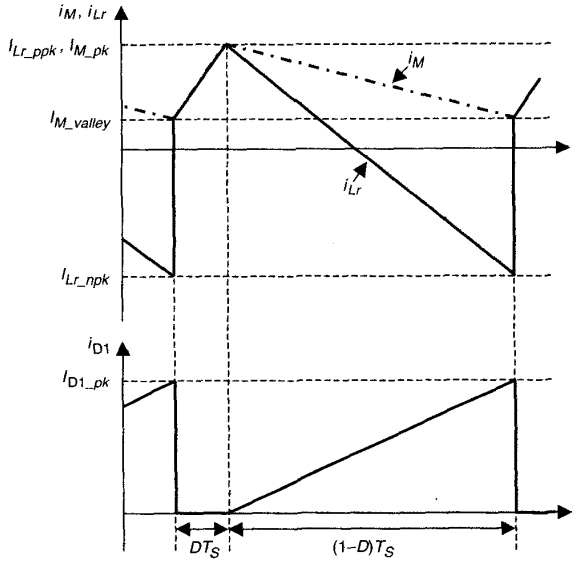

Fig. 5 *Simplified current waveforms of resonant inductor, magnetising inductor and output rectifier*

From Fig. 5, the peak value of i_{D1} can be solved by

$$\frac{1}{2} I_{D1\_pk}(1 - D) = I_o \quad (50)$$

Solving (50), the peak current of the output rectifier is

$$I_{D1\_pk} = 2\frac{I_o}{1 - D} \quad (51)$$

According to the circuit operational principles described in Section 2, i_{D1} is equal to the difference of i_M and i_{Lr} multiplied by the turns ratio of T_X when S2 is on. The negative peak current of the resonant inductor can be derived from

$$I_{Lr\_npk} = I_{M\_valley} - \frac{1}{n} I_{D1\_pk} \approx -\frac{I_o}{n}\frac{1 + D}{1 - D} - \frac{1}{2}\frac{V_{in}(1 - D)}{L_M} DT_S \quad (52)$$

The current of L_r is the key determinant of ZVS operation of the switches, which will be discussed in the following Section.

(vi) ZVS condition. The ZVS mechanism of S2 is like a linear charging process. According to (10) in Section 2, the ZVS condition of S2 can be obtained as

$$v_{ds}(t) = (V_{in} - v_C(t_1))\frac{C_b // C_{ds}}{C_{ds}}(1 - \cos[\omega_{r2}(t - t_1)]) + \frac{i_{Lr}(t_1)}{\omega_{r2} C_{ds}} \sin[\omega_{r2}(t - t_1)] \geq V_{in} \quad (53)$$

For $C_b \gg C_{ds}$ and $\omega_{r2}(t - t_1)$ small, such that $\sin[\omega_{r2}(t - t_1)] \approx \omega_{r2}(t - t_1)$ and $\cos[\omega_{r2}(t - t_1)] \approx 1$, we get an approximate solution:

$$t - t_1 \geq C_{ds}\frac{V_{in}}{i_{Lr}(t_1)} \quad (54)$$

where $i_{Lr}(t_1)$ is the I_{Lr_ppk} in (48). From (54), the ZVS operation of S2 can always be maintained when a sufficiently long dead time between the two power switches is used. The required dead time to achieve ZVS operation of S2 can be obtained from (48) and (54).

The ZVS condition of S1 depends on the energy stored in L_r, which is quite different from S2. It can be obtained from (28) in Section 2:

$$v_{ds}(t) = (-v_C(t_4) + nV_o)\frac{C_b // C_{ds}}{C_{ds}}(1 - \cos[\omega_{r4}(t - t_4)]) + \frac{i_{Lr}(t_4)}{\omega_{r4} C_{ds}} \sin[\omega_{r4}(t - t_4)] + V_{in} \leq 0 \quad (55)$$

Owing to the angular frequency ω_{r4} being much bigger than ω_{r2}, we cannot assume that $1 - \cos[\omega_{r4}(t - t_4)] \approx 0$ and omit this term, as in the previous case. However, this term can still be omitted because its coefficient is negligible when compared with that of the other terms. Therefore, (55) can be further simplified to

$$\frac{i_{Lr}(t_4)}{\omega_{r4} C_{ds}} \sin[\omega_{r4}(t - t_4)] + V_{in} \leq 0 \quad (56)$$

We can rearrange (56) to give

$$\sin[\omega_{r4}(t - t_4)] \leq -\frac{V_{in}}{i_{Lr}(t_4)} \omega_{r4} C_{ds} \quad (57)$$

Solving (57), the ZVS condition of S1 can be obtained:

$$\frac{1}{2} L_r i_{Lr}(t_4)^2 \geq \frac{1}{2} C_{ds} V_{in}^2 \quad (58)$$

where $i_{Lr}(t_4)$ is the I_{Lr_npk} in (52). From (58), the ZVS condition of S1 depends on the energy stored in L_r.

(vii) Loss analysis. The major contributions to losses of the studied converter are classified into two categories: the losses in the semiconductor devices, and the losses in

the transformer. The former includes the turn off switching losses of S1 and S2, and the conduction losses of S1, S2, and D1. The turn off switching losses of S1 and S2 can be calculated as:

$$P_{off\_S1} = \int_{t_1}^{t_2} v_{ds}(t) i_{Lr}(t) dt \quad (59)$$

$$P_{off\_S2} = \int_{t_4}^{t_5} [V_{in} - v_{ds}(t)] i_{Lr}(t) dt \quad (60)$$

The conduction losses of S1, S2, and D1 are:

$$P_{on\_S1} = R_{on\_S1} I^2_{S1\_RMS} \quad (61)$$

$$P_{on\_S2} = R_{on\_S2} I^2_{S2\_RMS} \quad (62)$$

$$P_{on\_D1} = V_{diode} I_o \quad (63)$$

where R_{on_S1} and R_{on_S2} are the drain-to-source on-resistance of S1 and S2 respectively, and V_{diode} is the forward voltage drop on D1. The losses in the transformer include the core loss and the copper loss, which are no different to those for a traditional flyback converter. With careful design, these losses can be controlled within an acceptable level.

4 Design considerations

This Section presents the design considerations and important design parameters of the studied converter according to its operational principles and characteristics.

(i) Duty cycle. From (35) in Section 3, the linear relationship between the input voltage and the output voltage means that the maximum duty cycle can exceed 50% when voltage mode control is applied. The drawback of wider duty cycle operation is that larger input capacitance would be required to satisfy the hold-up time requirement in some applications. On the other hand, increasing the duty cycle will lower the voltage stress on the output rectifier. This can be derived from the maximum reverse voltage seen by the output rectifier:

$$V_{D1\_KA} = \frac{V_{in} - V_C}{n} + V_o \approx \frac{V_o}{D} \quad (64)$$

Fig. 6 illustrates this phenomenon distinctly. In real life conditions, the hold-up time is required to be greater than one line period, or about 16 ms for a 60 Hz AC line frequency. Usually, a 17~20 ms hold-up time is the common specification in most commercial products. In Fig. 6, the value of the input capacitance to satisfy the 20 ms hold-up time requirement when operating under current mode control and voltage mode control are given, respectively. Owing to the upper constraint on the duty cycle, the input capacitance should be greater when current mode control is applied. A compromise between the input capacitor size and the output rectifier voltage stress should be made.

(ii) Transformer magnetising inductor. The magnetising inductor design is similar to the energy storage choke in the

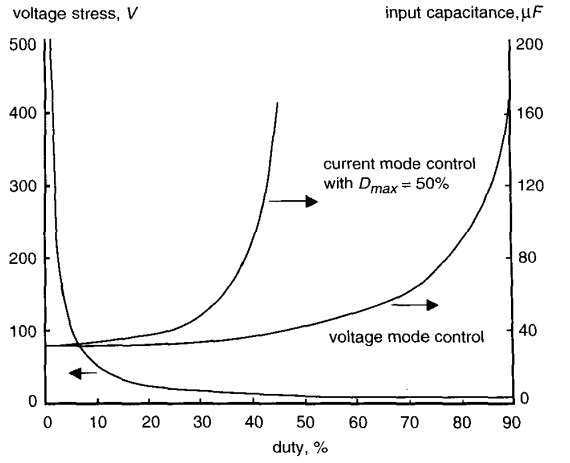

Fig. 6 *Required input capacitance and output rectifier voltage stress as function of duty cycle (this 'input capacitance' is referred to bulk electrolytic capacitor connected in parallel with input source; simulated at holdup time = 20 ms, V_{in} = 400 V, V_o = 5 V, and I_o = 20 A)*

conventional flyback converter operating in continuous current mode. It can be determined by

$$L_M \leq \left[B_{sat} \times 10^{-8} - \frac{V_{in} D(1-D) T_S}{2 N_p A_e} \right] \times N_p A_e \frac{n}{I_o} \quad (65)$$

(iii) Resonant inductor. The resonant inductor design can be determined by the selected ZVS operation range of S1. From (52) and (58), the required resonant inductance for achieving ZVS of S1 can be obtained. However, using a larger resonant inductance to ensure the ZVS operation of S1 at light load condition is not preferred. Fig. 7 shows the required resonant inductance to achieve ZVS of S1 under the full load range at different duty cycle operation. The steep slope curve of the resonant inductance of 'D = 30%' shows that the necessary resonant inductance for ZVS of S1 in light load is much greater

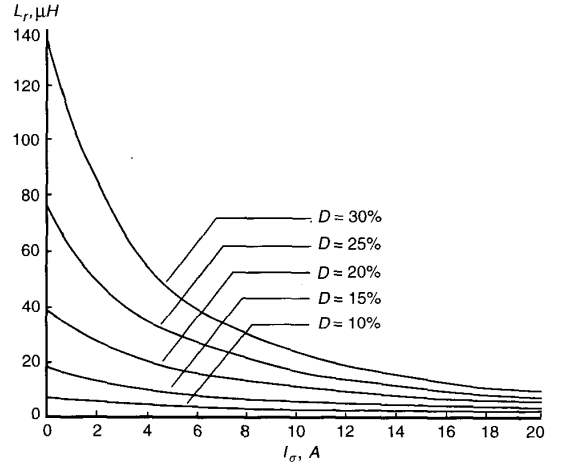

Fig. 7 *Required resonant inductance for ZVS operation of S1 as function of load, for several value of duty cycle (simulated at V_{in} = 400 V, V_o = 5 V and I_o = 20 A)*

than that in heavy load. When the output rectifier starts to cut off, the energy stored in the resonant inductor will cause resonance between the resonant inductor and the parasitical capacitors of the output rectifier and the transformer. Choosing an even curve in Fig. 7, which means choosing a lower duty cycle, or narrowing the ZVS operation range to alleviate the excessive ringing effect at heavy load is recommended.

In real life conditions, using the sandwich winding construction for the winding arrangement of the transformer, T_X, to reduce the leakage inductance is recommended. After measuring the leakage inductance from the finished transformer, one can determine the necessary external inductance to satisfy (58). This method will increase the controllability and also remove the heat inside the transformer to the external inductor.

(iv) Blocking capacitor. The greater the value of C_b, the more energy is stored in C_b when S1 is on. After S1 is off, the energy stored in L_M and L_r is transferred to the output and charges C_b at the same time. The energy of C_b does not release to the output via T_X until the current of L_r changes direction. Using a larger size of C_b will increase the energy stored in C_b when S1 is on, but will slow down the circuit dynamic response.

(v) Power switches. According to the circuit operational principles, the current of the resonant inductor is equal to i_{S1} when S1 is on, and is equal to i_{S2} when S2 is on. Therefore, the peak current of S1 is the same as the positive peak current of the resonant inductor, which is

$$I_{S1\_pk} = I_{Lr\_ppk} \approx \frac{I_o}{n} + \frac{1}{2}\frac{V_{in}(1-D)}{L_M}DT_S \tag{66}$$

The RMS current of S1 can be derived from

$$I_{S1\_RMS} = \frac{1}{T_S}\int_0^{DT_S} i_{lk}(t)dt \approx \sqrt{\frac{I_o^2}{n^2}D + \frac{D}{12}\Delta^2 I_{M\_pp}} \tag{67}$$

where ΔI_{M_pp} is the peak-to-peak value of the magnetising current of T_X.

S2 and the resonant inductor have the same current when S2 is conducted. Owing to the arrangement of S2 and L_r, I_{S2_pk} is equal to the negative value of I_{Lr_npk}, which is

$$I_{S2\_pk} = -I_{Lr\_npk} \approx \frac{I_o}{n}\frac{1+D}{1-D} + \frac{1}{2}\frac{V_{in}(1-D)}{LM}DT_S \tag{68}$$

The RMS current of S2 can be obtained from

$$I_{S2\_RMS} = \frac{1}{T_S}\int_{DT_S}^{T_S} -i_{lk}(t)dt \approx \sqrt{\frac{I_o^2}{n^2}\left[\frac{3D-1}{3(1-D)}\right] + \frac{1}{3}\Delta I_{M\_pp} + \frac{1-D}{12}\Delta^2 I_{M\_pp}} \tag{69}$$

The voltage stresses of S1 and S2 are no greater than the DC input voltage.

(vi) Output rectifier. The RMS current and the voltage stress of the output rectifier depend on the duty cycle. When the peak output rectifier current has been obtained in (51), the RMS value of this current can be derived from

$$I_{D1\_RMS} = \frac{1}{T_S}\int_0^{T_S} [i_M(t) - i_{lk}(t)]dt \approx 2I_o\sqrt{\frac{1}{3(1-D)}} \tag{70}$$

The output rectifier should be chosen to handle the voltage stress of $\frac{V_o}{D}$ and RMS current calculated in (70).

5 Experimental results

According to the design considerations presented in the preceding Section, a prototype is implemented with the following specifications: input voltage $V_{in} = 400$ V DC, output voltage $V_o = 5$ V DC, maximum load current = 20 A, switching frequency $f_S = 60$ kHz, and ZVS range = 0% to 100% load.

The power stage consists of the following parameters. Switches S1 and S2: Toshiba 2SK2842, diode D1: 2 × Toshiba 30GWJ2C42C, blocking capacitor C_b: 3.3 μF/250 V, input capacitor: 68 μF/450 V, transformer: A_e of core = 1 cm^2, primary is 36 turns of litz wire 20 × 0.1 mm, secondary is 3 turns of litz wire 100 × 0.1 mm, $L_M = 280$ μH, $L_{lk} = 8$ μH, resonant inductance, $L_r = 18$ μH (includes L_{lk} and an external inductance), and dead time = 100 μs (between the turn-off of S1 and turn-on of S2).

Some key experimental waveforms are shown in Fig. 8. These waveforms resemble closely those shown in Fig. 3. The ZVS operations of S1 and S2 can be noted from the waveforms shown in Fig. 9. From Fig. 9*a* and 9*c*, the converter retains ZVS operations of S1 and S2 even under the no load condition. The efficiency of the converter is plotted in Fig. 10.

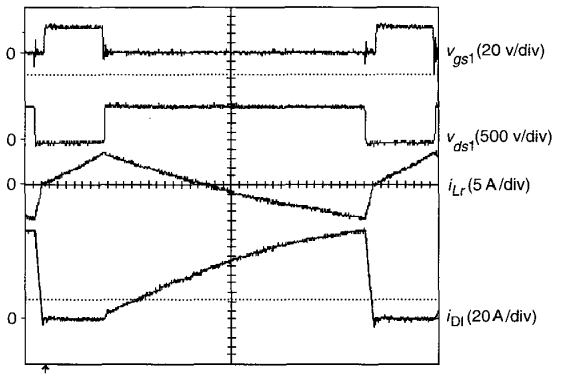

Fig. 8 *Experimental waveforms (time scale is 2 μs/div)*

6 Conclusion

From the analytical and experimental results, several circuit features have been observed.

Not only the magnetising inductor of the transformer and the resonant inductor, but also the blocking capacitor store energy when the output rectifier is off. When the duty cycle increases, the energy stored in the blocking capacitor will also increase accordingly. However, the energy stored in the magnetising inductor and the resonant inductor will decrease. Most of the energy is stored in the blocking capacitor when the duty cycle exceeds 50%.

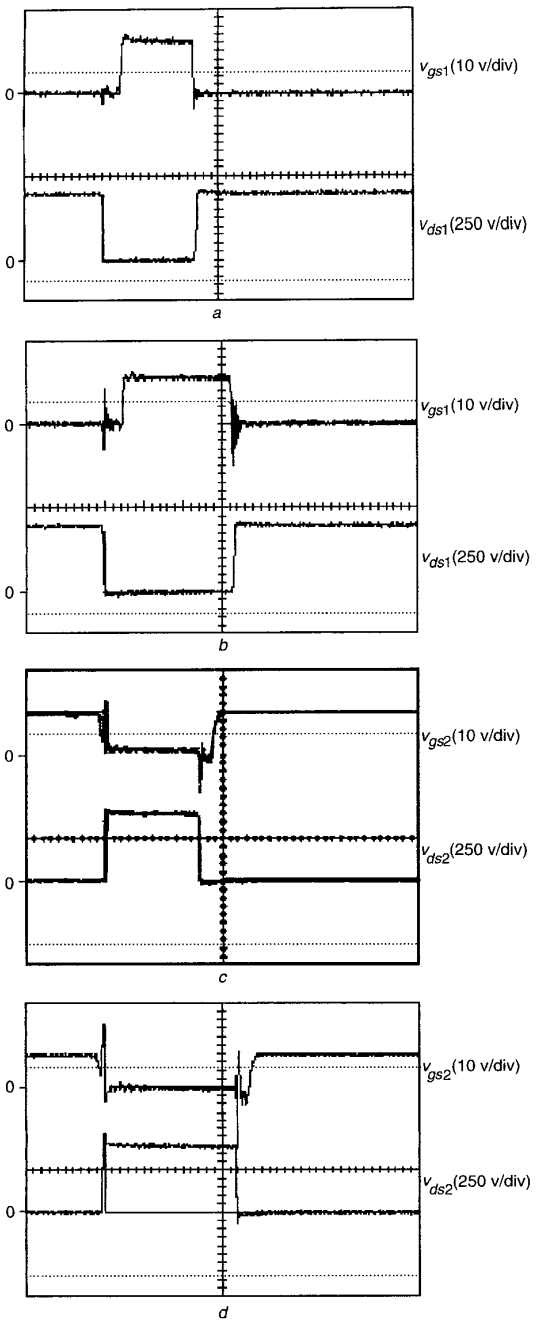

Fig. 9 *Experimental ZVS waveforms (Time scale is 1 μs/div)*
a S1 at no load
b S1 at full load
c S2 at no load
d S2 at full load

The ZVS conditions of the two power switches are quite different. The ZVS operation of S2 can always be maintained when a sufficiently long dead time between S1 and S2 is used. However, S1 achieves ZVS only when the energy stored in L_r is larger than that of C_{ds}.

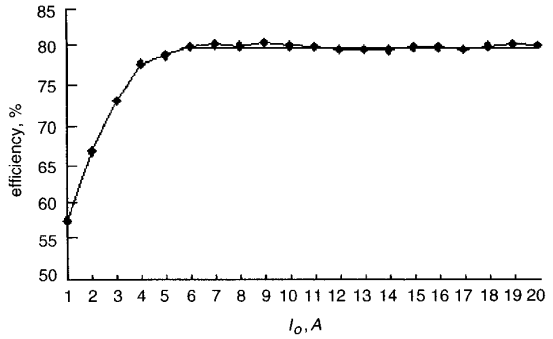

Fig. 10 *Measured efficiency of prototype (V_{in} = 400 V, V_o = 5 V)*

Larger L_r ensures the ZVS operation of S1, but increases the noise in the output rectifier. Lowering the duty cycle can extend the ZVS operation range of S1 and can also suppress ringing on the output rectifier. However, this will increase the voltage stress on the output rectifier. A compromise between ZVS range and the level of noise in the output rectifier should be made.

This paper has described the circuit behavior of the asymmetrical half bridge flyback converter. Design considerations and trade-offs have also been suggested. A 5 V/20 A prototype has been built to verify the analytical results. The experimental results show that the power switches can maintain ZVS operations from no-load to full-load, and that the efficiency can reach an optimum value of 80%.

7 Acknowledgments

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