A 0.8-8 GHz 9.7 mW Analog-Digital Dual-Loop Adaptive-Bandwidth DLL Based Multi-Phase Clock Generator

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Abstract

This paper presents an implementation of a low-jitter wide-range multi-phase clock generator using a delay-locked loop (DLL) for ultra-wideband (UWB) application. The analog-digital dual-loop adaptive-bandwidth structure in conjunction with a complementary phase detector (PD) ensures low-jitter clock generation over a wide frequency range. The self-feedback technique reduces the power consumption of the level-shifter circuit 50% at least. The 0.18-μm CMOS prototype exhibits the maximum clock jitter of 3.9 ps (rms) and 28.7 ps (pk-pk) at an output clock rate of 1.6 to 8 GHz (50-250 MHz input reference frequency) and consumes 9.7 mW from a 1.8-V supply at 8 GHz.

1. Introduction

One critical aspect of VLSI implementation of pulse-based UWB radio is the accurate generation of timing signals to support reliable data communications [1]. Phase-locked loops (PLLs) and delay-locked loops (DLLs) have been typically employed to generate the required accurate high-frequency system clock from a low-frequency, precise, and stable oscillator. Usually, DLLs are easier than PLLs to implement the clock generator. A DLL is unconditionally stable and only needs one capacitor in its first-order loop filter. Moreover, a DLL offers better jitter performance than a PLL because phase errors induced by supply or substrate noises do not accumulate over many cycles in the delay line [2]. The adaptive-bandwidth architecture is often adopted in the design of the DLL to ensure optimum performance over a wide frequency range and across process, voltage, and temperature (PVT) variations [3], [4]. However, these conventional DLLs would lose the adaptive-bandwidth characteristic and generate more jitters inherently if the DLL output signal swing which is proportional to loop control voltage approaches the device threshold [5], [6]. Therefore, the conventional adaptive-bandwidth design still suffers from large performance variation when the DLL needs to operate across a wide frequency range.

This paper describes an adaptive-bandwidth DLL for the low-jitter wide-range multi-phase clock generation in UWB application. The proposed analog-digital dual-loop structure maintains the output signal swing at a sufficiently high voltage level to ensure jitter performance over a wide operating frequency range. The complementary phase detector (PD) and self-feedback level shifter are introduced to further improve the jitter performance and reduce the power consumption respectively.

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2. DLL Architecture

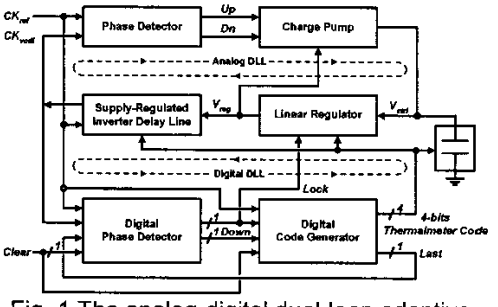

Fig. 1 The analog-digital dual-loop adaptive-bandwidth DLL architecture.

The proposed dual-loop DLL shown in Fig. 1 is composed of a *digital DLL* and an *analog DLL*. The *digital DLL* first judges delay relationship between the input reference clock CK_{ref} and delayed clock from the last stage of delay line CK_{vcdl} by digital phase detector which signals the following digital code generator to generate digital control word of 4-bits thermometer code. The delay of the delay line can be coarsely tuned by the digital control code word through sequentially turning off four additional parallel banks of delay line placed around the main delay line. The lock-in process within digital DLL would continue until the delay of the delay line has been placed in the optimum lock-in range of the *analog DLL*. The analog DLL then takes over the loop and finely tunes the delay of the delay line to eliminate the remaining phase error. The linear PD, the charge pump (CP), the loop filter, the linear voltage regulator, and the supply regulated delay line comprising 16 pseudo-differential delay elements compose the analog DLL.

Fig. 2 shows the detailed timing diagram of the dual-loop DLL when the DLL starts from reset state. The four additional parallel banks of delay line are initially all turned on (corresponding to the code word *0000*) and the delay of the delay line is set to its minimum delay in order to avoid harmonic-locking problem. The digital code generator then keeps updating the digital control code word to increase the delay of the delay line by sequentially turning off the parallel banks of the delay line. If the delay of the delay line is larger than one period of CK_{ref}, the

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digital phase detector would immediately respond by activating the *Lock* control signal and setting the digital control code word to its prior value. The analog DLL takes control of the loop from this time with minimum phase error, which means that it can finally lock to the highest possible loop control voltage at steady state. This two-step lock-in process ensures the proposed DLL can keep good jitter performance while achieving a wide operating frequency range.

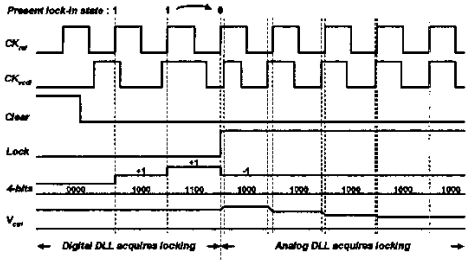

Fig. 2 Timing diagram of the dual-loop DLL.

The loop bandwidth of the charge pump based DLL can be expressed as [3]:

$$\omega_N = I_{CH} \cdot K_{DL} \cdot F_{REF} \cdot \frac{1}{C_L} \tag{1}$$

where I_{CH} is the charge pump current, C_L is the loop filter capacitor, K_{DL} is the delay line gain, and F_{REF} is the frequency of the input reference clock. In the analog-digital dual-loop DLL architecture, because the delay of the delay line is controlled by both the number of the turned-on delay line banks and the regulated supply voltage, K_{DL} is related to the value of the digital control code word D_{ctrl} and loop control voltage V_{ctrl} by:

$$K_{DL} = \frac{K_1 \cdot D_{ctrl}}{(V_{ctrl} - V_T)^2} \tag{2}$$

where K_1 is a proportional constant and V_T is the threshold voltage of the transistor. If the charge pump is biased with V_{ctrl} and the number of capacitors in the loop filter is determined by D_{ctrl}, it can be shown:

$$I_{CH} = K_2 \cdot (V_{ctrl} - V_T)^2 \tag{3}$$

$$C_L = K_3 \cdot D_{ctrl} \tag{4}$$

where K_2 and K_3 are proportional constants. By combining (1)-(4), the loop bandwidth of the dual-loop DLL is then given by:

$$\omega_N = \frac{K_1 \cdot K_2}{K_3} \cdot F_{REF} \tag{5}$$

Equation (5) indicates ω_N is directly proportional to F_{REF}, which means the dual-loop DLL has the adaptive-bandwidth characteristic similar to the conventional analog adaptive-bandwidth DLLs [3], [4]. Therefore, the dual-loop DLL possesses all the advantages of the adaptive-bandwidth architecture no matter which digital control code word D_{ctrl} is chosen to acquire locking.

3. Circuit Design

3.1. Digital Phase Detector and Code Generator

Fig. 3 shows the schematic of the digital phase detector, which is composed of a lock-in state decoder, a transition detector, and decoding logics for *Lock* signal. The present lock-in state can be determined by sampling CK_{vcdl} at the rising edge of CK_{ref}, as shown in Fig. 2. The *Last* signal generated by the digital code generator is activated when the delay of the delay line has reached the maximum value (corresponding to the code word *1111*) in the lock-in process of the digital DLL. Fig. 4 shows the schematic of the digital code generator, which consists of six code cells to produce 4-bit thermometer code. The additional two cells are used for pipelining in order to increase the timing margin allowed for circuits to response.

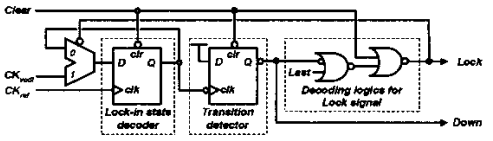

Fig. 3 The digital phase detector.

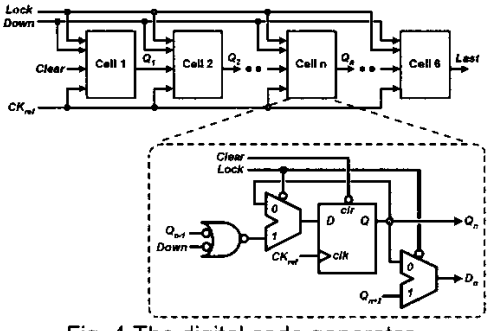

Fig. 4 The digital code generator.

3.2. Complementary Phase Detector

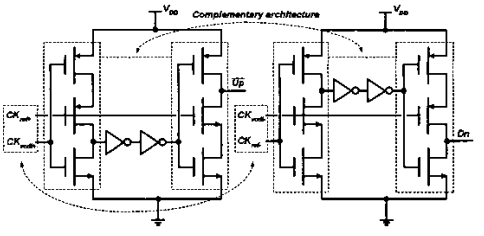

Fig. 5 The complementary phase detector.

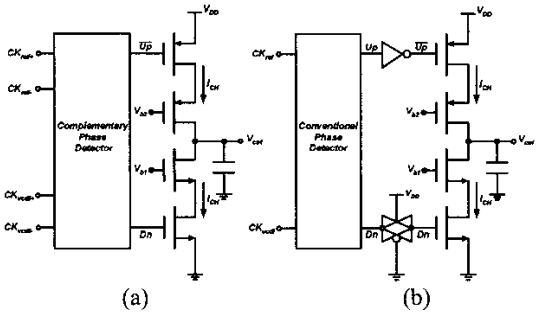

Fig. 6 (a) Complementary PD and (b) conventional PD with CP.

Fig. 5 shows the schematic of the complementary PD circuits, which are based on one basic dynamic logic PD

cell and its complement. The complementary property is established by using the complementary input signals and interchanging the positions of the two dynamic logics. The additional inverters interposed between dynamic logics help the PD periodically to produce a chain of short pulses in the locked state which can reduce the dead zone of the PD effectively. The complementary PD can directly generate two control signals $\overline{Up}$ and *Dn* with zero skew difference to sense the following CP circuit charging or discharging the loop filter, as shown in Fig. 6(a). The conventional approach shown in Fig. 6(b) uses an additional inverter and a transmission gate to produce $\overline{Up}$ and *Dn* control signals. However, the delays caused by the inverter and the transmission gate are usually hardly matched under PVT variations, which causes additional ripples on the loop control line and thus results in a deterministic jitter of the DLL output when the loop is locked.

3.3. Supply-Regulated Delay Line

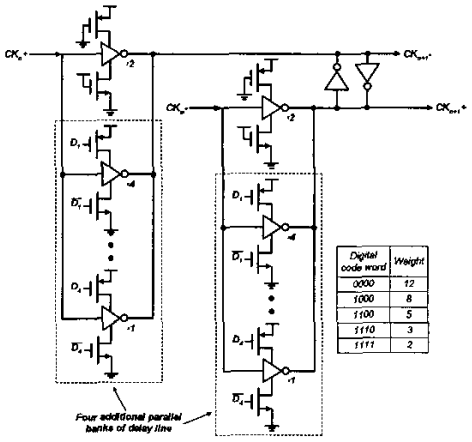

Fig. 7 The programmable delay line.

The delay line shown in Fig. 7 is based on simple CMOS inverter stages with weak cross-coupled inverters to minimize skew. The CMOS inverter delay element has lower power consumption than the delay element based on source-coupled differential pair. The loop control voltage V_{ctrl} can adjust the delay by varying the supply voltage of the delay line through linear regulator. Four additional parallel banks of delay line with different weights are placed around the main delay line for digital tuning. If the delay of the delay line needs to be large, the low-weighted digital control code word can be automatically selected to turn off the corresponding parallel delay line banks due to the operation of digital DLL. The change of delay from digital turning effectively reduces the required dynamic range of the loop control voltage and extends the operating frequency range of the DLL. This approach prevents the loop control voltage from being below 1 V and thus ensures low-jitter performance of the DLL over a wide operating frequency range.

3.4. Self-Feedback Level Shifter

Fig. 8 shows the schematic of the improved self-feedback level-shifter circuit. The output signals *CK+* and *CK-* from the supply regulated delay line only have the swings between loop control voltage V_{ctrl} and ground. A level shifter is used to convert the V_{ctrl} level signal to full V_{DD} level if a rail-to-rail clock is required. Conventional level-shifter circuit based on the current mirror amplifier topology consumes a lot of power and usually becomes most power-hungry part in the clock generator. The substantial reason is that the diode-connected devices M_5 and M_7 keep drawing static currents every half clock cycle. The PMOS switches M_9-M_{10} and M_{11}-M_{12}, which are controlled by the feedback level-shifted output clock signals *Out+* and *Out-*, are inserted in the current mirror amplifiers to eliminate this problem. These switches dynamically turn off the static current paths after one inverter delay time when the level-shifted output clock signals reach to V_{DD} level. The self-feedback technique effectively reduces the power consumption of the level-shifter circuit over the entire operating frequency 50% at least.

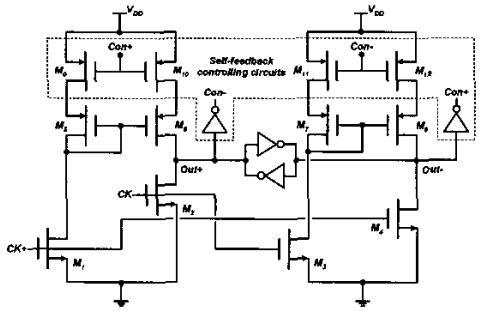

Fig. 8 Schematic of self-feedback level shifter.

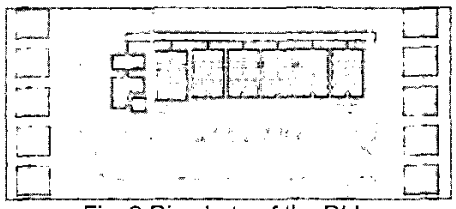

Fig. 9 Die photo of the DLL.

4. Experimental Results

The analog-digital dual-loop DLL has been designed and fabricated in a 0.18-μm CMOS technology. As shown in the die photo in Fig. 9, the DLL core area is 0.2 mm^2 (640 μm × 310 μm). The experimental results show that the DLL can operate in a frequency range from 25 to 250 MHz which corresponds to an output clock rate of 0.8 to 8 GHz with a 1.8-V supply. Fig. 10 depicts the measured transfer curve of the delay line, which consists of five partially overlapping sub-curves. The jitter performance of the DLL output at 125MHz is demonstrated in Fig. 11. The jitter histogram measures 2.1-ps rms and 14.9-ps peak-to-peak jitter characteristics with the loop control voltage V_{ctrl} 1.4 V and a digital control code word *1100*. In order to demonstrate the advantage of the dual-loop structure, the digital DLL is disabled and the digital control code word *1000* is set externally for comparison. The output rms jitter and peak-to-peak jitter would be increased to 2.9 ps and 21.6 ps respectively with the loop control voltage V_{ctrl} falling to 1.1 V, as demonstrated in

Fig. 12. Fig. 13 shows the measured rms jitter characteristics of the dual-loop DLL over different operating frequencies and corresponding digital control code words. The performance degradation at low operating frequency is due to clean low-frequency input reference clock not available especially below 45MHz. Table 1 summarizes the performance of the proposed DLL.

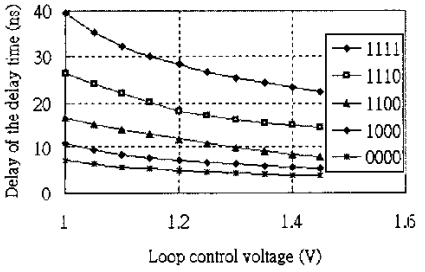

Fig. 10 Measured transfer curve of the delay line.

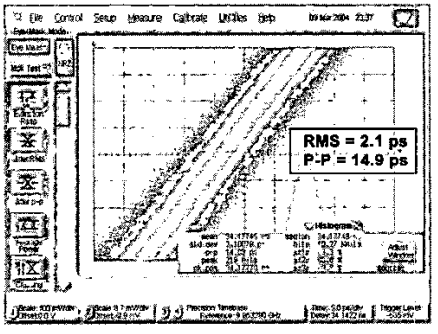

Fig. 11 DLL output jitter histogram at 125 MHz (analog V_{ctrl} = 1.1 V and digital control code *1100*).

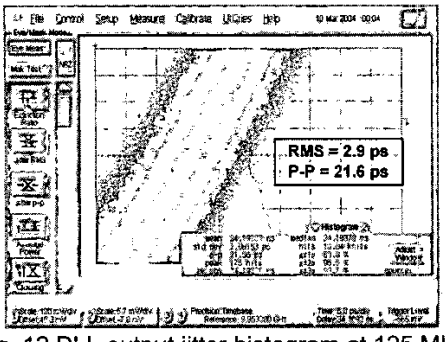

Fig. 12 DLL output jitter histogram at 125 MHz when the digital DLL is disabled (analog V_{ctrl} = 1.1 V and digital control code *1000*).

5. Conclusion

An analog-digital dual-loop adaptive-bandwidth DLL is proposed to achieve a low-jitter characteristic over a wide operating frequency range and across PVT variations. The deterministic jitters induced by the unnecessary ripples on the loop control line are eliminated by employing the complementary phase detector (PD). The level-shifter circuit reduces the power consumption over the entire operating frequency 50% at lest by using a self-feedback technique. The output multi-phase clocks of the DLL achieve an equivalent sampling clock rate spanning from 0.8 GHz to 8 GHz, which is sufficient for most UWB system applications. Because of the analog-digital dual-loop architecture, the proposed DLL can easily improve the performances such as operating frequency range and jitter characteristic with little extra hardware, which will benefit greatly from future scaling-down CMOS process.

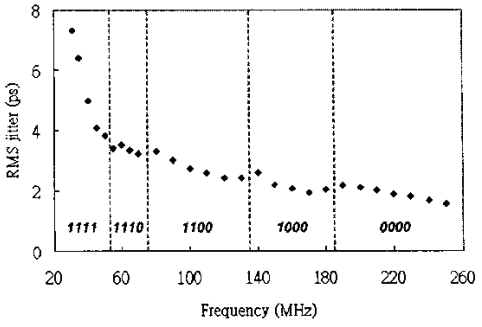

Fig. 13 Measured rms jitter characteristics of the DLL over different operating frequencies and corresponding digital control code words.

Table 1. Performance summary

Process	0.18-um 1P6M CMOS process
Operating voltage	1.8 V
Operating frequency range	25 MHz ~250 MHz
Output multi-phase clock rate	0.8 GHz ~ 8 GHz
RMS jitter	2.1 ps @ 125 MHz 1.6 ps @ 250 MHz
Peak-to-peak jitter	14.9 ps @ 125 MHz 12.1 ps @ 250 MHz
Power dissipation	1.6 mW @ 25 MHz 9.7 mW @ 250 MHz
Active area	0.2 mm^2

6. Acknowledgement

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