# DC-to-135 GHz SPST and 15-to-135 GHz SPDT Traveling Wave Switches Using FET-Integrated CPW Line Structure

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***Abstract* — High operation frequency SPST and SPDT switches based on commercial 0.15-μm GaAs pHEMT are developed. A novel integrated CPW line structure, which integrates the device, signal line and ground into the CPW line structure, is proposed. By using this structure, the limitation of the traveling wave switch caused by the parasitic inductance between the device to signal and ground in the conventional microstrip line designs can be removed. From the measurement results, high operation frequency of 135 GHz is achieved. The SPST switch achieves less then 5 dB insertion loss from DC to 135 GHz. The SPDT switch achieves less than 6 dB insertion loss from 15 GHz to 135 GHz. This switch has the highest operation frequency among the reported traveling wave switches.**

***Index Terms* — SPST, SPDT, CPW, pHEMT.**

## I. Introduction

In wireless communication, T/R switch plays a role to change the RF signal path to transmitter or receiver. Recently, switches using FET device become popular because they can be realized by the standard process and are easy to integrate with other active component such as power amplifier or low noise amplifier. For high frequency operation, the design concept of traveling wave shunt FET switch was proposed. In this design approach, the parasitic capacitance or inductance can be modeled as the low pass transmission line with specific impedance [1]. Because of the broadband frequency response, switches based on traveling-wave concept are reported [1]-[6]. For higher frequency over W-band, there exists the limitation by the parasitic inductance between the device to ground and signal line. One special HJFET process was proposed to overcome this problem [4], and demonstrated the operation frequency to 110 GHz. As for the standard process, the FET integrated transmission line was reported. The FET integrated transmission line eliminated the parasitic inductance between device and signal line the special the layout. However, there still exists the parasitic inductance between devices to ground caused by the via holes.

In this paper, a novel concept of FET integrated CPW line is proposed. By using the CPW transmission line, the inductance of via hole can be removed, and thus higher operation frequency can be achieved. A SPST and a SPDT switches are presented in this work and demonstrate good measured performance up to D-band, which is the highest operation frequency among the reported traveling wave switches [1]-[6].

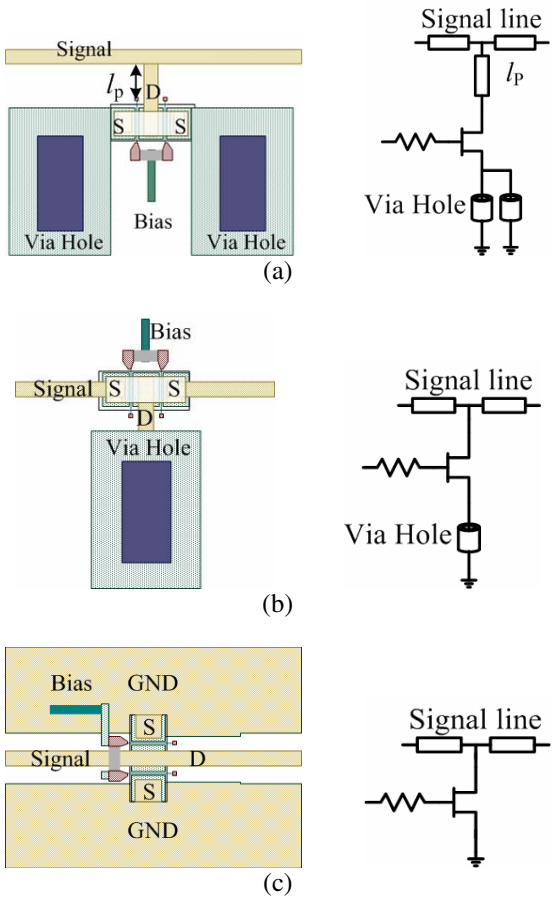
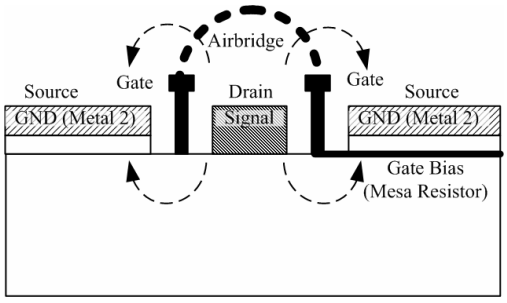



Fig. 1. Layout and the equivalent circuit of (a) conventional traveling wave switch, (b) FET integrated transmission line, and (c) FET integrated CPW line.

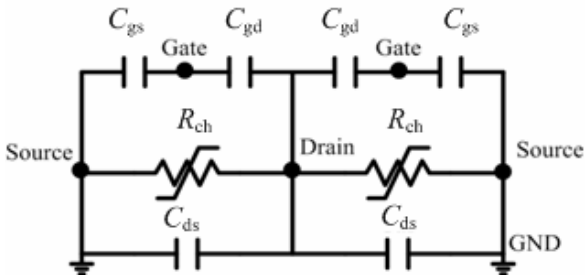
## II. FET Integrated CPW Line Concept

Fig. 1(a) is the layout and the equivalent circuit of a conventional FET traveling-wave switch. The switch is composed of two-finger common source shunt transistors and signal lines. There are one additional transmission line $l_p$ and two via holes due to the layout consideration. For the high frequency operation, $l_p$ becomes significant limitation for the insertion loss [6]. To overcome this problem, the traveling-wave switch using FET integrated transmission line was

proposed [6]. Fig. 1(b) shows the layout and the schematic of FET integrated transmission line. The signal line connects to the source of the device directly and $l_p$ can be eliminated. However, there still exists the via hole inductance, which will increase the insertion loss at high frequencies. The switch using integrated CPW line is shown in Fig. 1(c). A coplanar waveguide is realized based on the physical structure of the FET device as shown in Fig. 2(a). The signal line connects to the drain of the device and the source connects to the ground directly. This structure removes not only $l_p$, but also the via hole inductance. Fig. 2(b) is the equivalent circuit of the transistor. $R_{ch}$ is the channel resistor and varies with the gate to source voltage. The switches are controlled by changing the gate to source voltage. It is noted that there is no additional inductance between transistor to ground and signal, thus the bandwidth can be improved. The design consideration can be reduced to only $C_{gd}$, $C_{ds}$, $C_{gs}$ and $R_{ch}$. From Fig. 1(a) and Fig. 1(b), it is observed that the gate bias network in the conventional switch and the integrated FET transmission line switch is easily to be realized by a resistor because the signal line and the gate bias network is separated by the transistor. For the integrated CPW transmission line, the gate bias network is close to the drain and the source, therefore the bias network must go through the ground. As shown in Fig. 2(a), two gates are connected by the airbridge and the high resistance mesa resistor on a different layer from the ground is used for the bias circuit.




(a)

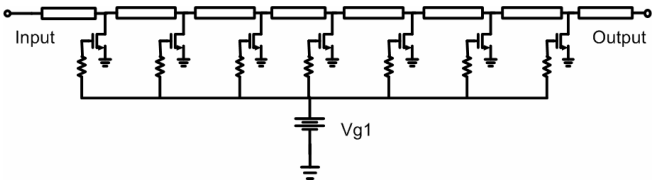



(b)

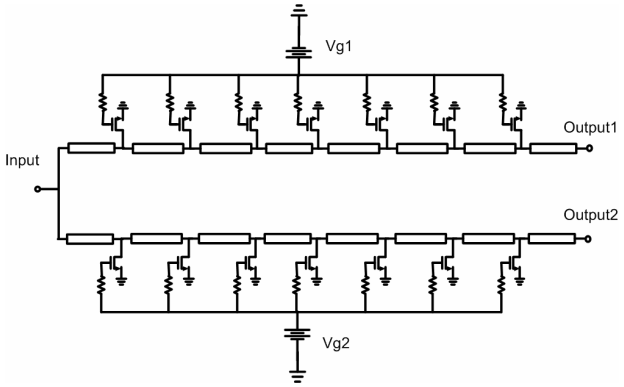
Fig. 2. (a) The profile of a transistor structure. (b) The equivalent circuit of this transistor.

## III. Device Characteristic and MMIC Process

The process used in this design is WIN's 0.15-μm high linearity AlGaAs/InGaAs/GaAs pHEMT MMIC process. The HEMT device has a typical unit current gain cutoff frequency ($f_T$) of higher than 85 GHz and maximum oscillation frequency ($f_{max}$) of greater than 120 GHz at 1.5-V drain bias, with a peak dc transconductance ($G_m$) of 495 mS/mm. The gate-drain breakdown voltage is 10 V, and the gate to source voltage at peak transconductance at 1.5-V drain-source voltage is -0.45 V. This MMIC process also includes thin-film resistors, MIM capacitors, spiral inductors, and air-bridges. The wafer is thinned to 4 mil for the gold plating of the backside and reactive ion etching via holes are provided.




(a)




(b)

Fig. 3. (a) Circuit topology of the SPST switch (b) Circuit topology of the SPDT switch.

## IV. Circuit Design

Fig. 3(a) is the complete schematic of the SPST traveling wave switch, which is composed of 7 common source transistors and high impedance transmission lines. For the realization of the FET integrated CPW line, 2-finger transistors were chosen. The finger width of each transistor was determined by the trade off between bandwidth and insertion loss [1]. The length and the impedance of the transmission line are selected by the design procedure reported in [1]. The transistors exhibit a shunt capacitor when the gate voltage is -2 V as the switch turns on. On the other hand, the

TABLE I
RECENTLY REPORTED PERFORMANCE OF MILLIMETER-WAVE SWITCHES USING TRAVELING-WAVE CONCEPT

| Device | Frequency (GHz) | Insertion loss (dB) | Isolation (dB) | I/O | Chip size ($mm^2$) | Ref. |
|---|---|---|---|---|---|---|
| HEMT | 15-80 | <3.6 | >25 | SPDT | 1.5x1.5 | [1] |
| HEMT | DC-60 | <3 | >24 | SPDT | 1x1 | [1] |
| HEMT | DC-80 | <3 | >24 | SPST | 1x0.75 | [1] |
| MESFET | 20-40 | <2 | >23 | SPDT | 1.25x1.25 | [2] |
| MESFET | DC-40 | <3 | >23 | SPDT | 0.84x1.27 | [2] |
| HEMT diode | 23-78 | <4 | >25 | SPDT | 1.65x1.33 | [3] |
| HJFET | DC-110 | <2.55 | >22.2 | SPST | 0.85X0.45 | [4] |
| HEMT | 15-50 | <3.1 | >40 | SPDT | 1.5x2 | [5] |
| HEMT | 40-85 | <2 | >30 | SPDT | 1.45x1 | [6] |
| **HEMT** | **15-110 DC-135** | **<4 <5** | **>25 >15** | **SPST** | **1.64x0.42** | **This work** |
| **HEMT** | **20-110 15-135** | **<5 <6** | **>23 >20** | **SPDT** | **1.35x0.5** | **This work** |

transistors provide shunt resistors to ground when the gate voltage is 0 V.

Fig. 3(b) is the complete schematic of the SPDT traveling wave switch consisting of two SPST switches and quarter wave length transformers are included. The low-end operation frequency is limited by the quarter wavelength transmission line.

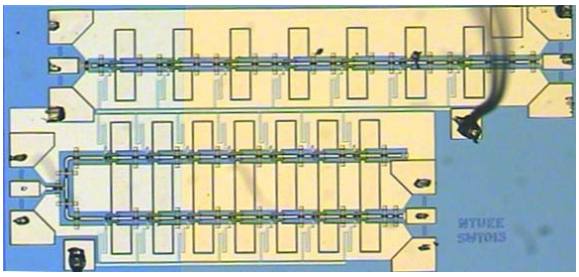


Fig. 4. Die Photo of the SPST and SPDT switch.

For the single mode operation of CPW line, air bridges are used to suppress the odd mode of the CPW line. Via holes are placed between top and bottom ground plane to prevent the parallel plate mode. All the distributed elements are characterized by the 3D full wave EM simulation [7]. Fig. 4 shows the die photo for both the SPST and SPDT switches, with the total chip size of $2 \times 1$ $mm^2$. On the top of the photograph is the SPST switch, which is $1.64 \times 0.42$ $mm^2$. The SPDT switch occupies the bottom of the chip with a chip size of $1.35 \times 0.5$ $mm^2$. For on-wafer testing consideration, since two GSG probes cannot be placed on the same side of the SPDT chip, the second output port was terminated by the 50-Ω termination.

## V. MEASUREMENT RESULTS

The SPST and SPDT switches are measured by on wafer test. Four different frequency ranges (45 MHz to 50 GHz, V-band, W-band, and D-band) are measured by the network analyzer with different test sets.

Fig. 5 presents the measured and simulated results of the SPST switch. The SPST switch achieves an insertion loss of 2.5 dB at 75 GHz, 4.1 dB at 110 GHz and 5.0 dB at 135 GHz respectively. It also achieves an isolation of more than 30 dB. Fig. 6 shows the performance of the SPDT switch. It achieves an insertion loss of 4.1 dB at 75 GHz, 5 dB at 110 GHz and 6 dB at 135 GHz, respectively. The isolation of the SPDT switch is also higher than 30 dB from 40 GHz to 135 GHz. The measurements agree with the simulation results well.

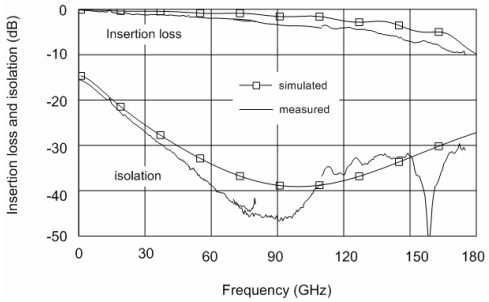



Fig. 5. The measurement and simulation results of insertion loss and isolation of the SPST switch.

Table I lists the previously reported switches by using traveling wave concept. It can be observed that the operation

frequency is limited below 100 GHz except [4]. In [4], the problem of the parasitic inductance was eliminated by the special process of HJFET. In [6], the high frequency performance is achieved by the integrated FET transmission line structure, but the limitation of the via hole inductance still exists. The advantage of chip size of our new integrated FET CPW line structure can also be observed in Table I. Because of no additional via holes or transmission lines for the connections between devices and the signal lines, compact chip sizes of $1.64 \times 0.42$ mm$^2$ and $1.35 \times 0.5$ mm$^2$ are achieved for the SPST and SPDT switches, respectively.

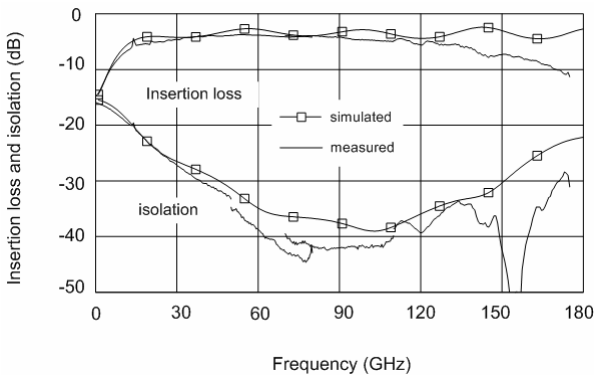



Fig. 6. The measurement and simulation results of insertion loss and isolation of the SPDT switch.

## VI. Conclusion

In this paper, a new integrated FET CPW line structure is presented. By using this structure, the parasitic inductance between device to signal line and ground can be removed, and thus the operation frequency can be achieved. The SPST switch exhibits less than 5 dB measured insertion loss and larger than 15 dB isolation from DC to 135 GHz. The SPDT switch gets less than 6 dB insertion loss and larger than 25 dB isolation from 15 GHz to 135 GHz. To our knowledge these circuit demonstrated the highest operation frequency among the reported traveling wave switches [1]-[6].

## Acknowledgement

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