行政院國家科學委員會補助專題研究計畫成果報告

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※ 磷化銦鎵 HFET MMIC 製程(2/3) ※

※ GaInP HFET MMIC processing ※

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計畫類別：□個別型計畫 □整合型計畫

計畫編號：NSC 88－2219－E－002－023

執行期間：88 年 8 月 1 日至 89 年 7 月 31 日

計畫主持人：呂學士 國立台灣大學電機系

共同主持人：

本成果報告包括以下應繳交之附件：

□赴國外出差或研習心得報告一份

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□出席國際學術會議心得報告及發表之論文各一份

□國際合作研究計畫國外研究報告書一份

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中 華 民 國 88 年 8 月 31 日

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主持人：呂學士　國立台灣大學電機系

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一、中文摘要

為了電晶體達到更高的截止頻率(f_T)、最大振盪頻率(f_{max})，以及較低的雜音指數(noise figure)，我們需要減少電晶體閘極的長度，及減低閘極端的電阻。因此，如何在縮小閘極長度的同時，也能一併降低閘極電阻，便成了決定電晶體優劣的關鍵因素。基於上述兩點考量，T 型(或蘑菇型) 的閘極便被廣泛應用在現今的次微米元件之中。本年度的研究目標就是將上年度次微米 T 型閘極的製作方法應用到實際的元件製作。由實驗結果顯示，我們在沒有昂貴的電子束曝光機的幫助下，僅利用傳統的 UV 光阻微影術，便可做出具有次微米線寬之 T 型閘極之元件。

Abstract

It is well known that the gate length of a FET has to be reduced in order to achieve a higher current gain cut-off frequency (fT). However, it is also necessary to keep the gate resistance low enough to maintain a high maximum oscillation frequency (fmax) and a low noise figure. Therefore, T gates are widely used in the submicron FETs, which are usually fabricated by expensive and time-consuming technologies, such as electron beam or deep ultra violet (UV) lithography [1] [2] [3] [4]. In this report, we propose a much less expensive technology for the fabrication of submicron T gates by using the flowing property of normal UV photoresist.

二、緣由與目的

In order to achieve a higher current gain cut-off frequency (f_T), it is taken for granted that the gate length of a FET has to be reduced essentially. On the other hand, it is also necessary to keep the gate resistance low enough to maintain a high maximum oscillation frequency (fmax) and a low noise figure. Therefore, the T-shape gates, which can meet these both requirements at the same time, are widely used in the submicron FETs.

However, the technologies of fabricating T gates, such as electron beam and deep ultra violet (UV) lithography, are very expensive and time-consuming, In view of this, we propose a much less expensive technology for the fabrication of submicron T gates by using the flowing property of normal UV photoresist. In this report, a HEMT device with a submicron T gate was fabricated by the proposed method, and the submicron property of T gate was verified by measuring the high frequency performance of this device.

三、研究方法與成果

The fabrication technique of sub-micron T gates by re-flowed photo-resist has been developed last year (the first year of the project) and is detailed here as follows with reference to Fig.1(a) through Fig.1(d).

First, 1 μm opening was defined by normal lithography as shown in Fig.1(a). The normal UV resist then flowed because of heat treatment and as a result the opening shrunk (see Fig.1(b)). The gate length was determined by the shrunk opening, which could be controlled by the baking temperature and baking time. Deep UV resist was spun on the flowed resist followed by a flood exposure to a deep UV source. A top opening was developed by normal lithography after the application of the second normal UV resist on the deep UV resist. The exposed deep UV resist was then developed to obtain the desirable undercut for T shape gate and for lift-off (Fig. 1(c)). Finally, the submicron T gate was formed after gate metal deposition and lift-off process as shown in Fig. 1(d).

This year (the second year of the project) we have applied the sub-micron T gate technique developed last year to the fabrication of HEMTs. Conventional optical lithography and mesa type wet etching technique has been combined with the sub-micron T gate technology in the fabrication of FETs.

四、結果與討論

The experimental profile of the trilayer resist for the fabrication of the submicron T gate structure is shown in Fig. 2. Note that the undercut profile is visible and desirable. The top opening of the resist profile of the T-shape gate is 3μm. In Fig. 3 the T-shape gate formed after lift-off process is shown. The footprint of T-gate is about 0.8μm and the top opening of T-gate is 6μm. The DC common-source characteristics of the fabricated HEMT are shown in Fig. 4(a). Clearly, Imax of 430mA/mm and Idss of 200mA/mm are obtained. A peak transconductance (gm) of 315mS/mm were also achieved at Vds = 2 V and Vgs = 0 (see Fig. 4(b)).

The results of microwave on-wafer S-parameters measurement showed that the current gain cut-off frequency (f_t) and maximum oscillation frequency (f_{max}) were 21.6 and 26 GHz , respectively, under the bias condition of Vgs = -0.05V and Vds = 2V. The value of f_T we obtained, when compared with typical values (16-18GHz) from the 1 μm HEMT devices [5-6], demonstrated unequivocally that sub-micron performance has been achieved from our sub-micron devices. Recent results of ft (28GHz) and fmax (32 GHz) from 0.6 μm devices have also been achieved. More efforts are being put to push for deep sub-micron devices..

五、計畫成果自評

We have developed a novel method to fabricate sub-micron T gate FETs. This method is superior to the traditional techniques such as e-beam or deep UV lithography in terms of cost and time. We are applying a patent concerning about the sub-micron T gate by re-flowed resist we developed. Two IEEE journal papers (Transactions on Microwave Theory and Technology) and one conference paper (Asian Pacific Microwave Conference) were also generated because of the support of this project. Therefore we believed that we have done a very good job and we are grateful for the continued support from NSC.

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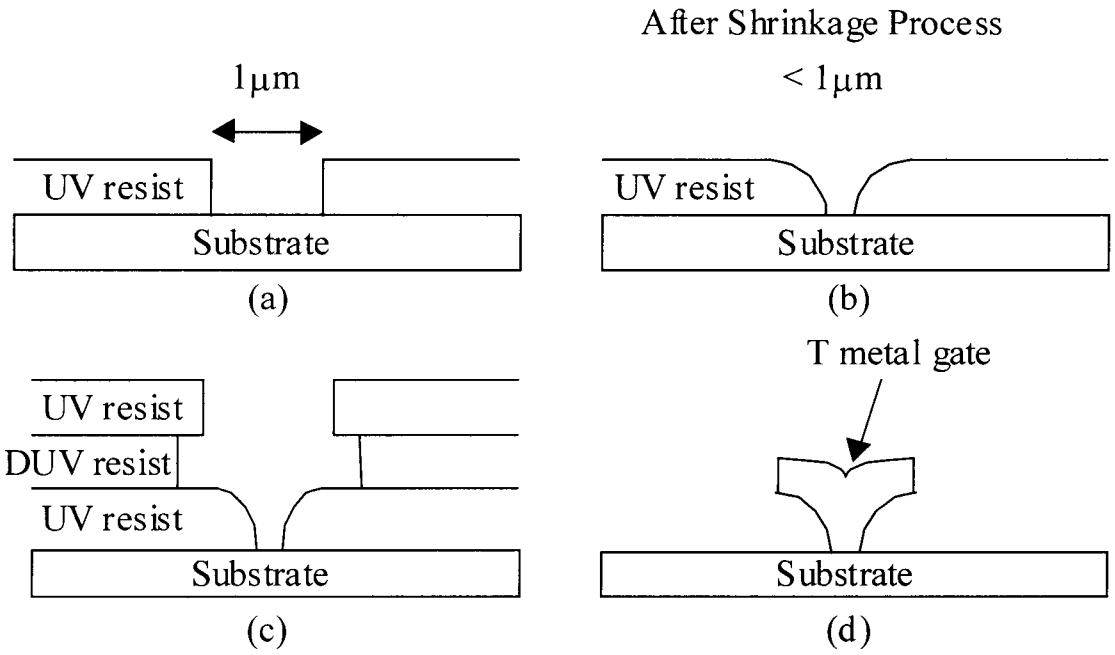


Fig. 1. Fabrication steps for a submicron T gate structure.

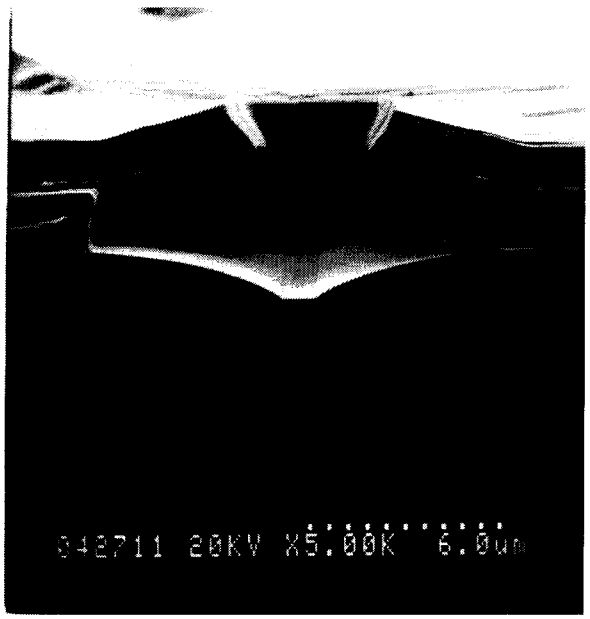
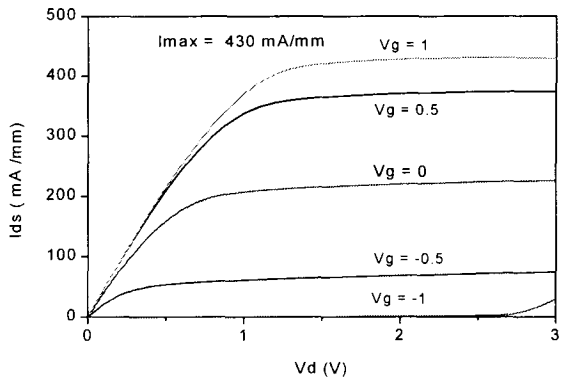
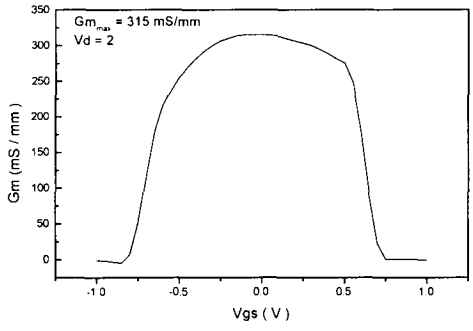


Fig. 2. The profile of the trilayer resist for the submicron T gate.

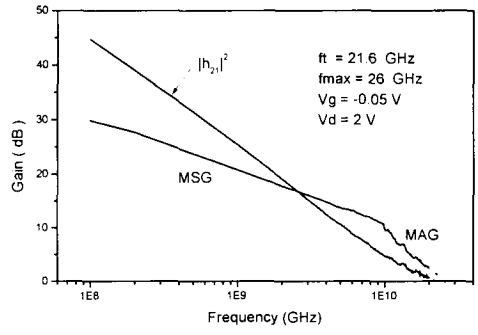
Fig . 3. The fabricated submicron T-gate on GaAs substrate. The footprint is 0.8μm.



(a)



(b)



(c)

Fig. 4 DC characteristics and Microwave characteristics of a HEMT device. (a) Common –source I-V chracteristics; (b) transconductance; (c) power gain and current gain.