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行政院國家科學委員會補助專題研究計畫成果報告

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※ 磷化銦鎵 HFET MMIC 製程(1/3~3/3)

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※ GaInP HFET MMIC processing ※

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計畫類別：□個別型計畫 □整合型計畫

計畫編號：NSC 87－2219－E－002－009

NSC 88－2219－E－002－023

NSC 89－2219－E－002－044

執行期間：87 年 8 月 1 日至 90 年 7 月 31 日

計畫主持人：呂學士 國立台灣大學電機系

共同主持人：

本成果報告包括以下應繳交之附件：

□赴國外出差或研習心得報告一份

□赴大陸地區出差或研習心得報告一份

□出席國際學術會議心得報告及發表之論文各一份

□國際合作研究計畫國外研究報告書一份

執行單位：台灣大學

中華民國 90年 10月 5日

行政院國家科學委員會專題研究計畫成果報告

砷化銦鎵 HFET MMIC 製程(1/3)
GaInP HFET MMIC processing

計畫編號：NSC 87-2219-E-002-009
執行期限：87年 8月1日 至88年 7月31日
主持人：呂學士　國立台灣大學電機系

一、中文摘要

為了要使電晶體有更高的增益與電流密度，縮小閘極長度並同時降低閘極電阻是必要的。因此，T型(或蘑菇型)次微米閘極元件的製作勢在必行。本年度的研究目標就是在探討次微米T型閘極的製作方法。我們利用光阻加熱流動的特性以及三層光阻的結構，設計了一套次微米T型閘極的製程步驟，並且以實驗驗證其可行性。結果顯示，在不需要昂貴的電子束曝光機的條件之下，我們利用傳統的 UV 光阻亦可做出具有深次微米線寬之T型閘極。

Abstract

For more power gain and current density, shrinking gate length but at the same time decreasing gate resistance is essential. The T shape submicron gate is the most effective way to meet both requirements. In this year, our research is focused on the fabrication of the T-shape submicron gate by photoresist reflowing method. Using the flowing property of photoresist under enough high temperature and tri-layer photoresist structure, we have formed the submicron T-gate without resorting to the E-beam or X-ray lithography.

二、計畫緣由與目的

With shorter gate length, better high frequency performance of a GaAs FET can be obtained in conjunction with other optimization in device structure and processing steps. However, a small gate resistance must be attained as well so that the enhanced device performance achieved by shorter gate length will not be deteriorated by the increase of the gate resistance. Usually, the smallest line width one can obtain by the traditional contact-mode I-line lithography is about 0.8um. In order to fabricate shorter gate length, some special techniques have to be used. In this project, we proposed to use the reflow property of photoresist to achieve the goal.

三、研究方法與成果

By making use of the reflow property of photoresist, we have developed a method to realize a T-shape submicron gate length. It involves a postbake process of a tri-layer photoresist structure. This postbake process was performed on a ordinary hotplate and by

critical control of this thermal process, a short line width pattern scaled down to 0.15μm has been made. Figures 1&2 showed the results of the reflowed photoresists.

After this postbake process, the first layer profile of a tri-layer photoresist structure was formed. Then the second layer and the third layer were spun on it sequentially and finally 2um wide top open window was formed by normal optical lithography process in order to realize a mushroom shape cavity in the tri-layer photoresist structure which also helped facilitate the lift-off process. Figure 3 illustrates the schematic diagram of the complete submicron T-gate structure. Also shown is the scanning electron microscope (SEM) photographs our fabricated submicron T-gate (see figure 4).

四、結果與討論

In this project, we were trying to realize submicron T-gates and have solved many problems we met. The biggest obstacle is the intermixing problem between PMMA and third layer photoresist. We have tried to get rid of it by R.I.E., but it seemed to be a more complex process. Therefore, we tried to solve this problem by putting a metal barrier between the second PMMA and the third S1813 layer. Titanium and Germanium have been used for this process but the barrier layer seemed to be wrinkled and cracked after subsequent soft-bake process. Finally, we found that Au was free of this kind of problem and therefore the tri-layer process become more reliable and repeatable.

Through precise control of the baking temperature and exposing time, we not only could realize submicron gates but also could fabricate any required gate length with high uniformity and reliability. Armed with the submicron-gate technology, we are planning to fabricate FET's with mushroom gate structures in the second year project. Better performance in terms of power gain and bandwidth are expected.

五、計畫成果自評

By using the novel tri-layer photoresist method, we demonstrated that a submicron T-gate could be fabricated with much cheaper traditional mask alignment system compared to E-beam or X-ray lithography process. Our method is suitable for mass production. We also have published 1 EDL, 1 TED and 1 JAP papers supported by this project. In short, we are very proud of and satisfied by the results we achieved in this year.

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4. G. M. Metze, etc. "A dielectric-defined process for the formation of T-gate

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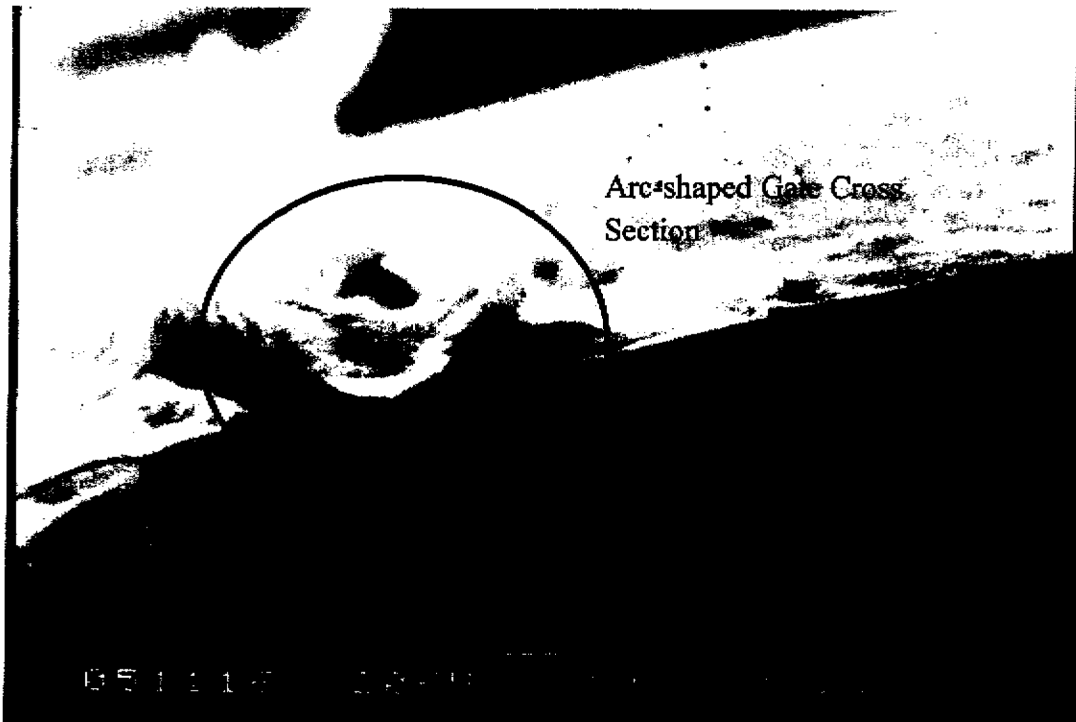


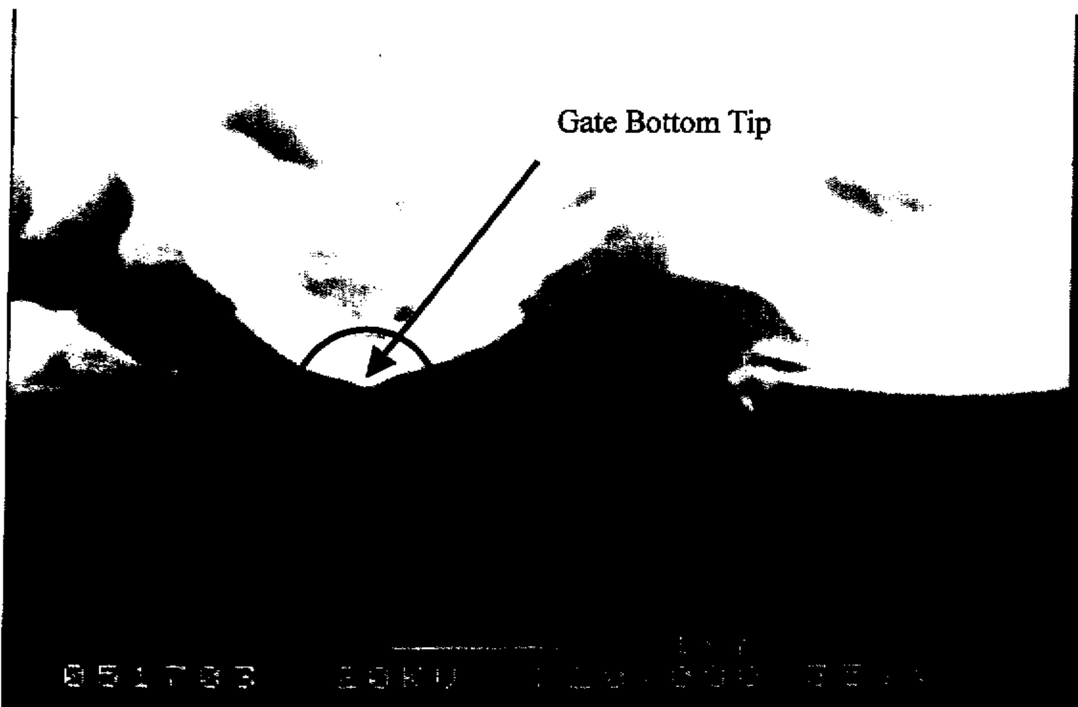


Fig.4 SEM photograph of T-gate Cross Section.

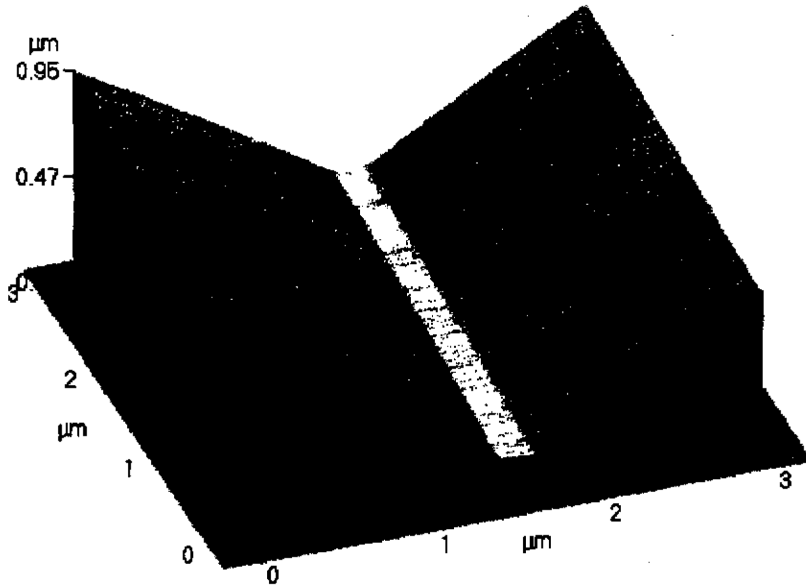
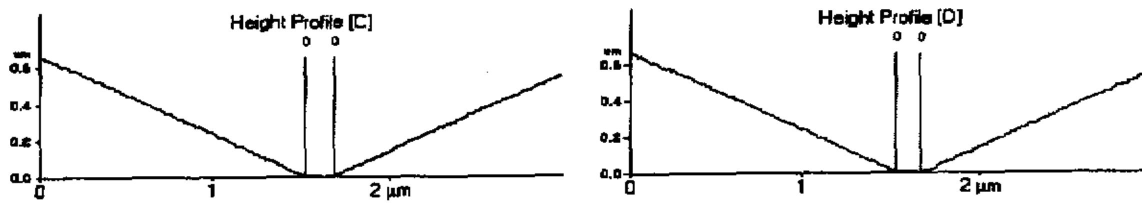


Fig. 1 The picture of reflowed photoresist by atomic force microscope (AFM) with 3µmx 3µm square area.



Line	Distance
[A]	0.153µm
[B]	0.141µm

Fig. 2 Two arbitrary cross sections of a reflowed photoresist measured by atomic force microscope (AFM).

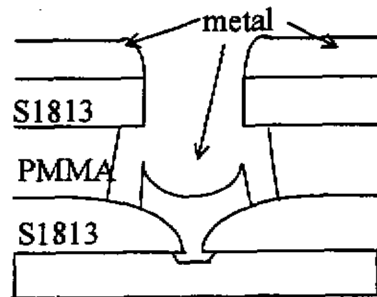


Fig. 3 The structure of submicron T-gate by tri-level normal UV photoresist.

行政院國家科學委員會專題研究計畫成果報告

磷化銦鎵 HFET MMIC 製程(2/3)

GaInP HFET MMIC processing

計畫編號：NSC 88-2219-E-002-023

執行期限：88 年 8 月 1 日 至 89 年 7 月 31 日

主持人：呂學士　國立台灣大學電機系

共同主持人：

計畫參與人員：廖光仁　國立台灣大學電機所

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涂欣元　國立台灣大學電機所

一、中文摘要

為了電晶體達到更高的截止頻率(f_T)、最大振盪頻率(f_{max})，以及較低的雜音指數(noise figure)，我們需要減少電晶體閘極的長度，及減低閘極端的電阻。因此，如何在縮小閘極長度的同時，也能一併降低閘極電阻，便成了決定電晶體優劣的關鍵因素。基於上述兩點考量，T 型(或蘑菇型 ）的閘極便被廣泛應用在現今的次微米元件之中。本年度的研究目標就是將上年度次微米 T 型閘極的製作方法應用到實際的元件製作。由實驗結果顯示，我們在沒有昂貴的電子束曝光機的幫助下，僅利用傳統的 UV 光阻微影術，便可做出具有次微米線寬之 T 型閘極之元件。

Abstract

It is well known that the gate length of a FET has to be reduced in order to achieve a higher current gain cut-off frequency (fT). However, it is also necessary to keep the gate resistance low enough to maintain a high maximum oscillation frequency (fmax) and a low noise figure. Therefore, T gates are widely used in the submicron FETs, which are usually fabricated by expensive and time-consuming technologies, such as electron beam or deep ultra violet (UV) lithography [1] [2] [3] [4]. In this report, we propose a much less expensive technology for the fabrication of submicron T gates by using the flowing property of normal UV photoresist.

二、緣由與目的

In order to achieve a higher current gain cut-off frequency (f_T), it is taken for granted that the gate length of a FET has to be reduced essentially. On the other hand, it is also necessary to keep the gate resistance low enough to maintain a high maximum oscillation frequency (fmax) and a low noise figure. Therefore, the T-shape gates, which can meet these both requirements at the same time, are widely used in the submicron FETs.

However, the technologies of fabricating T gates, such as electron beam and deep ultra violet (UV) lithography, are very expensive and time-consuming, In view of this, we propose a much less expensive technology for the fabrication of submicron T gates by using the flowing property of normal UV photoresist. In this report, a HEMT device with a submicron T gate was fabricated by the proposed method, and the submicron property of T gate was verified by measuring the high frequency performance of this device.

三、研究方法與成果

The fabrication technique of sub-micron T gates by re-flowed photo-resist has been developed last year (the first year of the project) and is detailed here as follows with reference to Fig.1(a) through Fig.1(d).

First, 1 μm opening was defined by normal lithography as shown in Fig.1(a). The normal UV resist then flowed because of heat treatment and as a result the opening shrunk (see Fig.1(b)). The gate length was determined by the shrunk opening, which could be controlled by the baking temperature and baking time. Deep UV resist was spun on the flowed resist followed by a flood exposure to a deep UV source. A top opening was developed by normal lithography after the application of the second normal UV resist on the deep UV resist. The exposed deep UV resist was then developed to obtain the desirable undercut for T shape gate and for lift-off (Fig. 1(c)). Finally, the submicron T gate was formed after gate metal deposition and lift-off process as shown in Fig. 1(d).

This year (the second year of the project) we have applied the sub-micron T gate technique developed last year to the fabrication of HEMTs. Conventional optical lithography and mesa type wet etching technique has been combined with the sub-micron T gate technology in the fabrication of FETs.

四、結果與討論

The experimental profile of the trilayer resist for the fabrication of the submicron T gate structure is shown in Fig. 2. Note that the undercut profile is visible and desirable. The top opening of the resist profile of the T-shape gate is 3μm. In Fig. 3 the T-shape gate formed after lift-off process is shown. The footprint of T-gate is about 0.8μm and the top opening of T-gate is 6μm. The DC common-source characteristics of the fabricated HEMT are shown in Fig. 4(a). Clearly, Imax of 430mA/mm and Idss of 200mA/mm are obtained. A peak transconductance (gm) of 315mS/mm were also achieved at Vds = 2 V and Vgs = 0 (see Fig. 4(b)).

The results of microwave on-wafer S-parameters measurement showed that the current gain cut-off frequency (f_t) and maximum oscillation frequency (f_{max}) were 21.6 and 26 GHz , respectively, under the bias condition of Vgs = -0.05V and Vds = 2V. The value of f_T we obtained, when compared with typical values (16-18GHz) from the 1 μm HEMT devices [5-6], demonstrated unequivocally that sub-micron performance has been achieved from our sub-micron devices. Recent results of ft (28GHz) and fmax (32 GHz) from 0.6 μm devices have also been achieved. More efforts are being put to push for deep sub-micron devices..

五、計畫成果自評

We have developed a novel method to fabricate sub-micron T gate FETs. This method is superior to the traditional techniques such as e-beam or deep UV lithography in terms of cost and time. We are applying a patent concerning about the sub-micron T gate by re-flowed resist we developed. Two IEEE journal papers (Transactions on Microwave Theory and Technology) and one conference paper (Asian Pacific Microwave Conference) were also generated because of the support of this project. Therefore we believed that we have done a very good job and we are grateful for the continued support from NSC.

六、參考文獻

1. Kazumi Nishimura, etc., " High performance 0.1-um-self-aligned-gate GaAs MESFET technology," *IEEE Trans. Electron Devices*, vol. 44, pp.2113, 1997.
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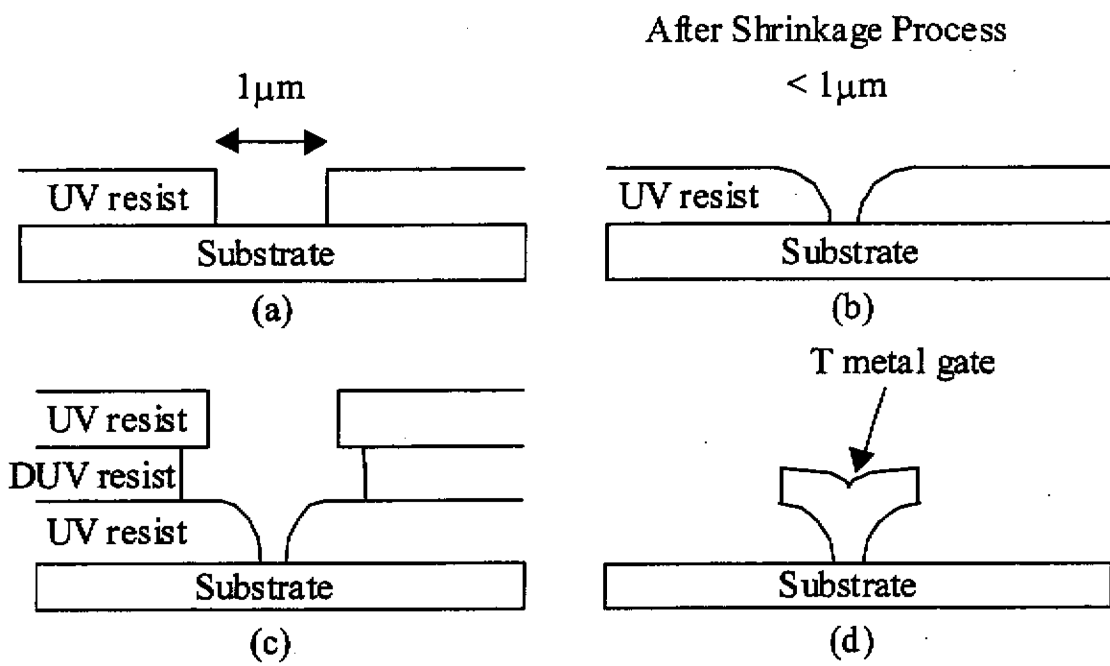


Fig. 1. Fabrication steps for a submicron T gate structure.

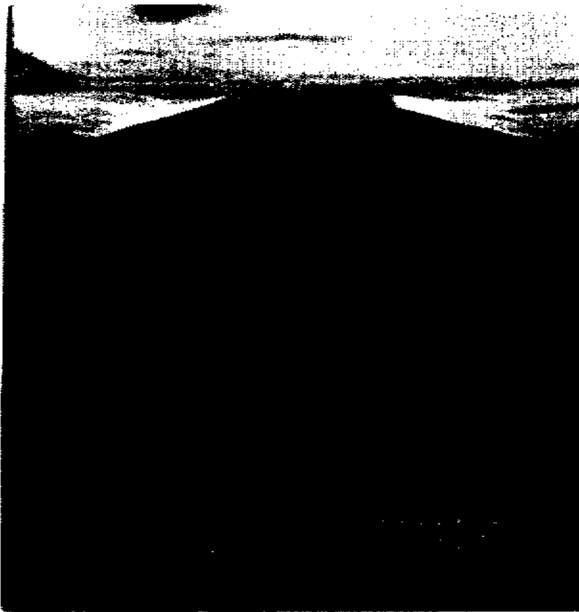


Fig. 2. The profile of the trilayer resist for the submicron T gate.

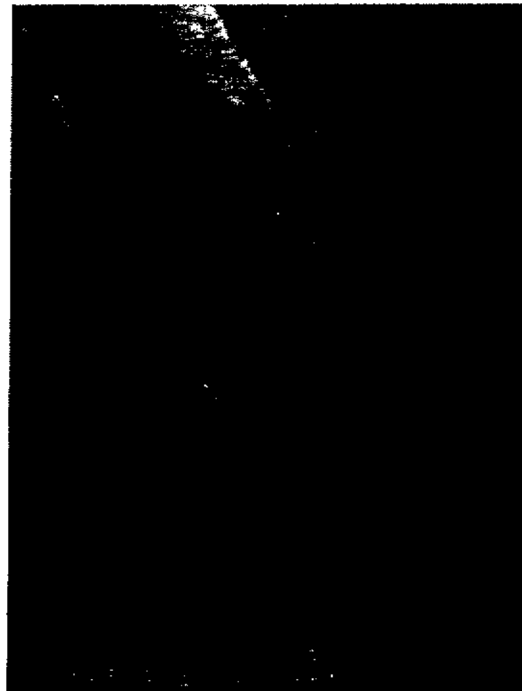
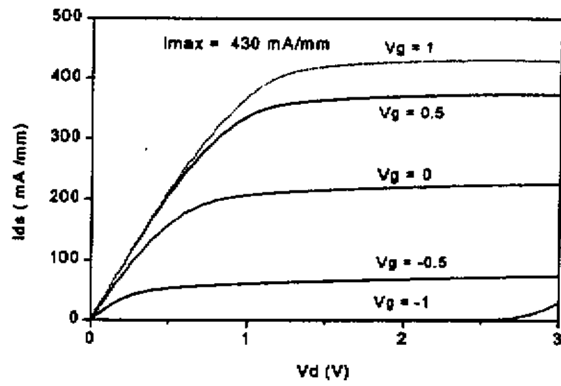
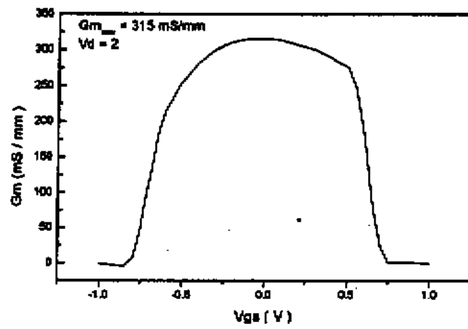


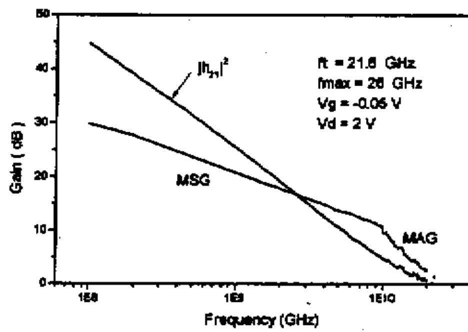
Fig . 3. The fabricated submicron T-gate on GaAs substrate. The footprint is 0.8μm.



(a)



(b)



(c)

Fig. 4 DC characteristics and Microwave characteristics of a HEMT device. (a) Common –source I-V chracteristics; (b) transconductance; (c) power gain and current gain.

行政院國家科學委員會專題研究計畫成果報告

磷化銦鎵 HFET MMIC 製程(3/3)

GaInP HFET MMIC processing

計畫編號：NSC 89-2219-E-002-044

執行期限：89年 8月1日 至90年 7月31日

主持人：呂學士　國立台灣大學電機系

共同主持人：

計畫參與人員：潘宣佑　國立台灣大學電機所

涂欣元　國立台灣大學電機所

一、中文摘要

為了電晶體達到更高的截止頻率(f_T)、最大振盪頻率(f_{max})，以及較低的雜音指數(noise figure)，我們需要減少電晶體閘極的長度，及減低閘極端的電阻。因此，如何在縮小閘極長度的同時，也能一併降低閘極電阻，便成了決定電晶體優劣的關鍵因素。基於上述兩點考量，T 型(或蘑菇型) 的閘極便被廣泛應用在現今的次微米元件之中。由實驗結果顯示，我們在沒有昂貴的電子束曝光機的幫助下，僅利用傳統的 UV 光阻微影術，便可做出具有次微米線寬之T型閘極之元件。本年度研究目標就是以次微米線寬之T型閘極異質場效電晶體為主動元件，設計並製造出工作在 28GHz 的 MMIC 功率放大器。

Abstract

It is well known that the gate length of a FET has to be reduced in order to achieve a higher current gain cut-off frequency (f_T). However, it is also necessary to keep the gate resistance low enough to maintain a high maximum oscillation frequency (f_{max}) and a low noise figure. Therefore, T-gates are widely used in the submicron FETs, which are usually fabricated by expensive and time-consuming technologies, such as electron beam or deep ultra violet (UV) lithography [1] [2] [3] [4]. We have proposed a much less expensive technology for the fabrication of submicron T-gates by using the flowing property of normal UV photoresist. In this report, We also successfully designed a 28GHz MMIC power amplifier.

二、緣由與目的

In order to achieve a higher current gain cut-off frequency (f_T), it is taken for granted that the gate length of a FET has to be reduced essentially. On the other hand, it is also necessary to keep the gate resistance low enough to maintain a high maximum oscillation frequency (f_{max}) and a low noise figure. Therefore, the T-shape gates, which can meet these both requirements at the same time, are widely used in the submicron FETs.

However, the technologies of fabricating T-gates, such as electron beam and deep ultra violet (UV) lithography, are very expensive and time-consuming, In view of this, we propose a much less expensive technology for the fabrication of submicron T gates by using the flowing property of normal UV photoresist. In this report, a HEMT device with a submicron T gate was fabricated by the proposed method, and the submicron property of T-gates was verified by measuring the high frequency performance of this device. We also successfully designed a 28GHz MMIC power amplifier.

三、研究方法與成果

The fabrication technique of

sub-micron T gate formation is detailed as follows. Initially, 1 μm opening was defined by normal lithography and then a rapid heat treatment by rapid thermal annealing (RTA) was use to flow and shrink the normal UV resist opening. The heating temperature and duration control the opening shrinkage and thus desired gate length. Then, a thick layer of deep UV PMMA resist was spun on flowed resist and followed by a flood exposure to a deep UV source. A thin layer of gold metal was evaporated on the top of the deep UV resist and followed by a normal UV resist. The gold metal layer is ~0.1 μm so that the alignment key on the substrate is still visible. The softness of gold metal eliminates any wrinkle and cracking problems caused by heating in the photolithography and metal evaporation processing. The thin layer of metal is used to prevent the formation of an intermixing layer between normal and deep UV resists during the resist baking process[5]. The intermixing layer can cause difficulties in the subsequent resist developing processing. Then 3 μm opening was developed on the second normal UV resist by a realignment technique. The thin layer metal was removed by wet chemical etching and the exposed UV PMMA resist was the developed by chlorobenzene or toluene to obtain the desirable trilayer resist profile, shown in Fig 1, for T-shaped gate and lift-off. Finally, the submicron T-gate shown in Fig. 2 was formed after gate metal deposition and lift-off process. The footprint of the T-gate is ~0.4 μm and the top opening of T-gate is 3 μm.

四、結果與討論

The proposed submicron T-gate technique combined with conventional optical lithography and mesa-type wet etching has been successfully applied to the fabrication of 0.4 μm GaInP HFETs. The results of microwave on-wafer S-parameters measurement are shown in Fig. 3. The current gain cut-off frequency (f_T) and maximum oscillation frequency (f_{max}) were 45GHz and 70GHz respectively, under the bais condition of Vgs=-2.2V, Vds=3.5V.Fig 4. illustrates the cut-off frequency against gate length by the resist flowing technology. The MMIC power amplifier with gate width =300μm we designed (chip layout shown in Fig 5) exhibited an experimental saturation output power of 20.6dBm at 28GHz as shown in Fig 6, which meets the goal (20dBm) of this project.

五、計畫成果自評

We have developed a novel method to fabricate sub-micron T gate FETs. This method is superior to the traditional techniques such as e-beam or deep UV lithography in terms of cost and time. We are applying a patent concerning about the sub-micron T gate by re-flowed resist we developed. One IEEE journal paper (Electron Device Letter) and one IEE Electronics Letter were also generated because of the support of this project. Therefore we believed that we have done a very good job and we are grateful for the continued support from NSC.

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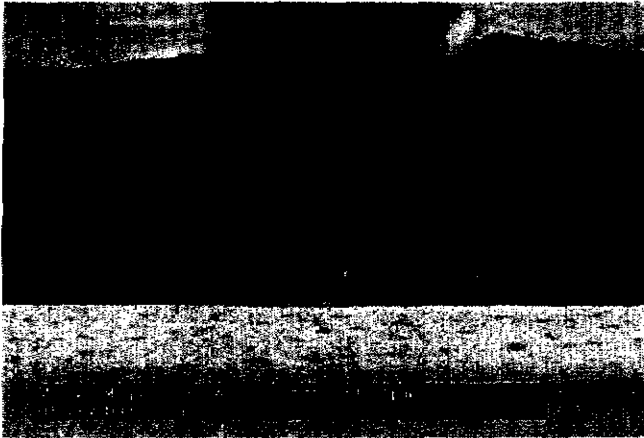

Fig.1. The profile of the trilayer resist for the submicron T gate.

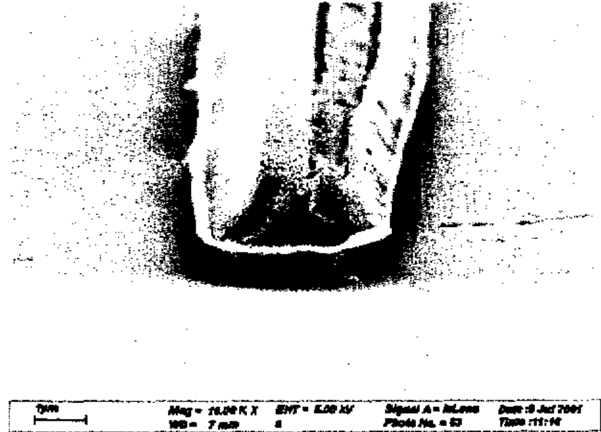

Fig . 2. The fabricated submicron T-gate on GaAs substrate. The footprint is 0.4μm.

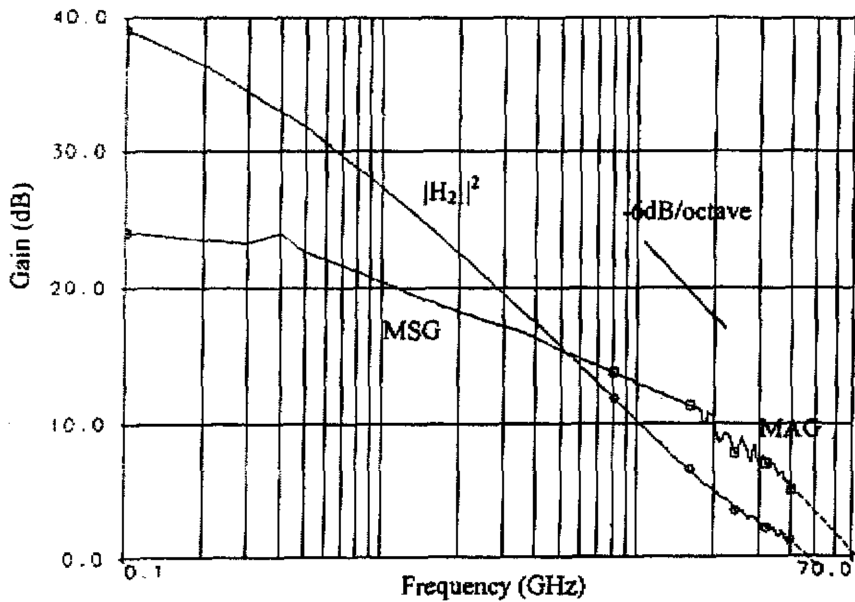

Fig.3. Power gain and current gain of GaInP HFET.

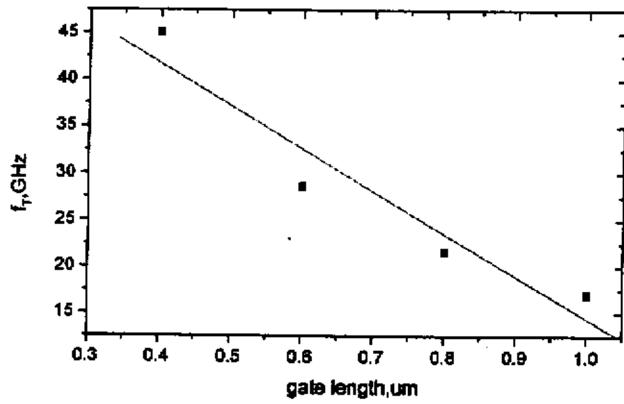

Fig. 4 Cut-off frequency against flowed photoresist gate length

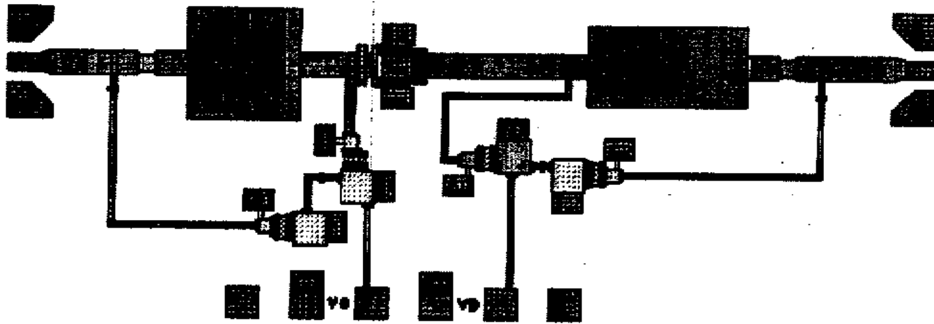

Fig. 5 The chip layout of 28GHz MMIC power amplifier

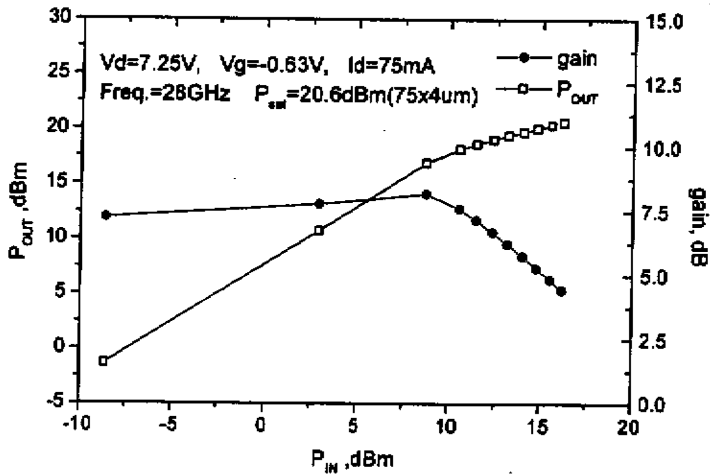

Fig. 6 The measured output power (P_{out}) and power gain characteristics versus input power of 28 GHz MMIC power amplifier