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用於超大型積電低電壓電路之深次微米小尺寸超薄絕緣體上矽金氧半元件模型

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Compact LDD/FD SOI CMOS Device Model Considering Energy Transport and Self Heating for SPICE Circuit Simulation

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Abstract

This paper reports a compact drain current model considering energy transport and self heating for short-channel fully-depleted (FD) SOI NMOS devices with a lightly-doped drain (LDD) structure. Considering energy transport and self heating, the compact drain current model provides an accurate prediction of the drain current behavior of a 0.25μm *FD SOI NMOS device with an LDD structure as verified by MEDICI 2D results and experimental data. The device with an LDD structure has a smaller effective electron mobility at a low drain voltage, where lattice temperature is dominant as compared to the device without an LDD structure, and a higher mobility at a high drain voltage, where electron temperature dominates.*

1. Introduction

SOI technology has been receiving a lot of attention owing to its potentials for VLSI. As for bulk CMOS devices, lightly-doped drain structure has been used in FD SOI CMOS devices to reduce high electric field effects [1]-[3]. As for bulk CMOS devices, due to the complicated structure of the sidewall/n- LDD region in the device, closed-form analytical models for LDD/FD SOI MOS devices have been difficult to obtain. Recently, an electron/lattice temperature related mobility model by considering energy balance equation has been reported for the short-channel SOI MOS devices [4]. Until now, no compact drain current models for short-channel FD SOI MOS devices with an LDD structure considering the electron and lattice temperature-related mobility model are available. In order to facilitate SPICE circuit simulation, in this paper, a concise drain current model considering energy transport and self heating for short-channel FD SOI NMOS devices with an LDD structure, using energy balance equation is presented.

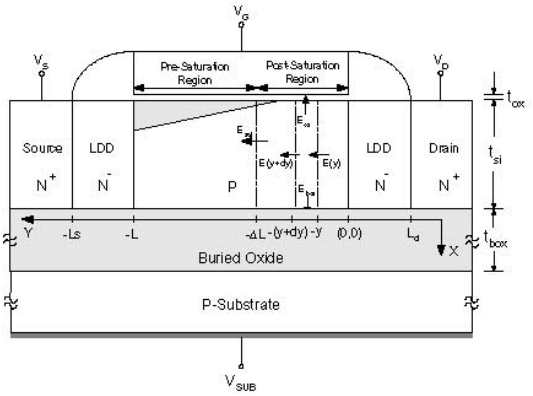


Figure 1: Cross section of the FD SOI NMOS device with an LDD structure.

2. Concise Model

Fig. 1 shows the cross section of the FD SOI NMOS device with an LDD structure under study. As shown in the figure, in order to simplify the analysis, an LDD structure without an overlap with the gate has been adopted in the FD SOI NMOS device. In addition, the fringing electric field effect via the oxide sidewall spacer is neglected. The potential distribution in the lateral channel/n- LDD region has been obtained by solving the 2D Poisson's equation ,using a second order polynomial for approximation. Considering that at the two n-LDD/channel boundaries, the electric field and the potential are continuous, the surface potential in the center channel region is solved as:

$$V_{sf}(y) = A_0 e^{r_0(y+L)} + B_0 e^{-r_0(y+L)} - \frac{qN_A k_s}{r_0^2 \epsilon_{si}} - \frac{\beta_1}{r_0^2} \quad (1)$$

From the lateral surface electric field by differentiating Eq. (1) and solving the energy balance equation, the electron temperature profile in the device can be obtained:

$$T_n(y) = M_0 e^{r_0(y+L)} + N_0 e^{-r_0(y+L)} + R_0. \qquad (2)$$

The temperature-dependent electron mobility can be expressed as a function of the difference between the electron and the lattice temperatures. The effective electron mobility, which is derived from the temperature-dependent electron mobility, is a function of the difference between the electron and the lattice temperatures. Therefore, for the device biased in the triode region, the drain current can be obtained. From the energy balance equation, the effective electron mobility and the drain current, the lattice temperature can be expressed as:

$$T_l(V_D, V_G) = \frac{-(Bf-1) - \sqrt{(Bf-1)^2 - 4Af(Cf+T_0)}}{2Af}, \qquad (3)$$

where $f = C_{ox}\frac{W}{L}[(V_G - V_T)V_D - a_0 V_D^2]V_D R_{th}$. For the device biased in the saturation region, the lateral channel region is divided into pre-saturation and post-saturation regions, separated by the boundary at $y = -\Delta L$ with a potential of V_{DSAT},which can be described as:

$$V_{DSAT} = V_{DSAT1} + V_p - (V_{DSAT1}^n + V_p^n)^{\frac{1}{n}} \qquad (4)$$

where V_p is the drain voltage when the device is biased with pinchoff at the drain ($\frac{dI_D}{dV_D} = 0$) and V_{DSAT1} is the drain voltage defined by the condition that traveling electrons reaching the saturated velocity at drain. Applying 2D Gauss law to the post-saturation region and using the boundary conditions that at the boundary the potential and electric field are continuous, the length of the post saturation region– ΔL can be obtained. In the saturation region, impact ionization effect has been included in the drain current model. Following a Similar approach as for the triode region, the lattice temperature can be obtained as:

$$T_l(V_D, V_G) = \frac{-(GBf'-1) - \sqrt{(GBf'-1)^2 - 4GAf'I_t}}{2GAf'}, \qquad (5)$$

where $I_t = GCf' + HI_{CB0}V_D R_{th} + T_0$ and $f' = C_{ox}\frac{W}{L-\Delta L}[(V_G - V_T)V_{DSAT} - a_0 V_{DSAT}^2]V_D R_{th}$.

3. Model Evaluation

In order to assess the effectiveness of the compact model for the FD SOI NMOS device with an LDD structure, the model results have been compared with the simulation results and the experimental data [3]. Fig. 3 shows the drain current characteristics of the FD SOI NMOS device with (a) and without (b) an LDD structure. As shown in the figure, without considering self heating (EB only), both the simulation and the model results indicate an overestimated drain current as compared to the experimental data[3]. Compared to the device with an LDD structure (Fig. 3(a)), the drain current behavior of the device without the LDD structure (Fig. 3(b)) demonstrate a much larger impact ionization current at a high drain voltage due to a larger electric field without the LDD structure. Considering both energy transport and self heating (EB+LT), the compact model could accurately predict the drain current characteristics for the device with and without the LDD structures.

Fig. 4 shows (a) the lattice temperature, (b) the ef-

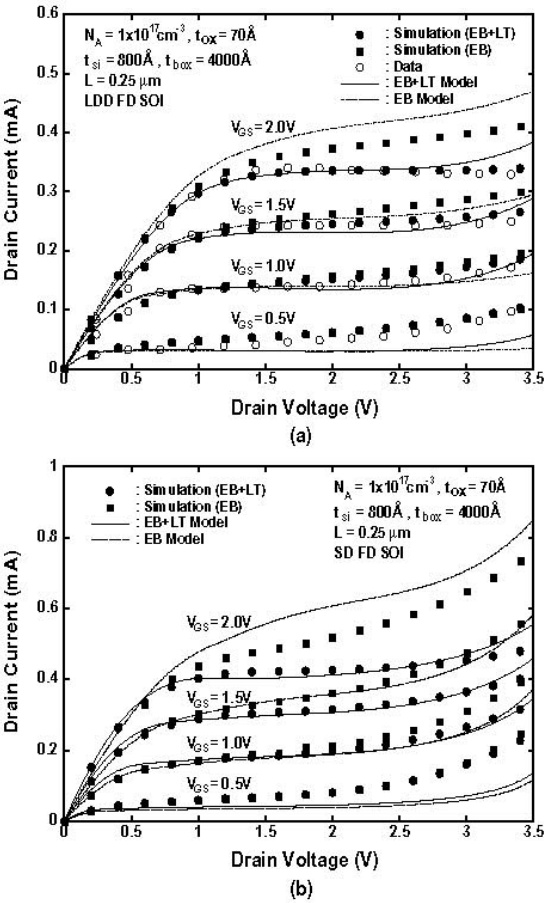
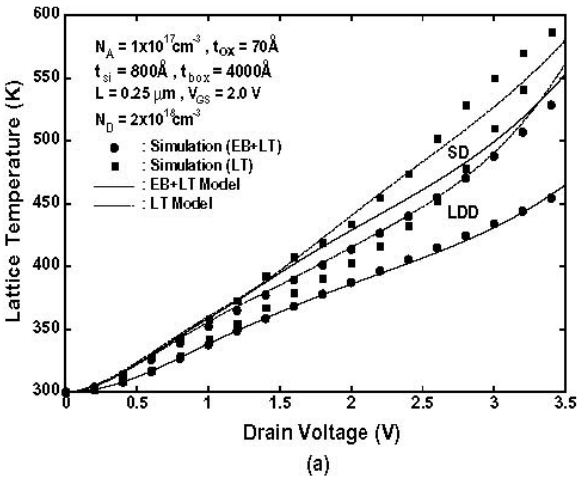
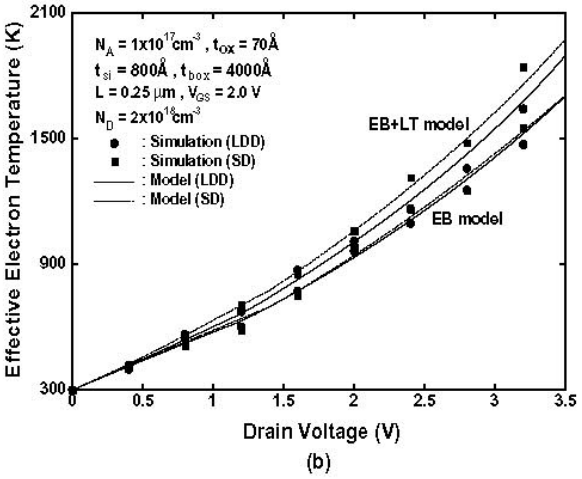


Figure 2: Drain current characteristics of the FD SOI NMOS device with (a) and without (b) an LDD structure, based on the experimental data [3], the model and the simulation results considering both energy transport and self heating (EB+LT) and considering energy transport only (EB).





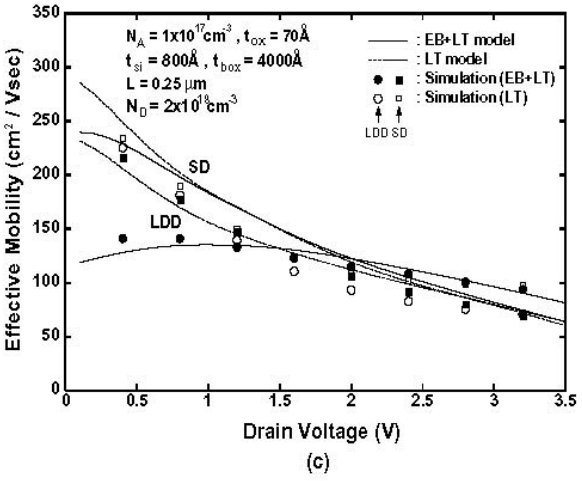
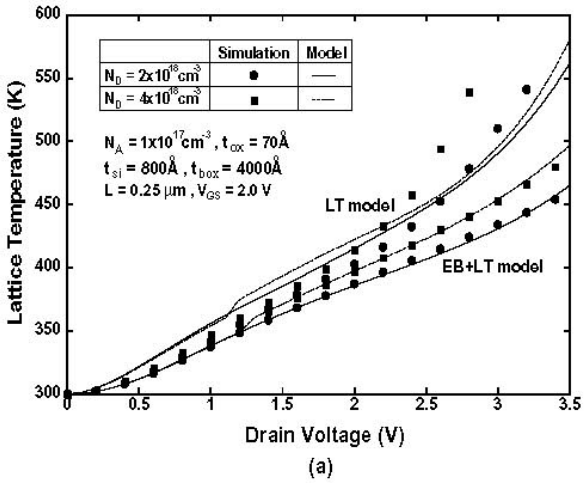


Figure 3: (a) Lattice temperature, (b) effective electron temperature and (c) effective mobility versus drain voltage of the FD SOI NMOS device with and without an LDD structure, based on the simulation and the model results considering both energy transport and self heating (EB+LT), only energy transport (EB), and only self heating (LT).



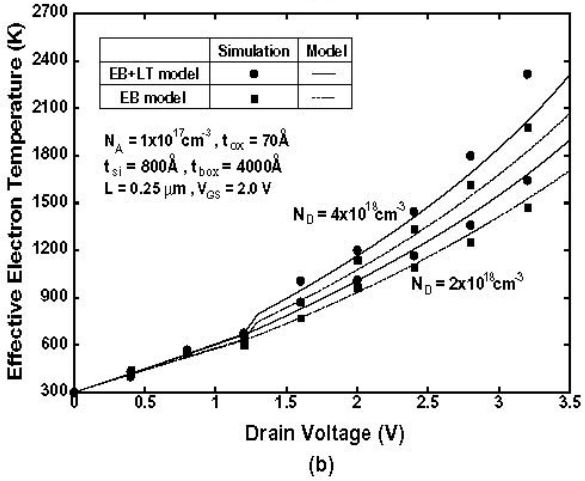


Figure 4: (a) Lattice temperature and (b) effective electron temperature versus drain voltage of the FD SOI NMOS device with, based on the the 2D simulation and the model results considering both energy transport and self heating (EB+LT), only energy transport (EB), and only self heating (LT).

fective electron temperature and (c) the effective mobility versus the drain voltage of the FD SOI NMOS device with and without an LDD structure. As shown in Fig. 4(a), compared to the case without an LDD structure, the lattice temperature of the device with the LDD structure is lower, which is especially noticeable at a high drain voltage. As for the effective electron temperature as shown in Fig. 4(b), considering both EB and LT, the effective electron temperature is higher for both devices with and without the LDD structure. In addition, the effective electron temperature of the LDD one is smaller than that of the one without the LDD structure (SD) due to a smaller electric field. For both SD and LDD, the model considering EB and LT provides a more accurate prediction of the lattice and the effective electron temperatures. As shown in Fig. 4(c), without consid-

ering EB, the effective mobility is over-estimated at a low drain voltage due to an over-estimated lattice temperature as indicated in Fig. 4(a). From Fig. 4(c), comparing the LDD curve with the SD one (EB+LT), the SD one has a higher effective electron mobility at a lower drain voltage and a lower value at a higher drain voltage. At a low drain voltage, the effective electron mobility is determined predominantly by the lattice temperature. At a high drain voltage, on the contrary, the effective electron mobility is determined mainly by the effective electron temperature.

Fig. 5 shows (a) lattice temperature and (b) effective electron temperature versus drain voltage of the FD SOI NMOS device, biased at $V_{GS} = 2V$, based on the 2D simulation and the model results considering both energy transport and self heating (EB+LT), only energy transport (EB), and only self heating (LT). As shown in the figure, when the doping density of the LDD region is increased from $2 \times 10^{18} cm^{-3}$ to $4 \times 10^{18} cm^{-3}$, both the lattice and the effective electron temperatures increase in the device due to the reduced effectiveness of the LDD region– a more highly doped LDD region raises the electric field in the channel region, therefore both temperatures increase, which is especially serious at a high drain voltage. As shown in the figure, without considering energy transport (LT only), the lattice temperature may have been over-estimated. In contrast, without considering self heating (EB only), the effective electron mobility is under-estimated at a high drain voltage.

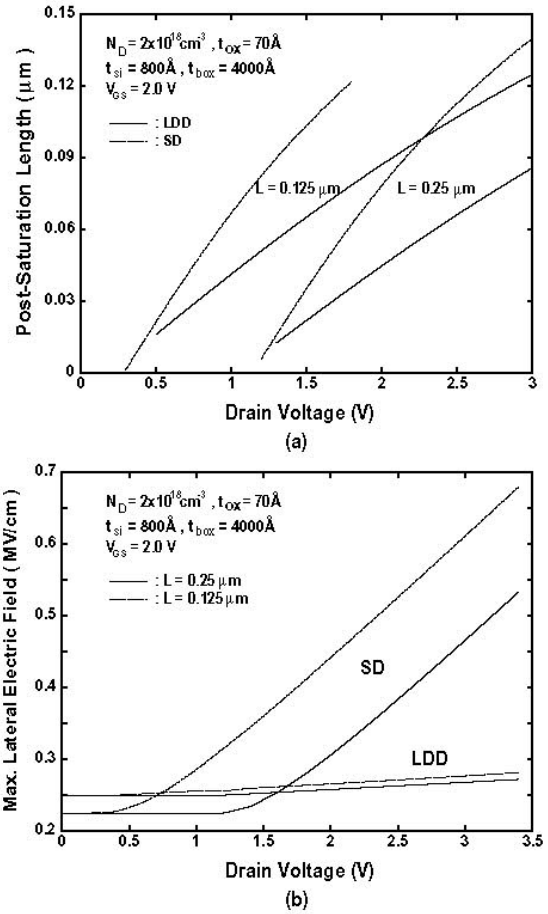


Figure 5: (a) Post-saturation length and (b) maximum lateral electric field versus drain voltage of the FD SOI NMOS device, based on the compact model considering both energy transport and self heating (EB+LT).

4. Discussion

Fig. 6 shows (a) post-saturation length and (b) maximum lateral electric field versus drain voltage of the FD SOI NMOS device with and without an LDD structure, based on the compact model considering both energy transport and self heating (EB+LT). As shown in Fig. 6(a), when the channel length is scaled down, for having an identical post-saturation length, the operation drain voltage is reduced for both SD and LDD devices. With the reduction of the electric field via the LDD structure, the LDD device does sustain a higher drain voltage at an identical post-saturation length based on the compact model considering both energy transport and self heating. As shown in Fig. 6(b), based on the compact model considering both energy transport and self heating, the maximum lateral electric field of the SD device increases when the drain voltage is raised. When the channel length is shrunk, the maximum lateral electric field for the SD device is even higher at a high drain voltage. In contrast, for the LDD one, regardless of the drain voltage, the maximum lateral electric field maintains at a low value. In addition, the shrinkage of the channel length results in a much smaller increase in the maximum lateral electric field as compared to the SD case, which implies that the LDD structure is also very effective in cutting down the high electric field effect even for the short-channel FD SOI device.

5. Conclusion

In this paper a closed-form LDD/FD SOI CMOS device model considering energy transport and self heating for SPICE circuit simulation has been described. Based on the analytical model, when the channel length of the FD SOI NMOS device is scaled down, the maximum lateral electric field in the device is much less sensitive to the drain voltage as compared to the counterpart without the LDD structure.

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