行政院國家科學委員會補助專題研究計畫成果報告

微機電微波元件之研究之
子計劃一
三五族微機電技術研發及應用

計畫類別：■整合型計畫

計畫編號：NSC　90-2218-E-002-035-

執行期間：　90年8月1日至91年7月31日

計畫主持人：呂學士　教授

本成果報告包括以下應繳交之附件：

■出席國際學術會議心得報告及發表之論文各一份

執行單位：國立台灣大學電子所

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主持人：　呂學士　台灣大學電機系教授

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一、中文摘要

本計劃已經成功利用微機電製程完成了IC電感下方的矽質基板的掏空。在後製程的步驟中最重要的是Laser burning的應用。這樣的製程最大的優點就是只要利用IC廠提供的製程就可完成後製程微機電製程，可這樣的方法將大大的降低了生產成本。最後實驗結果顯示，經過後製程掏空基板的電感其Q其可以改善50%，並減少電感與基板之間的耦合效應。

關鍵詞：微機電，後製程，電感

Abstract

This project has demostrated the micromachining between an on-chip spiral inductor and silicon substrate successfully. The micromachined on-chip inductor can be realized in standard silicon technologies without additional processing steps. The technique of laser burning is also applied in this paper. Experimental results show that the inductor achieves the most improvement. At 5 GHz, micromachining of the micromachined inductor increases the inductor quality factor up to 50% and reduces the substrate coupling between two adjacent inductors.

Keywords: micromachining, On-Chip-Inductor, RFIC

2. Introduction

The growing needs for miniature wireless communication and have prompted interest in monolithic RF amplifiers in silicon. Modern bipolar transistors and FET's certainly have a high enough ft to provide gain in required narrow frequency band at several GHz, for example, the application of HIPERLAN at 5 GHz; the challenge, interestingly enough, is in the difficult fabrication of monolithic passive components. Now we take use of the micromachining technique to remove the substrate. The following discussion will also show that micromachined inductors obtain the most improvement at 5GHz, where is the band of the HIPERLAN.

3. Principles of Inductor

The efficiency of an inductor is measured by its Q-factor, which is limited by the parasitic. The energy storage and loss mechanisms in an inductor on silicon can be described by the equivalent energy model shown in Fig.1, where L_S, R_S ,R_P and C_O represent the overall inductance, conductor loss, substrate loss, and overall capacitance respectively. ($C_O = C_P + C_S$) Note that R_P and C_P represent the combined effects of C_{OX} ,C_{Si} and R_{Si}, and hence are frequency-dependent. Combining the energy terms according to the fundamental definition of Q yields

$$Q = 2\pi \frac{|Peak\ Magnetic\ Energy - Peak\ Electric\ Energy|}{Energy\ Loss\ in\ One\ Oscillation\ Cycle}$$

$$= \frac{\omega L_s}{R_s} \times \frac{R_p}{R_p + \left[\left(\omega L_s / R_s\right)^2 + 1\right] \cdot R_s} \times \left(1 - \frac{R_s^2 C_o}{L_s} - \omega^2 L_s C_o\right)$$

[1], where $\omega L_S/R_S$ accounts for the magnetic energy stored and the ohmic loss in the spiral conductor. The second term is the substrate loss factor representing silicon substrate. The last term is the self-resonance factor describing the reduction in Q due to the increase in the peak electric energy with frequency and the vanishing of Q at self-resonance frequency.

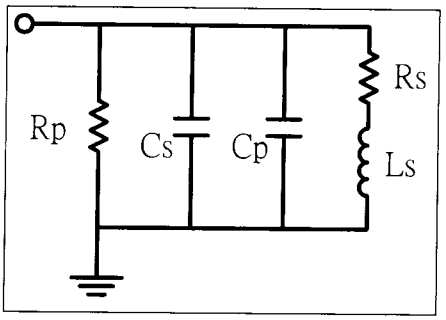


Fig. 1 The equivalent energy model for a one-port inductor.

L_S and R_S are subject to eddy current effect in the conductor. C_S is independent of frequency since it represents the metal-to-metal crossover capacitance between the spiral and the center-tap. From the discussion above, we can get such a conclusion that the degradation in Q-factor of an inductor is mainly due to the series resistance and the silicon substrate. Increasing the metal thickness or widening the width of metal lines can be used to reduce the series resistance. However, the thickness of metal connection has its limited in a CMOS process, and wider metal lines not only take larger chip area but also raise the substrate dissipation at high frequency. The strategy we take here is to remove the silicon substrate and it seems to be more attractive in the higher frequency range. If we want to push the CMOS RF circuit operating frequency up to 5GHz or higher, we can not take the risk of lowering self-resonance frequency to widening the metal lines as we wish; but contrive to make the underneath silicon substrate disappear.

3. Simulation and Fabrication

An etching simulator is used to get the etching sequels. This simulator is Anisotropic Crystalline Etching Simulation, ACES.The pictures of several etching pattern and their etching results are all shown in Fig.2 and Fig.3 [2]. From the simulation results, it is not difficult to decide which one should be our etching pattern. The first pattern in Fig.2(a) can achieve the task of substrate etching in a shorter time and leaves additionally four underpinnings under the inductor after etching process. The structure in Fig.3(c) likewise can remove most of substrate under an octagonal spiral inductor and leave two underpinnings.

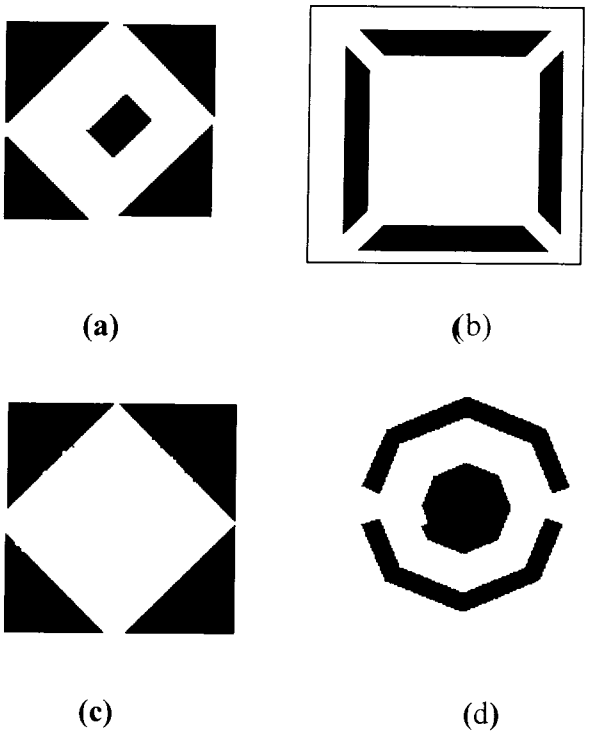


Fig. 2 The simulation results of etching process.

The micromachining technique is designed for a post-process compatible with present CMOS technology. First, we must design the adequate etching holes, so we adapted the pattern in Fig.2(a). The etching holes are made of the four via layers plus the passivation layer. If we design the layer of VIA where the metal layers do not exist, it will leave there a clearance with its shape

like a tube. When these tubes are superimposed connected in the CMOS process, a channel from outside to the substrate is formed. The etching process starts once the etching solution is heated up to 70°C, but we keep heating the solution to 92°C for a higher etching rate [3][4][5].

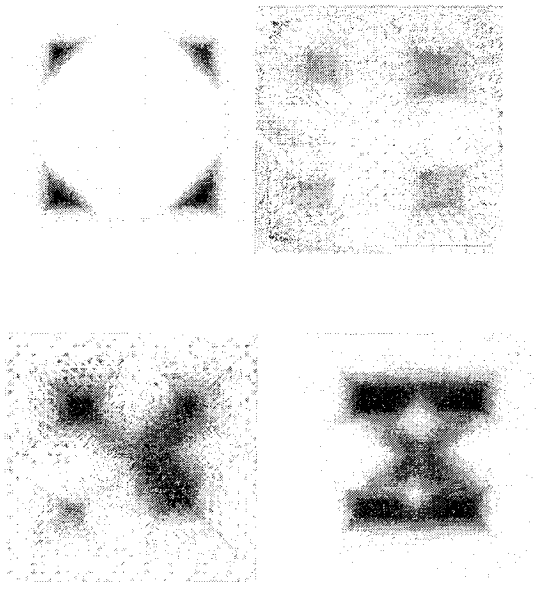
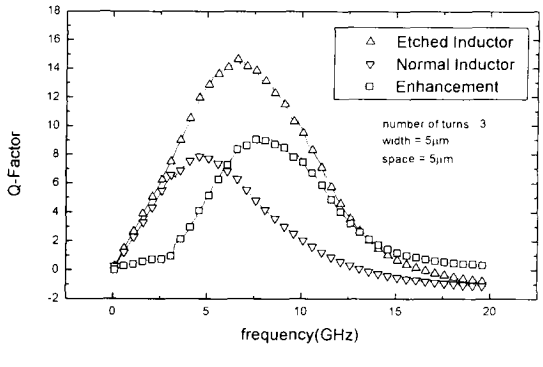


Fig. 3 The masks for etching process.

There is one problem about the metal pads where no passivation nitride covers. Since the etching solution TMAH is a soft organic acid and it not only reacts with silicon but also reacts with aluminum metal lines gently. As the time goes by, the resistance of metal pads for testing increases. We can not ignore this situation because sometimes we find it could make a large measurement error if the probe and pads do not have good contact. Under the circumstances, the approach of laser burning is proposed to solve this problem. First, we make the pads be covered by nitride passivation, and the metal pads will be well protected by this solid nitride layer during the etching process. After the silicon substrate is successfully removed by TMAH, we can take the nitride passivation away and perform the measurement. The nitride passivation is stripped by laser burning, the maximum size of exposure area is 50μm x 50μm. The power of the laser must be tuned properly. If the power is not properly controlled, the nitride will not be removed and the measurement can not be performed at all.

4 Measurement and Conclusion

The measured results of micro-machined and non-micro-machined inductor are compared. The Q factor of the inductor with different turns are shown on the Smith chart in Fig.4. At 5 GHz, micromachining of the micromachined inductor increases the inductor quality factor at least 60% .It also observed that the Q factor for both kinds of inductors are identical below 5GHz. This is not surprising because at low frequencies, the dissipation caused by silicon substrate is still negligible. This result could probably be explained as follows: The turns-number of an inductor increasing indicates that more metal lines lie on the silicon substrate and more parasitic capacitors and resistors due to the substrate are created and shunt together. Thus, the larger parasitic substrate capacitance and smaller substrate resistance will make more energy dissipate into the substrate. However, once the substrate is taken away, the difference provoked will be more marked and obvious. The models of normal inductors and substrate-etched inductors are extracted and compared as shown in the Table I.
It is obviously that the substrate parasitics such as R_{Si} ,*Cox and Csi* are reduced.



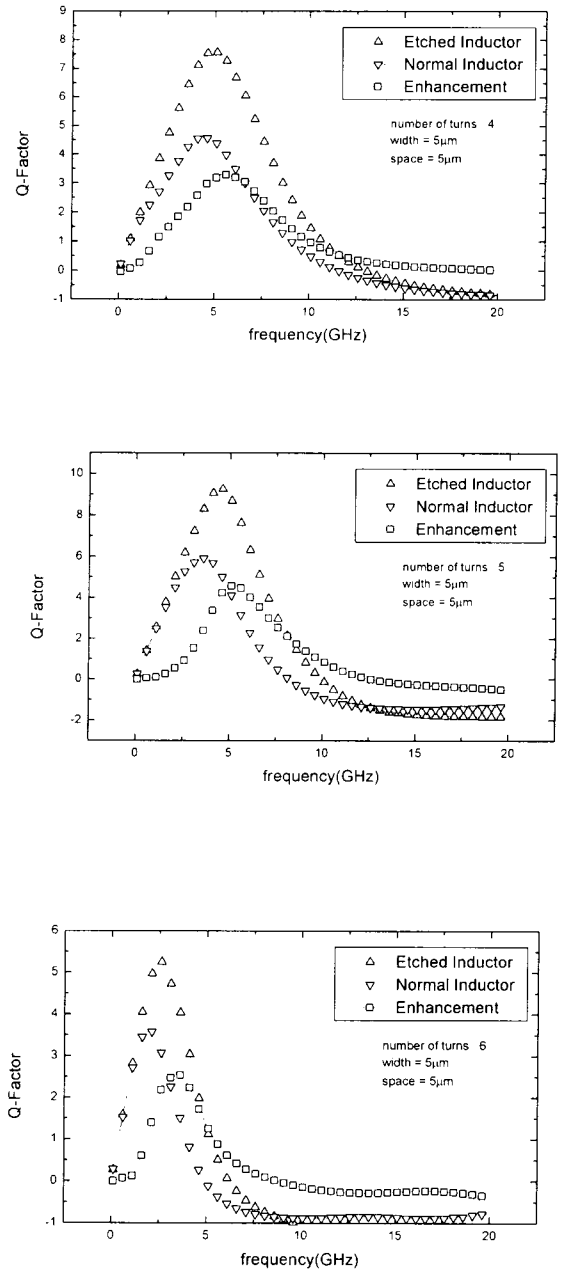


Fig. 4 Q factor results of inductor with different turns

ID	Rsi1(ohm)	Rsi2(ohm)	Csi1(fF)	Csi2(fF)	Cox1(fF)	Cox2(fF)
L03	323.42	181.39	2.06	2.32	38.1	55.9
L04	204.71	167.73	0	24.49	46	67.3
L05	172.26	293.72	0.11	0	58	74
L06	274.35	198.83	0.48	0.08	86	99
L03_etched	open	835.95	0	12.9	38.1	55.9
L04_etched	1087.63	566.13	0.03	0.17	46	67.3
L05_etched	600	2000	28.25	2.78	58	74
L06_etched	793.31	1364.17	0.01	0	86	99

Table I Comparison of the extracted parameter of inductors

Acknowledgements

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References

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QUALITY FACTOR IMPROVEMENT OF ON-CHIP INDUCTOR FOR HIPERLAN RFIC BY MICROMACHINING

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This paper present the micromachining between an on-chip spiral inductor and silicon substrate. The micromachined on-chip inductor can be realized in standard silicontechnologies without additional processing steps. The technique of laser buring is also applied in this paper. Experimental results show that the inductor achieves the most improvement. At 5 GHz, micromachining of the micromachined inductor increases the inductor quality factor up to 50% and reduces the substrate coupling between two adjacent inductors.

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