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子計畫八：HBT 中頻積體電路及後製程研究(2/3)

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行政院國家科學委員會專題研究計畫成果報告

38-GHz 無線收發系統關鍵元組件技術-子計劃八

HBT 中頻積體電路及後製程研究(2/3)

計畫編號：NSC 91-2219-E-002-021

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主持人：　　呂學士　台灣大學電機系教授

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中文摘要

本計畫首度以磷化銦鎵/砷化鎵異質接面製程成功地實現 5.7GHz 單晶片內插式壓控振盪器。不同於傳統上改變共振腔電容，本研究以改變開路增益的方式控制頻率變化，實驗證實在中心頻率 5.7GHz 時，頻率可調範圍達到 400 MHz，可成功地應用於 ISM 頻段。

關鍵詞：磷化銦鎵，砷化鎵，內插式，壓控振盪器。

Abstract — A 5.7 GHz monolithic interpolative voltage controlled oscillator using InGaP/GaAs HBT technology is demonstrated for the first time. Frequency tuning is achieved by changing the open loop gain instead of the tank capacitor. The experimental result showed that a 400-MHz tuning range at 5.7 GHz was realized, which can meet the requirement of 5.7GHz ISM band.

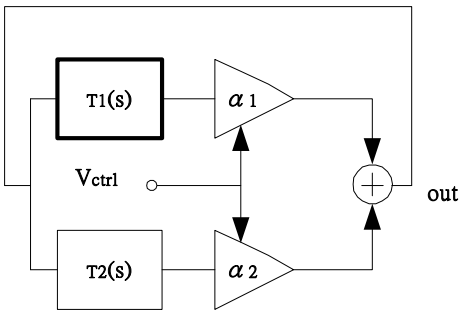
1. INTODUCTION

Voltage-controlled oscillators (VCO's) are widely used in communication systems. Among the many versions of the VCO's, such as relaxation oscillators [1], ring oscillators [2], and LC sinusoidal oscillators [3], it is generally accepted that LC sinusoidal oscillators have the best high frequency-performance in terms of phase noise characteristics and frequency stability [4]. Most LC oscillators use varactors to vary their oscillating frequencies. Nguyen and Meyer, however, proposed and realized an interpolative VCO [4] in which the oscillating frequency is interpolated from two resonant frequencies of two LC resonators and hence wide tuning range can be obtained quite easily. In their work a tuning range of 200-MHz at 1.8 GHz was obtained by using an oxide-isolated BiCMOS IC process with typical fT (n-p-n) = 10 GHz.

Recently FCC in the United States has proposed to allocate 300MHz of spectrum in 5-6GHZ band for ISM use, and the wireless LAN is one potential application which could exploit this new spectral allocation [5]. Consequently, an oscillator with a tuning range of 300-MHz at 5.7 GHz is necessary. In order to meet the requirements of high operating frequency and wide tuning range, we were motivated to use InGaP/GaAs HBT rather than BiCMOS IC process to realize the monolithic interpolative oscillators. The experimental results showed that a 400-MHz tuning range centered at 5.7 GHz , phase noise of –96 dBc/Hz measured at 100 kHz offset from the carrier (5.7 GHz) and output power of –13 dBm were obtained.

2. PRINCIPLES OF CIRCUIT DESIGN

The detailed analysis of the interpolative oscillator has been done in Ref. [4]. However, a different view- point in obtaining the open loop gain the VCO is presented in this paper. The fundamental idea of the interpolative VCO according to Ref. [6] is summarized as follows. This feedback oscillatory system as shown in Fig.1 incorporates two transfer functions, $T_1(s)$ and $T_2(s)$, whose outputs are scaled by variable factors α_1 and α_2, respectively, and summed. The overall open-loop transfer function is therefore equal to $L(s) = \alpha_1 \cdot T_1(s) + \alpha_2 \cdot T_2(s)$, which must



be equal to +1 for the system to oscillate. In the extreme case where $\alpha_1=0$ or $\alpha_2=0$, the oscillation frequency ω_C is

Fig. 1. The block diagram of the interpolative VCO

determined by only $T_2(s)$ or $T_1(s)$ and for intermediate values of α_1 and α_2, ω_C can be interpolated between its lower and upper bounds.

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The core circuit of the interpolative VCO is depicted in Fig. 2 where all the transistors in this figure are identical. The control voltage V_C is applied across the base nodes of Q1 and Q2

(also Q2 and Q3) to modify the transconductances (g_{m1} and g_{m2}) of Q1 and Q2, respectively. Note that the collector bias current I_{C1} of Q1 equals that I_{C4} of Q4 and so does I_{C2} of Q2 to I_{C3} of Q3, and I_{C5} of Q5 to I_{C6} of Q6. Furthermore, $I_{C1}+I_{C3} \cong I_{C5} \cong I/2 \cong I_{C6} \cong I_{C2}+I_{C4}$, where I is the constant curren source in Fig. 2. In fact I_{C1}, I_{C2}, I_{C3}, and I_{C4} can be given by

$$Ie1 = Ie3 = \frac{Ie5}{1+\exp(\frac{V_{b2}-V_{b1}}{V_T})} \quad (1)$$

$$Ie2 = Ie4 = \frac{Ie5}{1+\exp(\frac{V_{b1}-V_{b2}}{V_T})} \quad (2)$$

Because transconductances are proportional to the collector currents of BJT's, (1) and (2) can be rewritten as:

$$gm1 = gm3 = \frac{gm5}{1+\exp(\frac{V_{b2}-V_{b1}}{V_T})} \quad (3)$$

$$gm2 = gm4 = \frac{gm5}{1+\exp(\frac{V_{b1}-V_{b2}}{V_T})} \quad (4)$$

where $G_m = I/(2V_T)=g_{m5}=g_{m6}$.

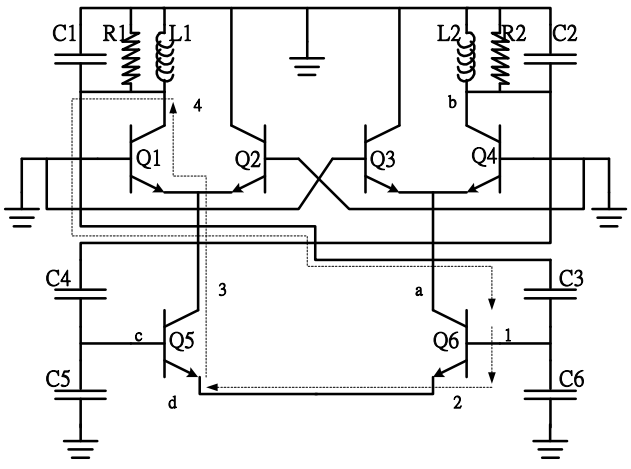


Fig. 2. The core circuit of the VCO. This a simplified AC schematic, and the DC bias is not shown here.

The total open loop gain L(s) can be found as follows. Since the output of the VCO will be taken differentially between the base nodes of Q5 and Q6, we break the loop there and then apply a test voltage Vx. Because of the symmetry of the circuit, it can be thought of as Vx/2 is applied to the base of Q6 and –Vx/2 to the base of Q5. Superposition can be used for the ease of analysis. That is, first the returned voltage appeared at base node of Q6 is calculated by applying Vx/2 to base of Q6 and zero voltage to the base of Q5. Then the returned voltage appeared at the base node of Q5 is calculated by applying –Vx/2 to the base node and zero voltage to the base node of Q6. The total returned voltage will be the difference of the two returned voltages in previous two cases. In the former case, the signal traverses along the path numbered from #1 to #4 (the left loop) with a returned voltage of $L_1(s)$ Vx/2 while the latter along the path from #a to #d with returned voltage of $L_2(s)$ (-Vx/2). L1(s) and L2(s) represent the loop gains of the left loop and the right loop, respectively. The total returned voltage is then (L1(s) + L2(s)) Vx and hence the total loop gain L(s) is L1(s) + L2(s). L1(s) and L2(s) can be shown to be

$$L_1(s) = -\frac{gm5}{1+\exp(\frac{V_{b2}-V_{b1}}{V_T})} \cdot \left(\frac{sL_1}{s^2L_1Cx + s\frac{L_1}{R_1}+1}\right) \cdot \left(\frac{C_3}{C_3+\frac{C_6}{2}+C_6}\right) \quad (5)$$

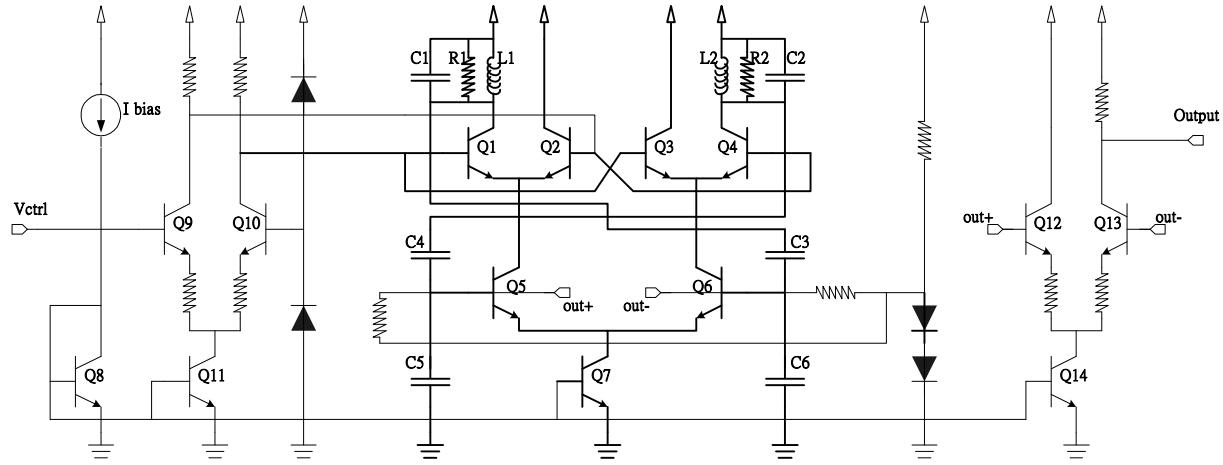
$$L_2(s) = -\frac{gm5}{1+\exp(\frac{V_{b1}-V_{b2}}{V_T})} \cdot \left(\frac{sL_2}{s^2L_2Cy + s\frac{L_2}{R_2}+1}\right) \cdot \left(\frac{C_4}{C_4+\frac{C_5}{2}+C_5}\right) \quad (6)$$

where

$$Cx = C_1 + \frac{C_2 \cdot (\frac{C_6}{2}+C_6)}{C_3+\frac{C_6}{2}+C_6} \quad (7)$$

$$Cy = C_2 + \frac{C_4 \cdot (\frac{C_5}{2}+C_5)}{C_4+\frac{C_5}{2}+C_5} \quad (8)$$

Therefore L(s) can be written as follow



$$L(s) = L_1(s) + L_2(s) = \sim_1 \cdot T_1(s) + \sim_2 \cdot T_2(s) \quad (9)$$

$$T_1(s) = -gm5 \cdot \left(\frac{sL_1}{s^2 L_1 C_x + s\frac{L_1}{R_1} + 1}\right) \cdot \left(\frac{C_3}{C_3 + \frac{C_6}{2} + C_6}\right) \quad (10)$$

where

Fig.3. The complete circuit schematic of the monolithic VCO.

$$T_2(s) = -gm5 \cdot \left(\frac{sL_2}{s^2 L_2 C_y + s\frac{L_2}{R_2} + 1}\right) \cdot \left(\frac{C_4}{C_4 + \frac{C_5}{2} + C_5}\right) \quad (11)$$

$$\sim_1 = \frac{1}{1 + \exp\left(\frac{V_{b2} - V_{b1}}{V_T}\right)}$$

$$\sim_2 = \frac{1}{1 + \exp\left(\frac{V_{b1} - V_{b2}}{V_T}\right)} \quad (12)$$

Finally, the open-loop gain L(s) is set to unity for the system to oscillate,.

3. CIRCUIT FABRICATION& MEASURED RESULTS

The complete circuit of the interpolative VCO based on the design principles presented in section II is shown in Fig.3. A single-to-differential converting circuit consisting of Q9 and Q10 is used to convert the single-ended control voltage Vctrl to the control voltage V_C. The differential output voltage across the base nodes of Q5 and Q6 of the core circuit is converted to a single-ended output voltage Vout by a differential amplifier composed of Q12 and Q13. The simulation result of oscillation frequency versus Vctrl by Star-HSPICE is shown in Fig. 4. InGaP/GaAs HBT IC process with fT = 40 GHz is used to fabricate the VCO and the die photograph of the finished VCO is shown in Fig. 5. The measured characteristics of oscillation frequency versus Vctrl exhibit a tuning range of 400MHz extending from 5.45GHz to 5.85GHz as shown in Fig. 4. For a Vctrl of 2.5 V, the phase noise measured at 100 kHz offset from the carrier (fo=5.7 GHz) is -96dBc/Hz. An output power level of –13dBm is also obtained. All these results are better than the previous reported values of

oscillating frequency (1.8 GHz), tuning range (200 MHz), phase noise (-88 dBc/Hz) and output power (-23 dBm). The reason is obviously due to the better technology (InGaP/GaAs) we choose.

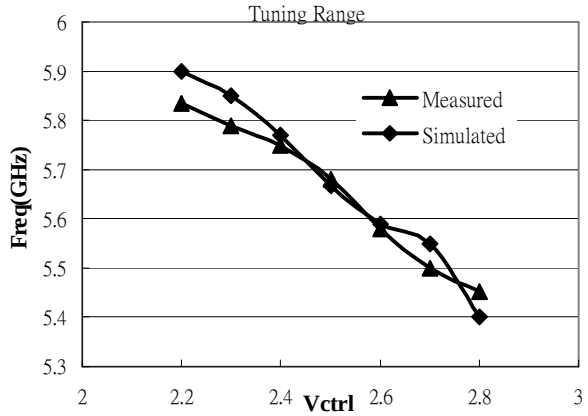


Fig.4. Measurement and simulation result.

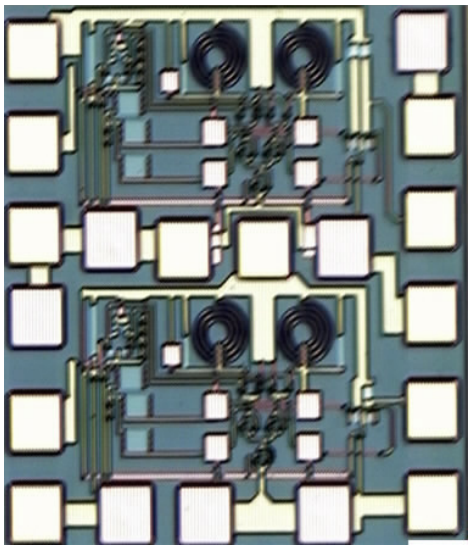


Fig.5. The die photograph of the monolithic VCO.

4. CONCLUSION

The first interpolative VCO using InGaP/GaAs HBT technology is reported. A 400-MHz tuning range at 5.7 GHz is achieved, which can meet the requirements of the recent FCC release of 300MHz spectrum in 5-6GHZ band for ISM use. The performance of the InGaP/GaAs interpolative VCO is better than that of BiCMOS VCO in terms of oscillating frequency, tuning range, phase noise and output power.

自我評估：本研就究按計畫成功地製出 5.7GHz 振盪器。本計畫亦衍生出一篇 IEEE Trans. Microwave Theory and Technique, 二篇 IEEE Trans. Electron Device, IEEE Electron Device Lett., 一篇 IEE Electronics Lett., 二篇 Microwave & Optical Technology Lett.，研究成果相當不錯。

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