HYBRID ROUTING ON MULTICHIP MODULES

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ABSTRACT

A new hybrid routing approach for multichip modules (MCM) is proposed and implemented. The routing implementation is divided into three stages: signal-net routing, i/o-pad interconnection, and power/ground layout. A special feature of our implementation is that in the second stage, some interconnected segments are allowed to be tilted with a slope for reducing the MCM layout area. Some tested examples are used to measure the effectiveness of our approach

1. INTRODUCTION

Recently, multichip modules (MCM) on a hybrid package have been effectively used to support high performance (or high speed) computer systems [1-3]. The hybrid package which combines several chips (2 to 20 unpackaged chips) with a number of metal layers (4 to 6 layers of metal) on a ceramic or silicon subtrate forms an MCM. In the MCM, since the placement is involved with fewer chips, and the sizes and shapes of chips are less variable, one can always obtain a good enough placement result. Therefore, successfully interconnecting these chips with a minimal MCM area is the other important issue of research.

The routing environment of an MCM can be described as follows. Given a good initial placement which consists of several one-row-pad or two-row-pad chips, a number of i/o pads around the MCM, a net-list information, and a hybrid technology [1-2] that involves four metal layers separated by a polyimide dielectric. The lowest metal layer forms a ground-net plane and covers the entire MCM area, the power-net is supplied through the second metal layer which covers the entire MCM area except areas under the chips, and the top two metal layers are used for signal interconnection. Fig. 1 shows the environment of routing on an MCM consisting of two unpackaged chips and a number of i/o pads. The goal of routing on an MCM is to complete the wiring of all the nets and minimize their interconnection length and the MCM area. This paper proposed a new hybrid routing approach for MCM. Its implementation consists of three stages: signal-net routing, i/o-pad interconnection, and power/ground layout. A special feature of our implementation is included in the i/o-pad interconnection where wires interconnecting net points and i/o pads are allowed to be tilted with a slope for reducing the MCM layout area. Some experimental examples are tested to confirm the effectiveness of our approach.

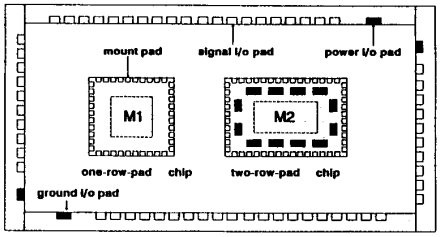

Fig. 1 Environment of the hybrid routing on an MCM consisting of two chips.

Section 2 introduces the hybrid routing approach for MCM; especially, the i/o-pad interconnection with sloped segments is depicted in details. Some experimental results is presented in Section 3. Finally, a conclusion is stated in Section 4.

2. HYBRID ROUTING APPROACH

Based on the routing environment of an MCM as introduced above, the implementation of the hybrid routing approach is divided into three major stages, which will be described in the following sub-sections.

2.1 Signal-Net Routing

Since only the top two layers are used to distribute the signal nets and high wiring density is often presented on an MCM, these two layers are always treated as one horizontal and one vertical layer, respectively. Also, the i/o pads around MCM are assumed still soft, i.e., the i/o pads location can be rearranged such that the net path obtained is closer to the shortest path. The signal-net routing is first involved to process all signal nets on the environment of an MCM by using the techniques of net-forest routing and H-V (Horizontal-Vertical) track assignment as presented in [4].

The net-forest routing, used in the H-V tile-expansion router [5], is a global router which logically wires all nets without violating the

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constraint of channel capacity and attempts to find a shortest net-forest path for each net. To achieve these goals, the net ordering must be carefully arranged: critical nets are the first ones to be routed; and if there are some bus nets, these nets are the next to be routed; finally, remaining nets are ordered according to their perimeter lengths (i.e., perimeter of the smallest rectangle which encloses all the terminals of a net) from short to long.

Then, the H-V track assignment is used to find the track distribution on each H-channel and V-channel such that the required tracks can be kept minimal. With the above techniques, routing area can be expanded or compressed in refining the placement to complete the layout and MCM area can thus be minimized. The detailed description on these techniques are presented in [4].

Since the i/o pads around MCM are assumed still soft, an i/o pad may be moved around for the purpose of obtaining a shortest net path in the stage of signal-net routing. However, some of i/o pads around MCM are possibly overlapped with each other, which will be solved in the stage of i/o-pad interconnection discussed below. Fig. 2 shows the initial layout of an MCM example mcm_x, which is obtained after the stage of signal-net routing.

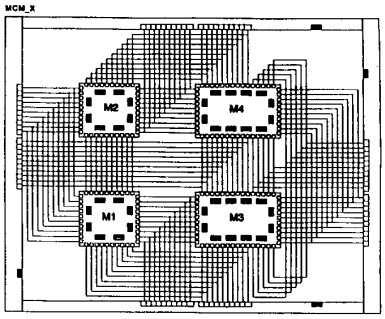

Fig. 2 Signal-net layout of an MCM example mcm_x.

2.2 I/O-Pad Interconnection

Most of i/o pads (except the power/ground pads) have been defined in the previous stage and can now be used to complete the routing of nets with shortest net paths, but this goal cannot always be achieved since the locations of these i/o pads are not completely correct. For instance, in Fig. 2, some of the i/o pads are overlapped with each other. Hence, it requires checking their locations to refine the i/o pads and re-connect their signal nets.

Also, to reduce the MCM area, interconnected segments between the i/o pads and their corresponding nets (or corresponding-net points) are allowed of being tilted with a slope, only if they do not cause any violation of design rules. For instance, Fig. 3(a) shows the initial layout of signal-net routing, which have five i/o pads and five net points. Since these i/o pads are

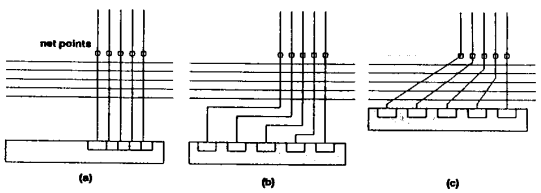

Fig. 3 Different schemes of I/O pad interconnections, (a) initial layout, (b) without, and (c) with sloped segments.

overlapped with each other, it is necessary to be expanded toward left or right. Here, left expansion is assumed for the i/o pads, and two methods can be used for completing the interconnection between these net points and i/o pads. One, a traditional method, is using H-V alternating segments to connect them and the other is using sloped segments. Clearly, the scheme of Fig. 3(c) with sloped segments would reduce more space area than the scheme of Fig. 3 (b) with H-V alternating segments. Note that the sloped segments in Fig. 3(c) are viewed as horizontal segments to avoid the design error of crossing vertical segments (in this case). Therefore, an MCM area can be reduced effectively by the sloped interconnections between the i/o pads and net points.

The space area (or called moat area) around MCM can be divided into four zones, i.e., left, right, bottom, and top zones. Each zone has some net points to be connected to the corresponding i/o pads. Thus, it is important to know how to align the net points and their corresponding i/o pads in each zone such that the sloped interconnections become correct (i.e., no violation of design rule) and with shortest length and MCM area is reduced.

Without loss of generality, a bottom zone is considered here. An i/o pad interconnection model is shown in Fig. 4, which have an initial results obtained from the signal-net routing. The model contains a number of net points, and their corresponding i/o pads. If these i/o pads are overlapped with each other, the expanded direction of these i/o pad locations depend on the locations of those net points.

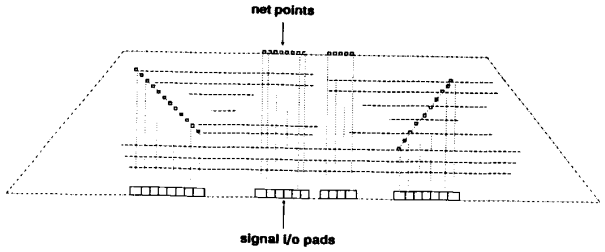

Fig. 4 Model of I/o pads interconnection.

The net points can be classified into three cases: parallel-net points (include a single-net point), downstair-net points, and upstair-net points, as shown in Figs. 5(a), 6(a) and 7(a), respectively. The interconnections of the parallel-net points to their corresponding i/o

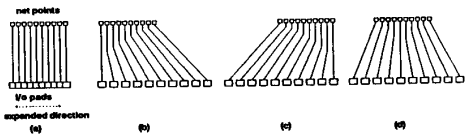

Fig. 5 Sloped interconnection of parallel-net points to I/o pads.

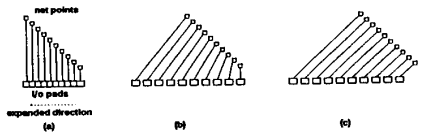

Fig. 6 Sloped interconnection of downstair-net points to I/o pads.

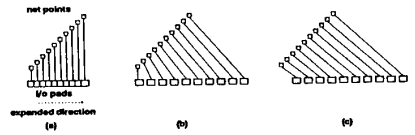

Fig. 7 Sloped interconnection of upstair-net points to I/o pads.

pads have two expanded directions, i.e., left and /or right, and there are three schemes for connecting between them with sloped interconnections, as shown in Figs. 5(b), (c) and (d). The interconnections of the downstair-net points to their corresponding i/o pads have only one expanded direction (i.e., left), and two schemes are needed for connecting between them with sloped interconnections, as shown in Figs. 6(b) and (c). The interconnections of the upstair-net points to their corresponding i/o pads have also only one expanded directions (i.e., right), and two schemes are required for connecting between them with sloped segments, as shown in Figs. 7(b) and (c).

The determination of net points in a zone may be referred to the above three cases. If some of net paths directly connect to the corresponding i/o pads without any bends, the net points can be classified to parallel-net points and the location of the net points are equal to the upper boundary of the zone. If some of net paths are connected to the corresponding i/o pads with a bend, the net points can be classified to upstair -net or downstair-net points. Consequently, the determination of i/o pads thus depend on the net points and the size of i/o-pad shape.

To obtain these sloped and corrected interconnection segments between the net points and i/o pads, it is necessary to estimate whether the locations of the net points are reasonable. If the sloped interconnections cannot be ensured, the net points may be refined. That is, the parallel-net points may be transformed to downstair-net or upstair-net points, and the downstair-net and upstair-net points may be interchanged by modifying some of original segments.

Once the locations of the net points and i/o pads are determined, the slope interconnections between them can be computed. Fig. 8 shows the

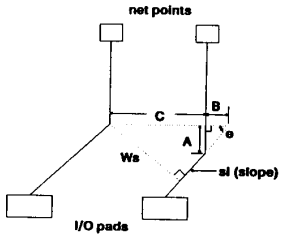

Fig. 8 Computation of a sloped interconnection between net points and I/o pads.

computation of a sloped segment. In Fig. 8, Ws, C, θ, and sl are known constant variables while A and B are unknown variables; where Ws is a minimal space between two wire segments, C is a distance between two net points, sl is a slope of the sloped segment located in the right side, and θ is an angle obtained by $\tan^{-1}(sl)$. The purpose is to determine the left segment located in the left side, that is, to compute the value of A for obtaining this sloped segment. Therefore, the procedure of computing the value of A is introduced as follow.

Since $\theta = \tan^{-1}(sl)$, the value of Ws is by

$$Ws = (B + C) \sin \theta$$

and the value of B can be calculated by the equation $B = Ws / \sin \theta - C$

Also, the value of A can be obtained by the equation $A = B \tan \theta$

Substitute $B = Ws/\sin\theta - C$ for this equation and simplify it, finally, the value of A is

$$A = (Ws / \sin \theta - C) \tan \theta$$
$$= Ws / \cos \theta - C (sl)$$

Once the value of A is calculated, the sloped segment in the left side of Fig. 8 is thus determined. Similarly, a number of sloped segments expanded from right to left (or from left to right) can be obtained by using this procedure. Therefore, the sloped interconnection between the net points and their i/o pads in a zone can be completed. Finally, an MCM with largely reducing space area can thus be generated . For example, Fig. 9 shows the layout result obtained from Fig. 2 with sloped interconnection.

2.3 Power/Ground Layout

Since the bottom two metal layers are respectively distributed to power and ground nets in the hybrid technology of MCM, the routing of power and ground nets can easily be done and independent of the signal nets. For simplicity, if two-row-pad chips are included in the MCM, the power and ground mount pads are arranged as the inner row and the power and ground i/o pads can be refined to proper locations according to the manner of the power/ground layout.

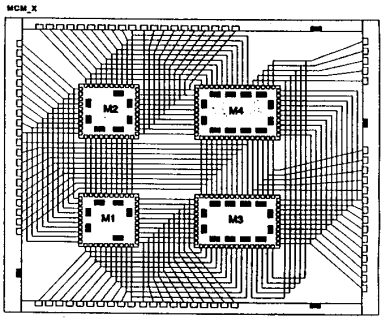

Fig. 9 Sloped interconnection layout of an MCM example mcm_x.

3. EXPERIMENTAL RESULTS

A primary version of the hybrid routing on MCM has been implemented using the standard C language and run on a SUN III/160 workstation under Berkeley 4.2 UNIX operating system. Table 1 shows the experimental results, two MCM examples are specially constructed and used to evaluate our approach. One example, mcm_x, which consists of four chips, 82 nets, 200 mount pads, and 80 i/o pads, and takes a cpu time of 14.18 seconds, is shown in Fig. 9. Another example, mcm_y shown in Fig. 10 consists of eight chips, 268 nets, 770 mount pads, and 120 i/o pads, and takes a cpu time of 51.41 seconds. These primary results showed that the performance of our hybrid routing, with special treatment in the stage of i/o pad sloped interconnection, is very encouraging.

Table 1 Eeperimental Results

example	nets	mount pads	i/o pads	cpu_time
MCM_X	82	200	80	14.18s
MCM_Y	268	770	120	51.41s

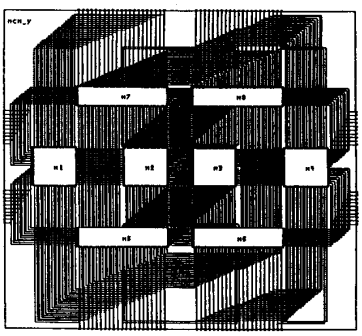

Fig. 10 Hybrid layout of the MCM example mcm_y consisting of eight chips, 770 mount pads, and 120 i/o pads.

4. CONCLUSION

Since the hybrid package technology is frequently used in building high performance computer systems, the routing within multichip modules (MCM) on a hybrid package is worth being studied. We have presented and implemented a new hybrid routing on MCM with this hybrid technology . The routing approach first proposed a new concept that the interconnection between two terminals with a slope can reduce the (moat) space area of MCM. This concept is currently extended to other traditional routing algorithms.

5. ACKNOWLEDGMENT

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