Improved asymmetrical half-bridge converter using a tapped output inductor filter

Y.-H. Leu and C.-L. Chen

Abstract: The asymmetrical half-bridge converter (AHBC) has the attractive features of zero voltage switching (ZVS) and voltage clamping. However, the converter is not suitable for wide input voltage range applications since it has the problem of a 50% maximum allowable duty cycle. A new AHBC topology with a tapped output inductor filter is proposed that not only extends the allowable operating duty cycle but also makes the ZVS condition less stringent. The principle of operation is explained and analysed. Experimental results obtained from a 24 V/3 A prototype are presented, which illustrate converter function and verify the analytical results.

List of symbols

D	duty cycle of switch S_1
i_{S1_pk}	peak current of switch S_1
i_{S2_pk}	peak current of switch S_2
i_{mDC}	average value of magnetising current
i_{mpk}^{+}	positive peak value of magnetising current
i_{mpk}^{-}	negative peak value of magnetising current
i_p	instantaneous current of leakage inductor L_l
i_{D1}	instantaneous current of output rectifier D_1
i_{D2}	instantaneous current of output rectifier D_2
I_{D1_RMS}	root-mean-square current of output rectifier D_1
I_{D2_RMS}	root-mean-square current of output rectifier D_2
V_C	average voltage across blocking capacitor C_b
T	transformer
A_e	effective cross-sectional area of the core of transformer T
L_M	magnetising inductor of transformer T
L_M	magnetising inductance for transformer T
L_l	leakage inductor
L_l	leakage inductance
n	turns ratio of transformer T
N_P	number of turns of transformer primary winding
N_1	number of turns of the first winding of the tapped-inductor
N_2	number of turns of the second winding of the tapped-inductor
k	windings ratio coefficient, which is defined as N_1/N_2
L_{N1}	inductance of the first winding of the tapped-inductor
L_{N2}	inductance of the second winding of the tapped-inductor
$i_{L_{N2}}$	current flows through L_{N2}
T_S	switching period of converter
f_S	switching frequency of converter

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1 Introduction

For low to medium power level applications, topologies derived from an asymmetrical half-bridge converter (AHBC) have been widely discussed due to their smaller component counts, lower stress on the power switch, and soft-switching phenomenon [1–8]. Among these topologies, the AHBC has a higher efficiency due to its lower root-mean-square (RMS) current of the output rectifiers. Fig. 1 shows the basic circuit of the converter. However, the converter has the problem of a 50% maximum allowable duty cycle [3–6]. This makes the converter unsuitable for operating within a wide input voltage range. Moreover, the voltage stress of the output rectifier depends on the operating duty cycle. If the operating duty cycle is adjusted to 50%, these two rectifiers will be under the same voltage stress. Thus, a lower voltage drop diode can be used and the conductive and switching loss of the rectifiers can be reduced.

In recent years, little effort has been expanded on extending the maximum allowable duty cycle of an AHBC

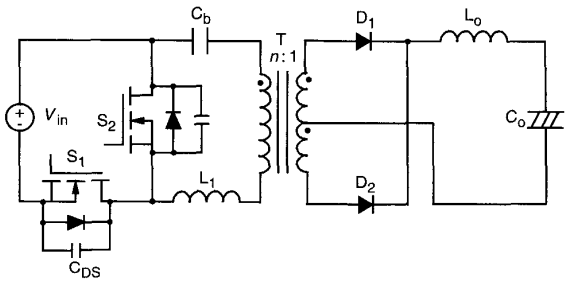

Fig. 1 *Simplified schematic of the AHBC*

[7, 8]. The two-transformer AHBC was proposed in 1999 [7]. By tuning the individual turns ratios of the two transformers, the maximum allowable duty cycle can be extended to be over 50%. However, this is at the price of an increased complexity and cost.

The problem of duty cycle limitation in an AHBC will now be addressed. A modified circuit will be proposed. Fig. 2 shows the basic circuit diagram. As the Figure indicates, the converter has the same components count as in Fig. 1. The only difference is that in the output inductor filter, a tapped-inductor replaces the one-winding inductor. By tuning the ratio of the number of windings of the tapped-inductor, the operating duty cycle of the converter can be extended to be over 50%. Compared with a conventional AHBC, the zero voltage switching (ZVS) condition and current stress on the power switch of the proposed converter are reduced. Additionally, the basic principle of operation and its steady-state characteristics will be analysed. The design considerations are given according to the analysis. To demonstrate the effectiveness of the characteristic performances, experiments are carried out with a 24 V/3 A, 120 kHz prototype.

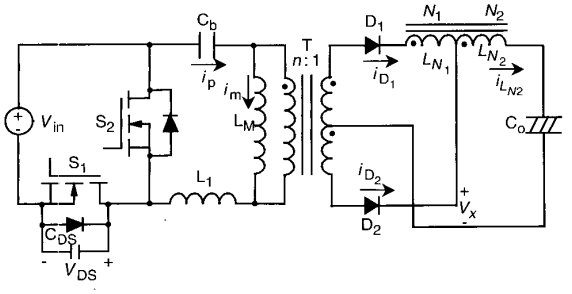

Fig. 2 *Tapped-inductor type AHBC*

2 Circuit description of the proposed converter

Referring to Fig. 2, the power switches S_1 and S_2 are driven alternately, but with a short blocking interval. L_l represents the leakage inductor of the transformer T, while C_{DS} represents the junction capacitor of S_1 and S_2. N_1, N_2 are the two windings of tapped-inductor, with the windings ratio coefficient, k, being is defined as N_1/N_2. Note that, when k is zero, the AHBC can be considered as being a special case of the proposed converter. The principle of operation and the steady-state analysis are illustrated with the following assumptions:

1. the converter operates under steady-state conditions;
2. the output filter operates in continuous conduction mode;
3. switching components are ideal; and
4. C_b is large enough, so that the voltage across it is constant.

The operating principle for one switching cycle is divided into eight stages, and the equivalent circuits for each one is illustrated in Fig. 3. The solid lines denote the current conducting paths. Fig. 4 shows the key waveforms of the converter. The operating behaviour of the converter will now be described.

t_0–t_1: S_1 and D_1 conduct before t_0. C_b, L_M, and L_l are charged by the input source. The transformer provides the electrical isolation between the input and the output sides, and transfers energy to the output. During this interval, the tapped-inductor works as a one-winding inductor and stores energy.

t_1–t_2: S_1 is turned off at t_1. C_{DS} is charged by the primary current, which is the combination of the magnetising current and the reflected output current. Because the transient interval is so short, the actual resonant charging manner is approximated as a linear charging characteristic.

t_2–t_3: At t_2, D_2 is forward biased. The output current circulates through D_1 and D_2. L_l and C_{DS} form a resonant network. During the interval, the voltage $V_{DS}(t)$ and the primary current $i_p(t)$ can be formulated as:

$$i_P(t) = i_P(t_2)\cos\omega_r(t-t_2) \tag{1}$$

$$V_{DS}(t) = \left[V_{in} - V_C + n\frac{kV_O}{(k+2)}\right] + i_P(t_2)\sqrt{\frac{L_l}{C_{DS}}}\sin\omega_r(t-t_2) \tag{2}$$

where, $\omega_r = 1/\sqrt{L_l \times C_{DS}}$, $k = N_1/N_2$.

t_3–t_4: After C_{DS} is charged to the input voltage at t_3, the anti-parallel diode of S_2 starts to conduct. To achieve ZVS operation and reduce the conduction loss for S_2, the switch should be turned on before the primary current changes direction. The voltage across the leakage inductor can be expressed by:

$$V_{L_l} = V_{in}\left[\frac{-D}{1+k(1-D)}\right] \tag{3}$$

The negative voltage across the leakage inductor makes the primary current i_p, decrease in a linear manner. This causes the current of D_1 to quickly decrease. When the current has reduced to zero, the device is off and this stage ends.

t_4–t_5: During this interval, the energy stored in the tapped-inductor starts to discharge. Because the inductor remains at a smaller value, the reflected current is larger than that in the AHBC. The larger reflected current contributes to the ZVS operation of the low-side switch, S_1.

t_5–t_6: At t_5, S_2 is turned off. The primary current discharges C_{DS}, and V_{DS} decrease linearly. This stage ends when the V_{DS} increases to forward bias D_1.

t_6–t_7: In this stage, D_1 and D_2 again simultaneously conduct. L_l and C_{DS} resonate. The $V_{DS}(t)$ and $i_p(t)$ are found as:

$$i_P(t) = i_P(t_6)\cos\omega_r(t-t_6) \tag{4}$$

$$V_{DS}(t) = \left[V_{in} - V_C + n\frac{kV_O}{(k+2)}\right] + i_P(t_6)\sqrt{\frac{L_l}{C_{DS}}}\sin\omega_r(t-t_6) \tag{5}$$

Supposing the energy stored in L_l is sufficient to discharge C_{DS} completely, the voltage across C_{DS} will be zero. The primary current can flow through the anti-parallel diode of S_1.

t_7–t_8: After V_{DS} decreases to zero, the voltage across the leakage inductor is:

$$V_{L_l} = V_{in}(1-D)\left[\frac{1+k}{1+k(1-D)}\right] \tag{6}$$

The positive voltage causes a rapid change rate in the primary current and D_2 current. Before the primary current changes polarity, S_1 should be turned on to ensure ZVS operation. At t_8, the current of D_2 is zero. D_2 turns off, and another switching cycle starts ($t_8 = t_0$).

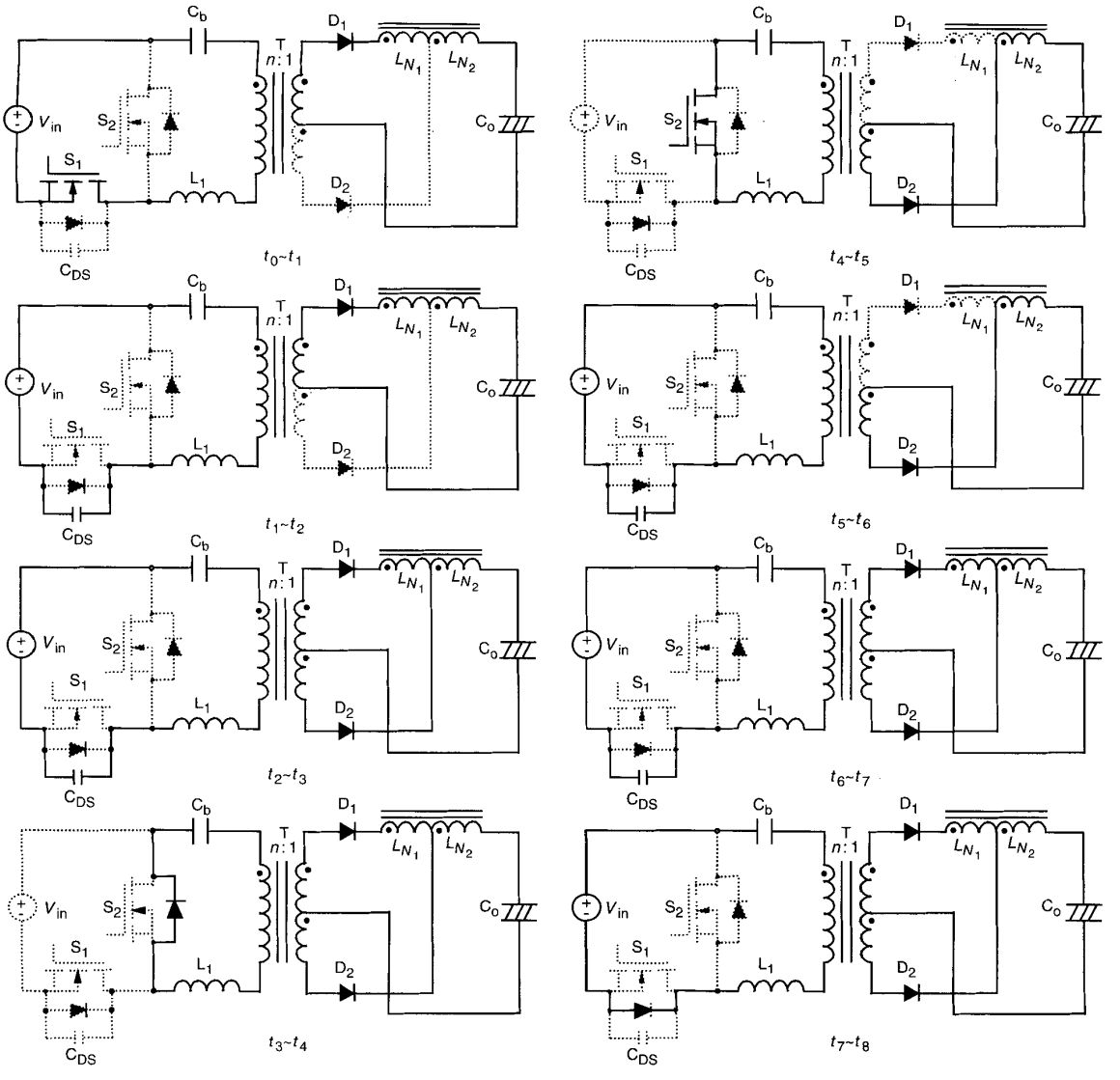

Fig. 3 *Eight topological states of the proposed converter*

3 Characteristics of the proposed converter

This section analyses the key improved characteristics of using a tapped-inductor in a AHBC.

3.1 Static voltage transfer ratio

In a switching cycle, the average flux variation of the magnetising inductor should be zero. Therefore, the voltage transfer ratio can be derived as:

$$\frac{V_O}{V_{in}} = \frac{1}{n}\left[\frac{(k+2)D(1-D)}{1+k(1-D)}\right] \tag{7}$$

Also, the maximum allowable operating duty cycle of the converter is:

$$D_{max} = \frac{(k+1)-\sqrt{(k+1)}}{k} \tag{8}$$

From (7), the voltage transfer ratio is a function of k and D. The influence of different k and D values on the voltage transfer ratio is shown in Fig. 5. It is found that the maximum allowable duty cycle of the converter can be extended to be over 50%. In steady-state operation, the voltage stress of the rectifiers is:

$$V_{D_1} = \frac{V_O}{1-D} \tag{9}$$

$$V_{D_2} = \frac{V_O}{D} \tag{10}$$

From (9) and (10), if the operating duty cycle is adjusted to 50%, the rectifiers will be under the same stress.

3.2 RMS current of the output rectifier

In order to simplify the analysis, the dead time between the conduction intervals of the power switches is neglected. Only the stages t_0–t_1 and t_4–t_5 are discussed in this section. The simplified operational circuits for these two stages are shown in Figs. 6*a* and 6*b*. During the D interval, the two inductors are in series and are charged by the input source. During the (1–D) interval, the energy

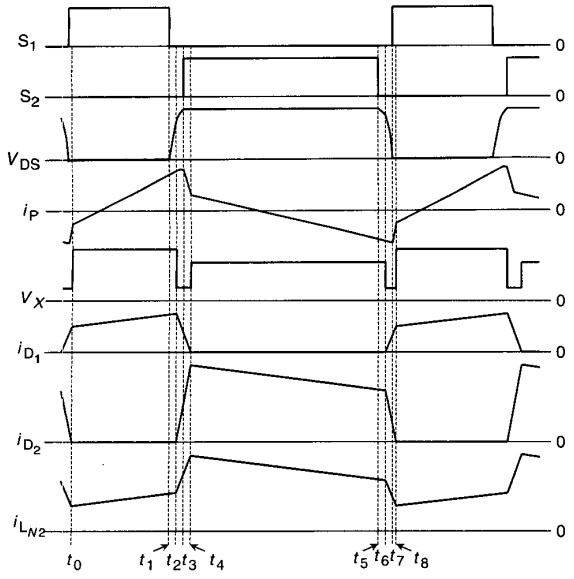

Fig. 4 *Theoretical waveforms on some key components*

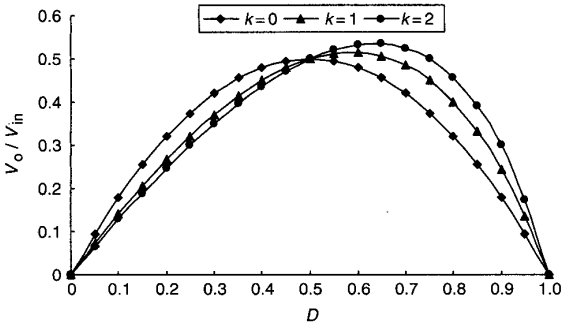

Fig. 5 *Voltage transfer ratio as a function of D, for different value of k*

stored in the two inductors is transferred to the output by L_{N2}. The simplified current waveform of the L_{N2} is shown in Fig. 6*c*.

As the diagram indicates, the relationship of the I_a, I_b, I_c, I_d, and I_O can be formulated as the following equations:

$$(N_1 + N_2)I_b = N_2 I_c \tag{11}$$

$$N_2 I_d = (N_1 + N_2)I_a \tag{12}$$

$$I_O = \frac{(I_a + I_b)D + (I_c + I_d)(1 - D)}{2} \tag{13}$$

$$I_b = I_a + m_1 DT_s \tag{14}$$

where

$$m_1 = \frac{1}{(k+1)(k+2)} \frac{(1-2D)}{D} \frac{V_O}{L_{N2}} \tag{15}$$

By solving (11)–(15), the currents I_a and I_c can be expressed as:

$$I_a = \frac{I_O}{D + (1+k)(1-D)} - \frac{(1-2D)}{2(k+1)(k+2)} \frac{V_O}{L_{N2}} T_S \tag{16}$$

$$I_c = \frac{I_O(1+k)}{D + (1+k)(1-D)} + \frac{(1-2D)}{2(k+2)} \frac{V_O}{L_{N2}} T_S \tag{17}$$

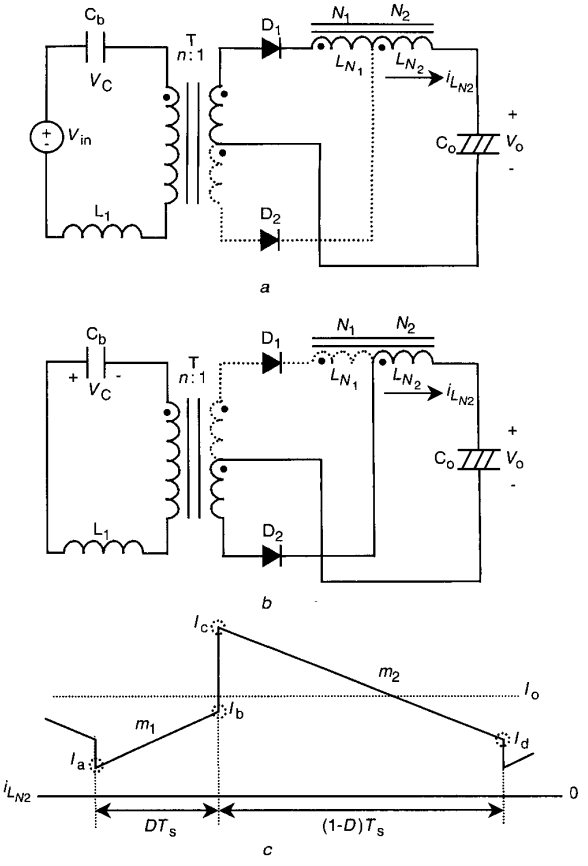

Fig. 6
a Simplified topological state: S_1 on,
b Simplified topological state: S_2 on,
c Simplified current waveforms of L_{N2}

The RMS current of the two rectifiers are:

$$I_{D1rms} = \sqrt{\frac{1}{T_S}\int_0^{DT_S} i_{D1}^2(t)dt} = \sqrt{\frac{1}{T_S}\int_0^{DT_S} [I_a + m_1 t]^2 dt} \tag{18}$$

$$I_{D2rms} = \sqrt{\frac{1}{T_S}\int_{DT_S}^{T_S} i_{D2}^2(t)dt} = \sqrt{\frac{1}{T_S}\int_{DT_S}^{T_S} [I_c + m_2(t - DT_S)]^2 dt} \tag{19}$$

where

$$m_2 = \frac{1}{(k+2)} \frac{(2D-1)}{(1-D)} \frac{V_O}{L_{N2}} \tag{20}$$

Fig. 7 shows the RMS current ratio of the two rectifiers ($IDRatio = I_{D2rms}/I_{D1rms}$) with different winding ratios ($k = 0$ and $k = 1$). It is found that no matter what the ratio is, the larger portion of the output current flows through D_2. At this point, the importance of extending the operating duty cycle is again highlighted. If the operating duty cycle is augmented, a lower voltage drop diode can be used. Moreover, increasing the windings ratio, the uneven current distribution of two rectifiers is worse.

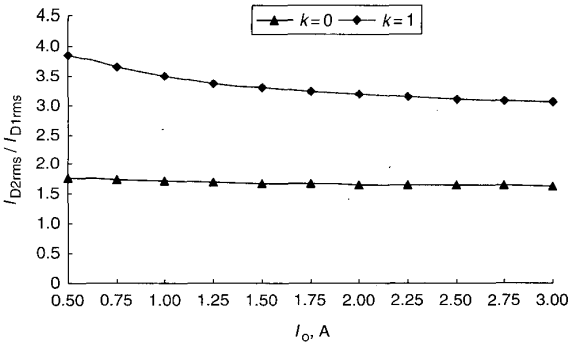

Fig. 7 *RMS current ratio of two output rectifiers as a function of the output current, for different values of k*

3.3 Maximum operating flux density of the transformer

Since the converter is controlled with an asymmetrical duty cycle, the average magnetising current is not zero, but a DC value. The DC value of the magnetising current lowers the transformer utilisation rate. In order to avoid saturation, the average magnetising current has to be taken into consideration in the design. The average input current (I_{in}) and the output current (I_O) should obey the following relationship:

$$\frac{I_{in}}{I_O} = \frac{1}{n}\left[\frac{(k+2)D(1-D)}{1+k(1-D)}\right] \tag{21}$$

The relationship between the average input current and the average magnetising current (I_{mDC}) is expressed by:

$$\frac{I_{in}}{D} = I_{mDC} + \frac{I_O}{n} \tag{22}$$

Substituting (21) into (22) yields:

$$I_{mDC} = \frac{I_O}{n}\frac{(1-2D)}{1+k(1-D)} \tag{23}$$

The average magnetising current is a function of the duty cycle and the winding ratio of the tapped-inductor. The relationship between the average magnetising current and the operating duty cycle for different winding ratios is shown in Fig. 8. It is found that the optimal operating duty cycle of the converter is 50%. If the converter operates at this point, the average magnetising current will be zero. Moreover, a larger winding ratio for the tapped-inductor results in a smaller DC value of the magnetising current. Taking the AC swing into account, the peak magnetising

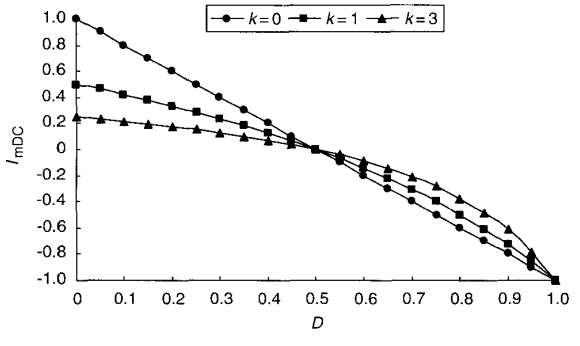

Fig. 8 *Normalised DC value of the magnetising current as a function of D, for different values of k.*

current of the transformer is:

$$i_{mpk}^{+} = \frac{I_O}{n}\frac{(1-2D)}{1+k(1-D)} + \frac{nV_O[1+k(1-D)]}{(k+2)}\frac{T_S}{2L_M} \tag{24}$$

$$i_{mpk}^{-} = \frac{I_O}{n}\frac{(1-2D)}{1+k(1-D)} - \frac{nV_O[1+k(1-D)]}{(k+2)}\frac{T_S}{2L_M} \tag{25}$$

The maximum operating flux density of the transformer is:

$$B_{max} = \left[\frac{L_M I_O(1-2D)}{nN_P A_e[1+k(1-D)]} + \frac{nV_O[1+k(1-D)T_S]}{2N_P A_e(k+2)}\right] \times 10^8 \tag{26}$$

3.4 ZVS transition

The ZVS condition for the two switches can be derived from (2) and (5). Before S_2 is turned on, V_{DS} should increase to match the input voltage. Before S_1 is turned on, V_{DS} should decrease to zero. Equations (27) and (28) quantitate the ZVS condition for S_2 and S_1, respectively.

$$L_l|i_p(t_2)|^2 \geq C_{DS}\left[V_c - \frac{nkV_O}{(k+2)}\right]^2 \tag{27}$$

$$L_l|i_p(t_6)|^2 \geq C_{DS}\left[V_{in} - V_c + \frac{nkV_O}{(k+2)}\right]^2 \tag{28}$$

where the current $i_p(t_2)$ and $i_p(t_6)$ can be approximated as:

$$i_p(t_2) \cong \frac{I_b}{n} + i_{mpk}^{+} \tag{29}$$

$$i_p(t_6) \cong \frac{I_d}{n} + i_{mpk}^{-} \tag{30}$$

From (27) and (28), it is found that whether or not ZVS operation is achieved depends on how much energy is stored in L_l. A larger leakage inductance is helpful to achieve ZVS operation of both switches. Fig. 9 shows the required value of the leakage inductance for ZVS operation at different winding ratios for the studied converter. As the Figure indicates, the ZVS condition of S_1 is stricter than S_2. Utilising a tapped-inductor in the output filter, means that the ZVS condition for S_2 can be reduced.

4 Design considerations

In this Section, the design considerations of the proposed converter are developed according to the analytical results. They can be described as follows:

4.1 Operating duty cycle

Determining the operating duty cycle is the first step. The optimal operating duty cycle of the AHBC is 50%. If the converter operates at this point, not only will the output rectifiers be under the same stress, but also the average magnetising current will also be zero. Equation (8) formulates the maximum allowable duty cycle of the proposed converter. If the winding ratio of the tapped-inductor is one, then the maximum allowable duty cycle can be extended to 0.586. In order to bear the load disturbance and duty loss, it is recommended to set the operating duty cycle it to be 40%.

The drawback of using a tapped-inductor is that an unbalanced output current flows through the output rectifiers. As indicated in Fig. 7, the larger k is, the more parts of the output current flow through D_2. Therefore, it is necessary to reconcile the winding ratio of the tapped-inductor with the operating duty cycle.

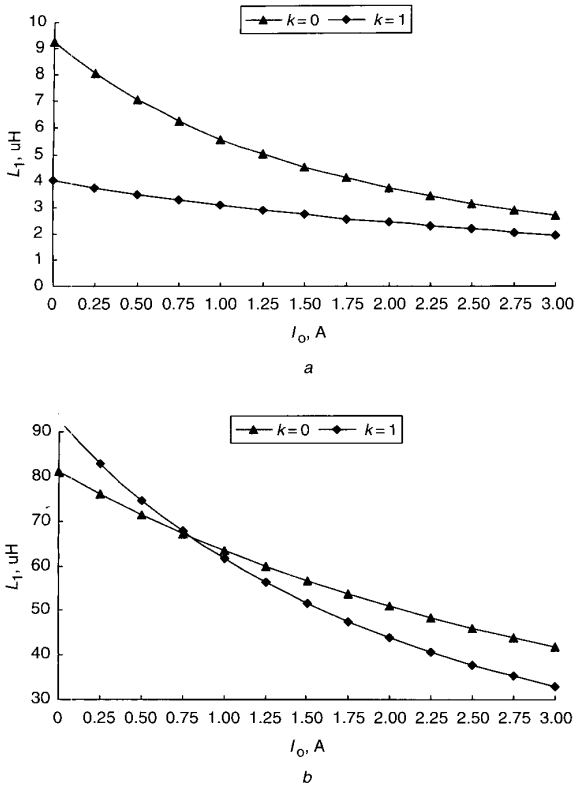

Fig. 9 *The required leakage inductance as a function of different ZVS range operation of the switches, for different values of k*
a Required values for S_2
b Required values for S_1

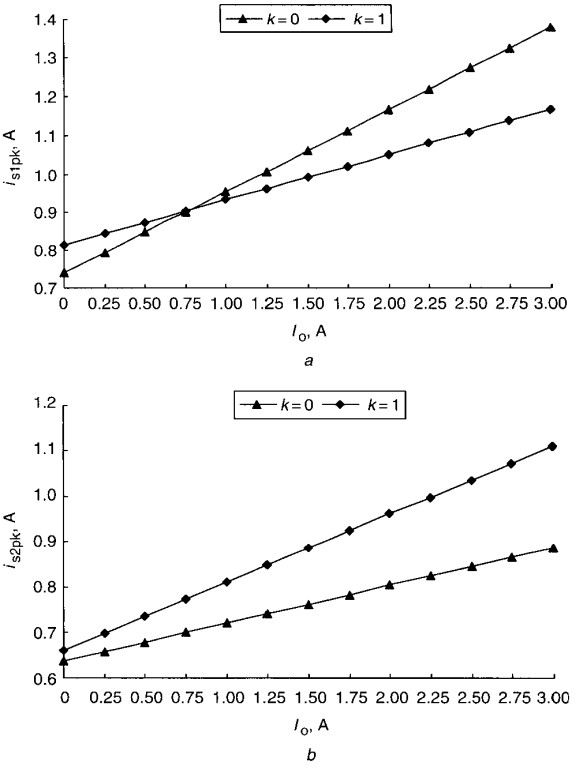

Fig. 10 *Current stress of the switches as a function of the output current, for different values of k*
a Peak current values of S_1
b Peak current values of S_2

4.2 Power switch

Referring to Fig. 4, the peak currents of S_1 and S_2 (i_{S1_pk}, i_{S2_pk}) are the same as the positive and negative peak values of the primary current, respectively. These currents can be expressed as:

$$\begin{aligned} i_{S1\_pk} &= i_p(t_2) \\ &= \frac{I_b}{n} + i^+_{mpk} \\ &= \frac{1}{n}\left[\frac{I_O}{D+(1+k)(1-D)}\right. \\ &\quad \left. + \frac{(1-2D)}{2(k+1)(k+2)}\frac{V_O}{L_{N2}}T_S\right] \\ &\quad + I_{mDC} + \frac{1}{2}\frac{V_{in}(1-D)}{L_M}DT_S \end{aligned} \tag{31}$$

$$\begin{aligned} i_{S2\_pk} &= -i_p(t_6) \\ &= -\left[\frac{I_d}{n} + i^-_{mpk}\right] \\ &= \frac{-(1+k)}{n}\left[\frac{I_O}{D+(1+k)(1-D)}\right. \\ &\quad \left. - \frac{(1-2D)}{2(k+1)(k+2)}\frac{V_O}{L_{N2}}T_S\right] \\ &\quad - I_{mDC} + \frac{1}{2}\frac{V_{in}(1-D)}{L_M}DT_S \end{aligned} \tag{32}$$

Figs. 10*a* and 10*b* show the peak currents of S_1 and S_2 (i_{S1_pk}, i_{S2_pk}) under different loadings for different values of the windings turn ratio (k). When $k=0$, the peak current stress of S_1 is 1.4 A at full load, and the stress of S_2 is 0.85 A. When $k=1$, the peak current stress of both switches is about 1.1 A at full load. This shows the current stress of the switches is more balanced by using a tapped-inductor in the AHBC. Additionally, the voltage stresses of the switches is the input voltage.

4.3 Transformer magnetising inductors

The DC magnetising current of the transformer affects the utility rate of the magnetic material. In a practical design, the DC value has to take this into account. If the useable flux density of the material is B_{sat}, the maximum allowable magnetising inductance can be derived from (26), and the value is:

$$\begin{aligned} L_M \le &\left[B_{sat}\times 10^{-8} - \frac{V_{in}D(1-D)T_S}{2N_pA_e}\right] \\ &\times \frac{nN_PA_e[1+k(1-D)]}{I_O(1-2D)} \end{aligned} \tag{33}$$

4.4 Leakage inductor

As the above-mentioned, in order to achieve a ZVS operation of the switch, the leakage inductor must store sufficient energy to charge/discharge C_{DS}. If the ZVS operating range is chosen, the minimum value of the required leakage inductance can be derived from (28).

5 Experimental results

A 120 kHz 24 V/3 A prototype is implemented for verification. The specifications of the converters are:

- input voltage: 400 V DC;
- output voltage: 24 V DC;
- maximum load current: 3 A;
- switching frequency: 120 kHz;
- normal operation duty cycle: 0.34.

The circuit parameters are listed as:

power switches S_1 and S_2: Fuji, 2SK2645, $R_{DS(on)} = 1\,\Omega$;
output diodes D_1 and D_2: IR, 10CTQ150, $V_F = 0.73$ V;
transformer T: A_e of core: 1 cm^2; W_1: 27 turns of Litz wire 50×0.1 mm; W_2: 4 turns of Litz wire 50×0.1 mm;
tapped-inductor: $k = 1$, $L_{N1} = 15\,\mu$H, $L_{N2} = 15\,\mu$H;
magnetising inductance L_M: 470 μH;
leakage inductance L_l: 20 μH.

Fig. 11 shows the experimental waveforms on some key components of the studied converter under half-load operation. These waveforms are arranged in the same order as in Fig. 4. It is shown that the experimental results coincide with the analysis. As mentioned earlier, the current $i_p(t_2)$ and $i_p(t_6)$ play crucial roles in the ZVS operation of the switches. Fig. 12 shows the predicted and experimental values of these currents. It is shown that the calculated values are very close to the measured values. Fig. 13 shows the predicted and experimental RMS currents of D_1 and D_2 under different loadings. The calculated current of D_1 is larger than the experimental ones, but the result is the opposite in D_2. The reason for this is that the duty loss of the converter is neglected in the analysis. In order to

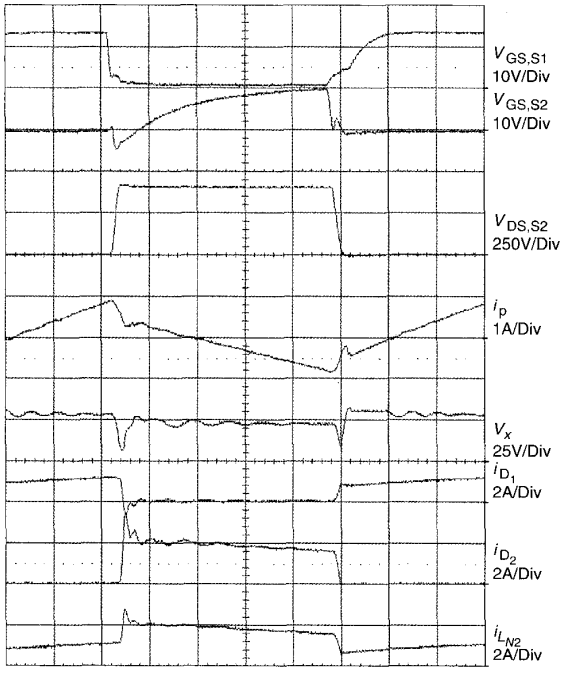

Fig. 11 *Experimental waveforms on key components. (Time scale is 1 us/div)*

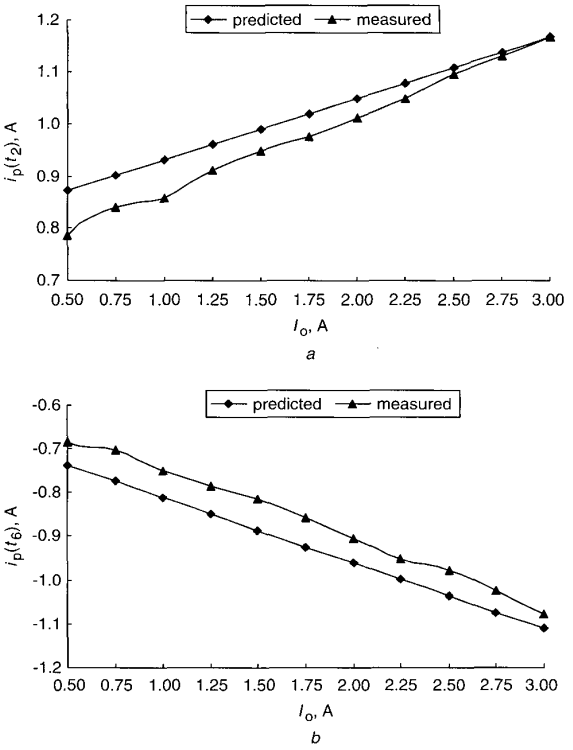

Fig. 12 *Experimental and predicted values of the primary current as a function of the output current*
a The values at time, t_2
b The values at time, t_6

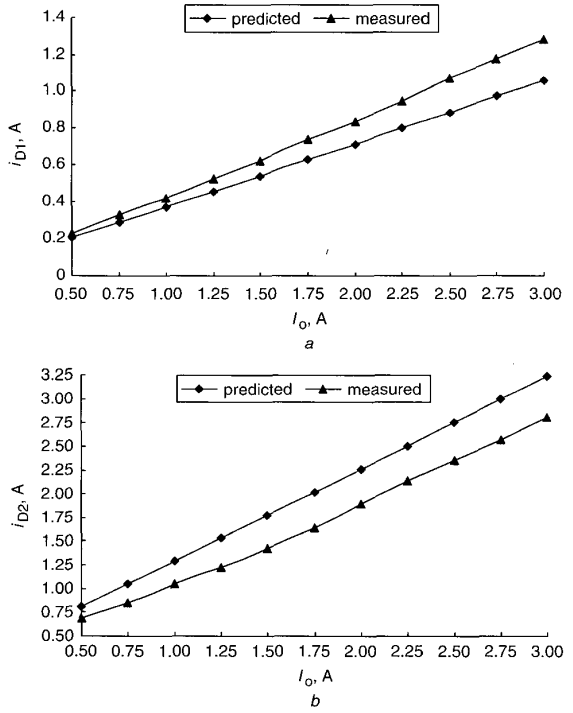

Fig. 13 *Experimental and predicted RMS current of the rectifiers as a function of the output current*
a the value of D_1
b the value of D_2

regulate the variation of the output voltage caused by the load disturbance, the operating duty cycle of S_1 must be increased, this will result in more current through D_1 and less through D_2. The overall efficiency was measured under different values for the output current range at different winding ratios, as shown in Fig. 14. The efficiency of the tapped-inductor type AHBC is higher than that of non-tapped-inductor type under a heavy load. However, the efficiency is worse under a light load. This is because using a tapped-inductor in a AHBC is not conducive to the ZVS operation of S_1 under light load. The efficiency of the two converters exceeds 90% under full load operation.

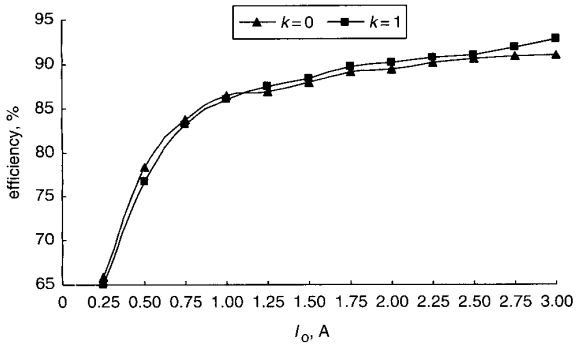

Fig. 14 *The measured efficiency as a function of the output current, for different values of k*

6 Conclusions

The AHBC is considered a suitable topology for low to medium power level applications. However, it has the problem of a 50% maximum allowable duty cycle. A new AHBC topology using a tapped output inductor filter has been proposed to solve the problem. From the analytical and experimental results, several advantages of a larger windings ratio coefficient of the tapped-inductor have been observed: (i) the maximum allowable duty cycle of the AHBC can be extended; (ii) the ZVS condition and current stress on the power switches can be reduced; (iii) the transformer utilisation rate is better; and (iv) a higher efficiency is obtained under a heavy load.

The only shortcoming is that the uneven current distribution of two rectifiers would be worse.

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