Turn-on Transient Imposed Extrinsic Base Consideration in BiNMOS Transistors

Yen-Wen Chen and James Kuo
Dept. of Electrical Eng., National Taiwan University
Taipei, Taiwan
FAX:886-2-363-8247, Telephone:886-2-363-5251

Abstract

This paper presents a detailed two-dimensional numerical simulation study on the bipolar devices in the BiCMOS circuit environment during turn-on transient. The unique charge build-up and removal phenomenon in the bipolar device determines the switching speed of the BiNMOS devices. The tradeoffs in designing the extrinsic base in terms of the switching behavior are also described. It is shown that the structure with the extrinsic base P+ area farthest from the intrinsic base area has the best switching speed owing to the largest overshoot in the base voltage initially and the lateral base effects.

Summary

NMOS and the bipolar devices are the most important part during the pull-down transient of a BiCMOS inverter[1]-[4]. It has been shown that the extrinsic base doping profile has a strong impact on the steady state performance of bipolar devices[5]-[7]. In addition, lateral base effects in bipolar devices are important during turn-on and turn-off transients[8]-[11]. The transient behavior of the bipolar devices in the BiCMOS circuit environment is different from that in standard bipolar circuits[12]-[13]. In this paper, the transient phenomenon of the bipolar device in a BiNMOS circuit environment is studied. This detailed study is based on a two-dimensional device simulator—PISCES[14].

Fig. 1(a) shows the cross section of the BiNMOS device based on a $1.2\mu m$ BiCMOS technology[15]. Here, NMOS devices without an LDD structure have been used in the study. The NMOS device has an effective channel length of $1\mu m$, a gate oxide thickness of $250\AA$, and a threshold voltage of $0.8V$. The NMOS device and the bipolar device are placed against each other separated by an oxide of $5000\AA$. The base and the source terminals are wired together with a parasitic capacitance of $0.1fF$. The collector and the drain contacts are connected by an interconnect where an output capacitive load of $0.1pF$ is placed. S is the distance between the edges of the ion-implantation masks for the emitter and the extrinsic base. D is the distance between the edge of the base contact and the edge of the ion-implantation mask for the extrinsic base ($D = 1.2\mu m - S$). Fig. 1(b) shows the vertical doping profile in the intrinsic and the extrinsic base regions. The intrinsic base has a width of $0.1\mu m$ and a peak concentration of $1 \times 10^{18} cm^{-3}$. For simplicity, metal contact to the emitter has been used. Gaussian vertical profiles and lateral straggles equivalent to 80% of the vertical ones have been assumed in the intrinsic and extrinsic base regions. Bandgap narrowing[16] and Shockley-Read-Hall and Auger recombinations[17] have been used in the simulations.

Fig. 2 shows the steady state performance of the BJT device. Three cases show similar curves in the Gummel plot as shown in Fig. 2(a), except for the base current at a high level. The $0.4\mu m$ case shows the least base current and consequently the highest current gain, β, as shown in Fig. 2(b). No matter what extrinsic base structure is, three cases show similar f_T's as shown in Fig. 2(c), except at a high current, where the $0.4\mu m$ case has the highest f_T. Little difference in the base-to-emitter capacitance is observed among three cases as shown in Fig. 2(d), except at a high current, where the $0.4\mu m$ case has the lowest diffusion capacitance. The base resistance, which is strongly dependent on the extrinsic base doping, affects both DC and transient performance. The base resistance has been extracted for a very low current level by directly measuring the voltage drop between the base electrode and the center of the intrinsic device area [13]. Based on the voltage drop and the base current, the base resistance has been extracted as shown in Fig. 2(e). The $0.4\mu m$ case shows the highest base resistance at a low current, where the base resistance is dominated by the extrinsic region. At a high current, the difference in base resistance among three cases is little. Based on the steady state performance, the case with the farthest extrinsic base contact has the best current gain, the worst base resistance overall and the highest unity gain frequency and the worst base-to-emitter capacitance at a high current. All the parameters obtained assume the steady state and small signal condition. However, for the BiNMOS transistor operating in the large signal regime, these parameters cannot accurately describe the behavior during the transient operations. In order to study the performance of the BiNMOS transistor, turn-on transient analysis is now described.

By imposing a voltage step from 0V to 5V in 10ps, the turn-on transient behavior of the BiNMOS device has been obtained for cases with $D = 0.4\mu m$, $0.6\mu m$, and $0.8\mu m$. Figs. 3 to 8 show the terminal voltages and currents during the turn-on transient. As shown in Fig. 3, during the input ramp-up period, there are overshoots in magnitude of the NMOS source current (I_M) and the base current (I_B). The difference in magnitude between I_M and I_B equals the magnitude of the current flowing into the internal capacitive node (I_{CP}). The overshoot in I_{CP} around $10ps$ is small due to the small parasitic capacitance, C_P. However, a substantial overshoot in the base current exists during the initial ramp-up period. Fig. 4 shows the base voltages for the cases with $D = 0.4\mu m, 0.6\mu m, 0.8\mu m$ during the initial $80ps$ period. The peak in V_B is determined by the gate-to-source overlapped capacitance and the total equivalent capacitance at the base node—mainly the parasitic capacitance (C_P) and the base-to-emitter capacitance (C_{BE}). The $D = 0.4\mu m$ case (with the extrinsic base P+ area farthest from the emitter) shows the highest overshoot in the base voltage owing to the smallest C_{BE}. Compared to the base currents during transient for other bipolar circuits [18]-[22], the overshoot in the base voltage during the input ramp-up period is a unique phenomenon in the BiNMOS device. Fig. 5 shows the corresponding base currents for the cases with $D = 0.4\mu m, 0.6\mu m, 0.8\mu m$ during the initial $30ps$ period. Despite the largest overshoot in the base voltage for the $D = 0.4\mu m$ case, the overshoot in the base current is the smallest among three cases. Fig. 6 shows the base and the collector voltages for three cases during the overall $1ns$ period. After the input ramp-up period, the base voltages settle to their steady values. The $D = 0.4\mu m$ case has the highest base voltage before $450ps$ and the lowestbase voltage after it. During transient, the collector voltage for the $D = 0.4\mu m$ case is always the lowest, which indicates the best switching speed. Figs. 6 and 7 show the base and collector currents for three cases during transient. After the input ramp-up period, the base voltage remains steady until $300ps$. In the mean time, the collector current is increasing monotonically. At $300ps$, the collector currents reach their peaks. However, I_C/I_B of the bipolar device is still much less than its dc value. After $300ps$, both the base and the collector currents are decreasing. During this period, the $D = 0.4\mu m$ case demonstrates the smallest base current and the largest collector current.

Fig. 9 shows the 2D electrostatic potential(Ψ) in the bipolar device area during transient for the $D = 0.4\mu m$ case. Initially, substantial potential gradients from emitter to collector and equal potentials at the base and the emitter nodes can be observed. At the end of the

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ramp(10ps), a potential difference of over 1V between the base and the emitter nodes can be seen. At 60ps, the intrinsic base area widens vertically and laterally. At 450ps, the 2D base push-out phenomenon is substantial. Finally, at 1000ps, small potential gradients can be observed in the whole device region. More insight into designing bipolar devices for BiCMOS circuits can be obtained by examining total electrons in the bipolar device during transient as shown in Fig. 10. All three cases with $D = 0.4\mu m$, $0.6\mu m$, $0.8\mu m$ show similar bell-shape curves. Total electrons increase monotonically in the bipolar area until 0.45ns and decrease after it. This indicates the unique electron build-up and removal phenomenon in the bipolar area, which determines the switching speed of the BiNMOS device. The $D = 0.4\mu m$ case shows a much higher value in total electrons during transient. Despite its largest value in total electrons to build and to remove during transient, the $D = 0.4\mu m$ case demonstrates the best switching speed.

Fig. 11 shows the 2D electrostatic potential(Ψ), electron(n) and hole(p) concentration contours for the cases with $D = 0.4\mu m$, $0.6\mu m$, $0.8\mu m$ at 450ps. 2D base push-out phenomenon exists for all three cases. From the 2D electrostatic potential, electron and hole concentration contours, especially the $n = 10^{17}cm^{-3}$ electron contour, the $D = 0.4\mu m$ case shows the most severe base push-out behavior in the lateral base direction. On the other hand, it doesn't have the worst base push-out in the intrinsic base area. This is due to the most voltage drop resulting from the extrinsic base resistance along the lateral base direction. In addition, thanks to the smallest initial C_{BE} and the largest β and f_T, the $D = 0.4\mu m$ case does show the best switching speed despite the largest extrinsic base resistance and the worst base push-out to handle during transient.

Acknowledgments

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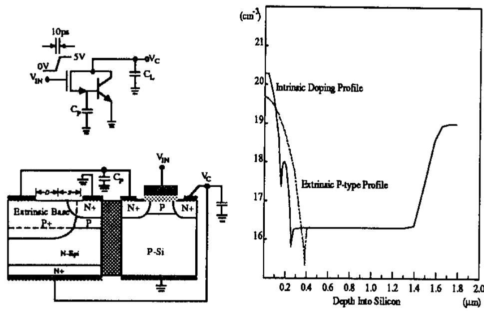


Fig. 1. (a) The BiNMOS device structure under study. S is the distance between the edges of the ion-implantation masks for the extrinsic base and the emitter. D is the distance between the edge of the base contact and the edge of the ion-implantation mask for the extrinsic base. (b) Vertical doping profiles in the intrinsic and the extrinsic base areas.

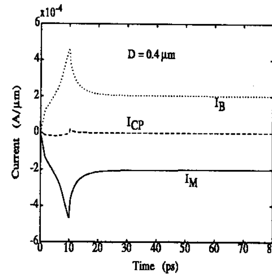


Fig. 3. The base current I_B, the NMOS source current (I_M and the current flowing into the internal parasitic capacitive node (I_{CP}) for the case with $D = 0.4\mu m$ during the initial $80ps$ period.

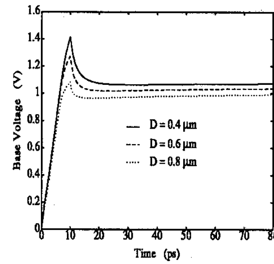
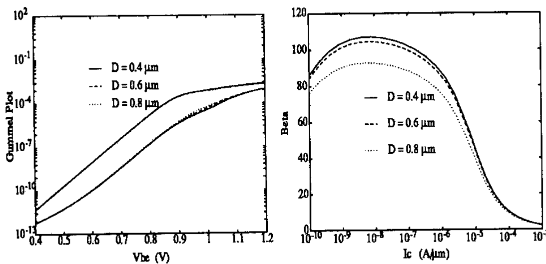
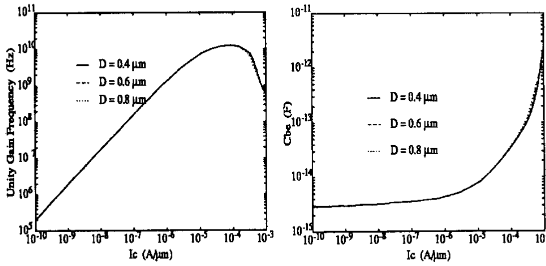


Fig. 4. The base voltages (V_B) for the cases with $D = 0.4\mu m$, $0.6\mu m$, $0.8\mu m$ during the initial $80ps$ period.





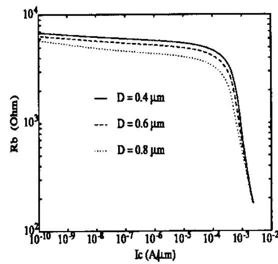


Fig. 2. DC performance of the bipolar device. (a) Gummel plot. (b) The current gain. (c) The unity gain frequency. (d) The base-to-emitter capacitance. (e) The base resistance.

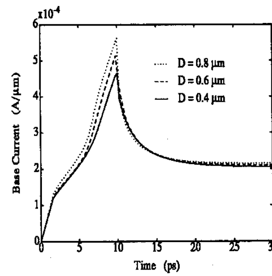


Fig. 5. The base currents (I_B) for the cases with $D = 0.4\mu m$, $0.6\mu m$, $0.8\mu m$ during the initial $30ps$ period.

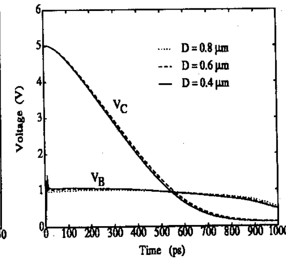


Fig. 6. The base and the collector voltages (V_B, V_C) during the overall $1ns$ period.

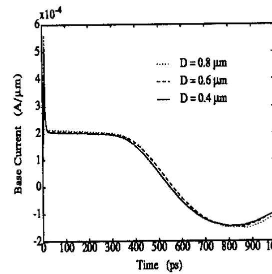


Fig. 7. The base currents (I_B) for the cases with $D = 0.4\mu m$, $0.6\mu m$, $0.8\mu m$ during the overall $1ns$ period.

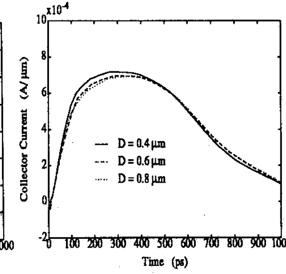


Fig. 8. The collector currents (I_C) for the cases with $D = 0.4\mu m$, $0.6\mu m$, $0.8\mu m$ during the overall $1ns$ period.

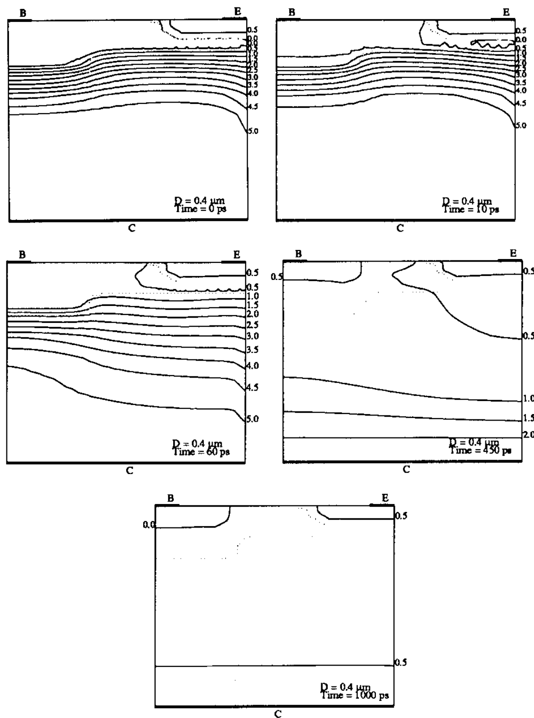


Fig. 9. 2D electrostatic potential(Ψ) contours in the bipolar device area for the cases with $D = 0.4\mu m$ at $0ps, 10ps, 60ps, 450ps, 1000ps$. The width of the cross section is $2\mu m$ and the depth is $1.8\mu m$. The metallurgical junctions are marked by the lightest lines.

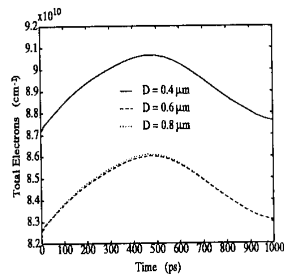


Fig. 10. Total electrons in cm^{-1} in the bipolar device area during transient.

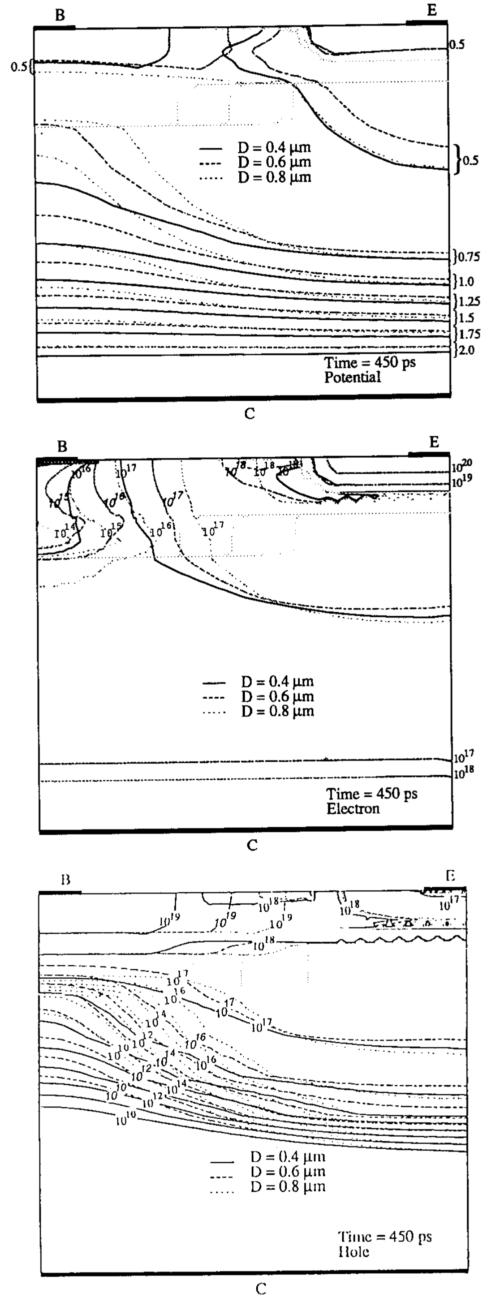


Fig. 11. 2D electrostatic potential(Ψ), electron (n) and hole (p) concentration contours for the cases with $D = 0.4\mu m$, $0.6\mu m$,$0.8\mu m$ at 450ps. The width of the cross section is $2\mu m$ and the depth is $1.8\mu m$. The metallurgical junctions are marked by the lightest lines.