Comparisons of zero-voltage-transition Cúk converters

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Abstract: With continuous input and output current, wide output voltage range and a small output filter, Cúk topology has received more and more attention in recent years. Soft switching is especially important to a Cúk converter, because the power handling capability requirements of semiconductor devices are higher than those of other topologies. Several kinds of newly proposed zero-voltage-transition (ZVT) topologies can be applied to Cúk converters to achieve soft switching. These ZVT topologies combine both the merits of conventional PWM converters and resonant converters. The power switches in the ZVT topologies commutate under zero-voltage-switching with the aid of resonant snubber cells during a short ZVT time. Circuit operations are identical to common PWM topologies during the rest time. Four classes of ZVT topologies for Cúk converters, with power MOSFETs employed as power switches, are discussed. Qualitative descriptions and experimental results are presented to illustrate each class of ZVT topology.

1 Introduction

Most DC/DC converters and power factor correctors use pulse-width-modulated (PWM) techniques as the control technique. The PWM technique prevails against other control techniques for its high-power capability and ease of control. Higher power density and faster transient response of PWM converters can be achieved by increasing the switching frequency. However, as the switching frequency increases, so do the switching losses and EMI noises. High switching losses reduce the power handling capability and serious EMI noises interfere with the control of PWM converters.

Cúk converters have been widely used as DC–DC converters and power factor correctors since first introduced in 1977 [1–3], they are less advantageous because of their continuous input and output current, ripple-free input current, small output filter and wide output voltage range. However, as shown in Fig. 1, the switch utilisation factor of the Cúk topology is much lower than those of the buck topology and the boost topology [4]. In other words, the power handling capability requirements of the semiconductor devices of a Cúk converter are much higher than those of a buck converter or a boost converter with the same output power. Reduction of switching losses and EMI noises are especially important to a Cúk converter.

To eliminate switching losses and EMI noises, a number of zero-voltage-transition (ZVT) topologies have been proposed in recent years [5–11]. These ZVT topologies use auxiliary switches and other passive components to form shunt resonant snubber cells. Switching losses and EMI noises are reduced, because the shunt resonant snubber cell helps the power switch to commutate under zero-voltage switching during a short ZVT transient time. The operation principles are identical to common PWM topologies during the rest time. Control strategies and design rules of PWM topologies can be directly applied to ZVT topologies. The advantages of both conventional PWM converters and resonant converters are maintained in ZVT converters. Several ZVT topologies can be applied to Cúk converters to reduce switching losses and EMI noises. Four classes of ZVT topologies for Cúk converters, with power MOSFETs employed as power switches, are discussed in this paper. Qualitative descriptions and experimental results are presented to illustrate each class of ZVT topology.

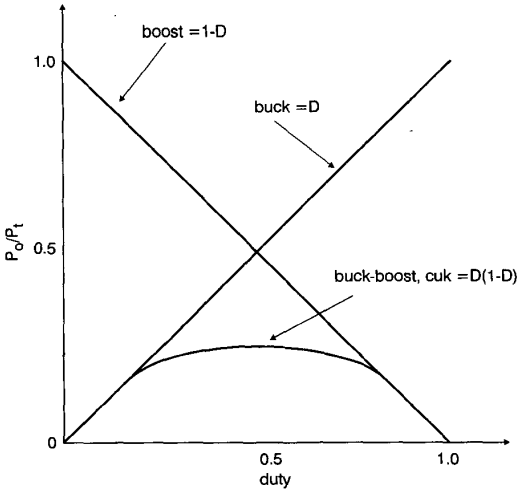

Fig. 1 *Switch utilisation factor in DC/DC converters*

2 The ZVT topologies for Cúk converters

To eliminate switching losses and EMI noises in Cúk converters when power MOSFETs are used as power switches, several kinds of ZVT topologies have been proposed in recent years. Among them, four classes of ZVT topologies are deemed suitable to be applied to Cúk converters. The circuit structures and qualitative characteristics of these

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four ZVT Cúk converters are presented. The voltage and current stresses of the main semiconductor devices in these four topologies are also shown in this Section.

2.1 Class A ZVT topology

The ZVT topology, first introduced in [5], can be applied to a Cúk converter, as shown in Fig. 2. It is called class A ZVT topology hereafter in this paper. It differs from a conventional PWM Cúk converter by possessing an additional resonant snubber cell consisting of a resonant inductor (L_r), a resonant capacitor (C_r), an auxiliary switch (S_2) and an auxiliary diode (D_2). The resonant capacitor C_r also incorporates the output capacitance of the power MOSFET. An additional diode in series with the resonant inductor or the auxiliary switch is required in practice. This diode can prevent the resonant inductor from resonating with the output capacitance of the auxiliary switch after the auxiliary diode is turned off. Based on the circuit analysis in [5], key waveforms of the class A ZVT topology are shown in Fig. 3.

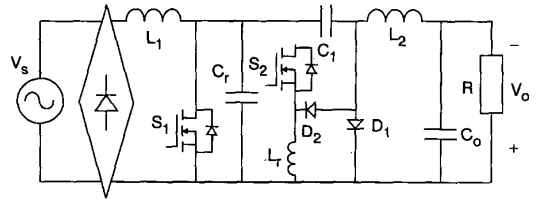

Fig. 2 *Circuit diagram of class A ZVT Cúk converter*

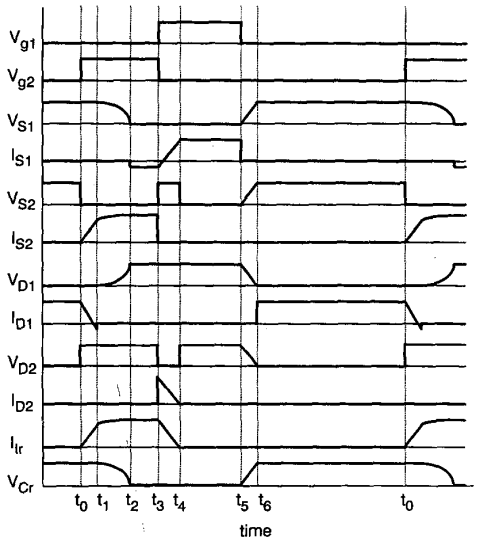

Fig. 3 *Key waveforms of class A ZVT Cúk converter*

The features of the class A ZVT topology are summarised as follows:

Advantages

- Minimum voltage and current stresses of switches and diodes: The voltage and current stresses of the main switch are identical to those in an ideal lossless Cúk converter. They are even smaller than those of a hard switching Cúk converter considering the voltage and current spikes during transients. The auxiliary switch has the same voltage stress as the main switch, while the current stress is less than that of the main switch because it only handles small amounts of resonant transition energy [8]. Voltage and current stresses of the main diode are the same as the main switch and those of the auxiliary diode are the same as the auxiliary switch. The active and passive switches in the class A ZVT topology are subjected to minimum voltage and current stresses.

Disadvantages

- Hard switching for the auxiliary switch and diode: The auxiliary switch and diode in the class A ZVT topology do not operate under soft switching. It can be seen from Fig. 3 that hard switching of these two semiconductor devices occurs when the auxiliary switch turns off at t_3. Not only the resulted switching losses, but also the dv/dt EMI noises significantly reduce the performance of the class A ZVT Cúk converter.
- Limited discharge of the resonant inductor: The main switch S_1 has to turn off after discharge of the resonant inductor L_r is accomplished. It lengthens the minimum duty cycle of the main switch. A long minimum duty cycle not only increases the minimum acceptable output voltage range but also makes the class A topology unsuitable to be employed under a wide range of applications.
- An additional saturable reactor required: In the class A ZVT topology, the main diode and the auxiliary diode are essentially in parallel. When the main diode is conducting, a certain percentage of current will flow through the auxiliary diode. This undesirable feature will cause considerable switching loss when the auxiliary switch turns on. An additional saturable reactor placed in series with the resonant inductor is required.

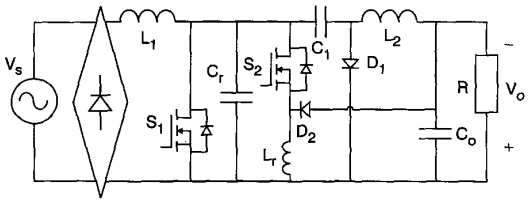

Fig. 4 *Circuit diagram of class B ZVT Cúk converter*

2.2 Class B ZVT topology

A modification of the class A ZVT topology proposed by the authors yields the class B ZVT topology, as shown in Fig. 4. The major difference between the class A and class B ZVT topologies is the discharge path of the resonant inductor. The anode of the auxiliary diode D_2 is connected to the output instead of the anode of the main diode D_1. Several distinct advantages are acquired, but no additional component is needed compared with the class A ZVT topology. The control ICs UC3855 and ML4822, designed for class A ZVT topology can be used in this topology as well. Circuit operations during one switching cycle can be divided into seven stages, which are shown in Figs. 5*a–g*.

Stage 1 (Fig. 5a; $t_0 < t < t_1$): The auxiliary switch S_2 turns on at t_0. The growth rate of the reverse recovery current of the diode D_1 is restricted by the resonant inductor L_r to achieve ZCS turn-on of the auxiliary switch S_2. Assuming that *trr* is the reverse recovery time of D_1, the peak value of the reverse recovery current, I_{rr}, can be given by

$$I_{rr} = I_{Lr}(t_1) - I_{L1} - I_{L2} \approx \frac{V_{C1} t_{rr}}{2L_r} \qquad (1)$$

Stage 2 (Fig. 5b; $t_1 < t < t_2$): The reverse recovery phenomenon finishes at t_1. As soon as D_1 is turned off, C_r starts to discharge to L_r through S_2. The growth rate of the voltage across D_1, which is equal to $V_{C1} - V_{Cr}$, is restricted by C_r to achieve ZVS turn-off of D_1. Assuming that the inductor currents I_{L1} and I_{L2} are both constant at this

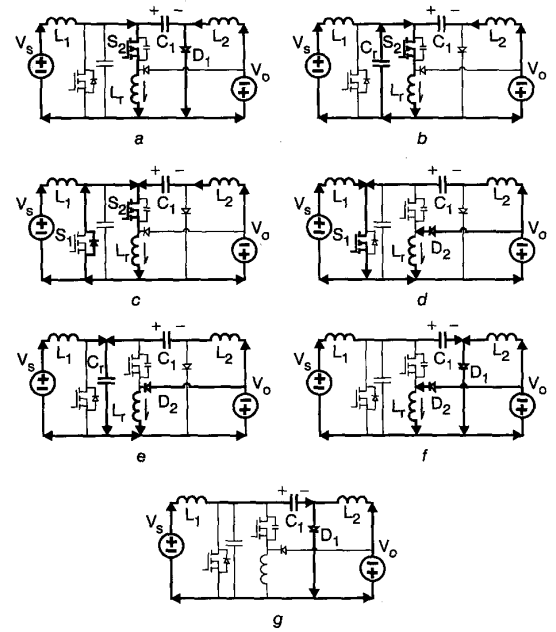

Fig. 5 *Equivalent circuits of class B ZVT Cúk converter during one switching cycle*
a Stage 1
b Stage 2
c Stage 3
d Stage 4
e Stage 5
f Stage 6
g Stage 7

stage, the resonant inductor current and resonant capacitor voltage are

$$I_{Lr}(t) = \frac{V_{C1}}{Z_1}\sin(\omega_1(t-t_1)) + I_{rr}\cos(\omega_1(t-t_1)) + I_{L1} + I_{L2} \quad (2)$$

$$V_{Cr}(t) = V_{C1}\cos(\omega_1(t-t_1)) - I_{rr}Z_1\sin(\omega_1(t-t_1)) \quad (3)$$

where

$$Z_1 = \sqrt{\frac{L_r}{C_r}} \quad (4)$$

$$\omega_1 = \frac{1}{\sqrt{L_r C_r}} \quad (5)$$

Stage 3 (Fig. 5c; $t_2 < t < t_3$): When V_{Cr} is discharged to zero at t_2, the body diode of the main switch, D_{S1B}, is turned on simultaneously. The drain-source voltage of S_1 remains zero after t_2. I_{Lr} retains its peak value at this stage and is given by

$$I_{Lr,p} = I_{L1} + I_{L2} + \sqrt{\frac{L_r I_{rr}^2 + C_r V_{C1}^2}{L_r}} \quad (6)$$

Stage 4 (Fig. 5d; $t_3 < t < t_4$): S_1 turns on and S_2 turns off at t_3. The resonant inductor L_r starts to discharge to the output through the auxiliary diode D_2. When S_1 turns on at t_3, since the main switch S_1 is not on the discharge path of L_r, the current through S_1 raises immediately to the normal turn-on current, which equals the sum of I_{L1} and I_{L2}.

Stage 5 (Fig. 5e; $t_4 < t < t_5$): S_1 turns off at t_4. After t_4, I_{L1} and I_{L2} start to charge the resonant capacitor C_r to achieve ZVS turn-off of S_1. Discharge of L_r can still be executed in this stage even if S_1 is off.

Stage 6 (Fig. 5f; $t_5 < t < t_6$): The main diode D_1 is turned on under ZVS when V_{Cr} is charged to V_{C1} at t_5. The resonant inductor L_r can keep discharging at this stage without influencing the state of S_1 and D_1.

Stage 7 (Fig. 5f; $t_6 < t < t_0$): The energy recovery process will be finished after I_{Lr} is discharged to zero at t_6. The auxiliary diode D_2 is also turned off under ZCS at the same time. After that, the circuit operation is identical to the turn-off state of a conventional PWM Cúk converter. It returns back to stage 1 when the auxiliary switch S_2 turns on again at t_0 in the next switching cycle.

Based on the analysis presented above, key waveforms of the class B ZVT topology are shown in Fig. 6.

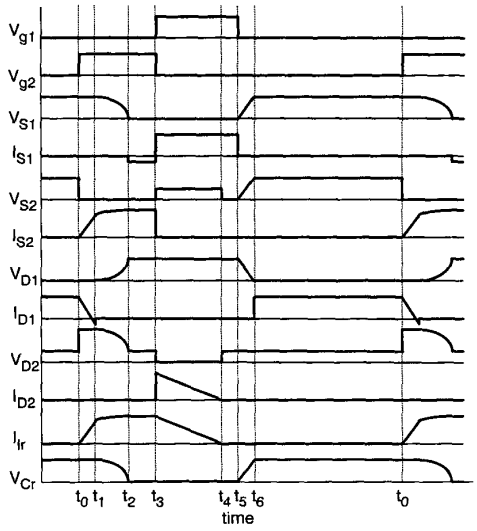

Fig. 6 *Key waveforms of the class B ZVT Cúk converter*

The features of the class B ZVT topology are summarised as follows:

Advantages

- Robust discharge of resonant inductor: Since the discharge current of the resonant inductor L_r does not flow through the main switch S_1, S_1 can turn off before L_r is completely discharged. The minimum duty cycle of the main switch is shorter than for other ZVT topologies. This desirable feature makes the class B ZVT topology especially suitable to be employed for PFC applications, for example. Since the duty cycle of the main switch determines the output voltage range for linear operation, the output voltage range of the class B ZVT topology is also the widest. The saturable reactor in the class A ZVT topology is no longer necessary in the class B ZVT topology due to robust discharge of L_r.
- Minimum ZVT time: Unlike other ZVT topologies, discharge time of the resonant inductor is not involved in ZVT time in the class B ZVT topology. The main switch handles all the current from L_1 and L_2 immediately after ultrashort ZVT time. The voltage and current waveforms of the switches in the class B ZVT topology are essentially square-waves, except during ultrashort ZVT time. Control and design techniques of PWM converters can be best applied to the class B ZVT topology. Compared with class A ZVT topology, a larger L_r can also be used to reduce reverse recovery loss of D_1 with the same ZVT time. It decreases not only the turn-on loss but also the current stress of S_2.

Disadvantages

- Hard switching for the auxiliary switch and diode: As in the class A ZVT topology, the auxiliary switch and diode

in the class B ZVT topology do not operate under soft switching.

• Increased voltage stresses of the auxiliary switch and diode: Compared with the class A ZVT topology, the voltage stresses of both the auxiliary switch S_2 and the auxiliary diode D_2 increase from $V_s + V_0$ to $V_s + 2V_0$. Since the high voltage stresses appear for only a short time period with the current stresses unchanged, semiconductor devices with only slightly larger voltage ratings are sufficient.

2.3 Class C ZVT topology

The ZVT topology, first introduced to be applied to a boost converter [6], can also be applied to a Cúk converter, as shown in Fig. 7. It is called a class C ZVT topology hereafter in this paper. It differs from a conventional PWM Cúk converter by possessing an additional resonant snubber cell, consisting of two resonant capacitors (C_{r1} and C_{r2}), a resonant inductor (L_r) and an auxiliary switch (S_2). The resonant capacitor C_{r1} incorporates the output capacitance of the main power MOSFET. Body diodes of the main switch and the auxiliary switch are also utilised. Based on the circuit analysis in [6], key waveforms of the class C ZVT topology are shown in Fig. 8.

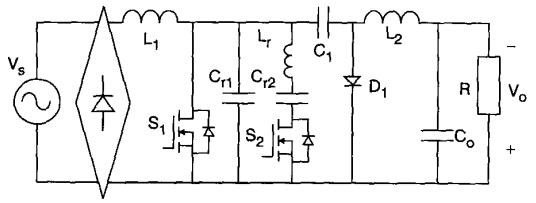

Fig. 7 *Circuit diagram of class C ZVT Cúk converter*

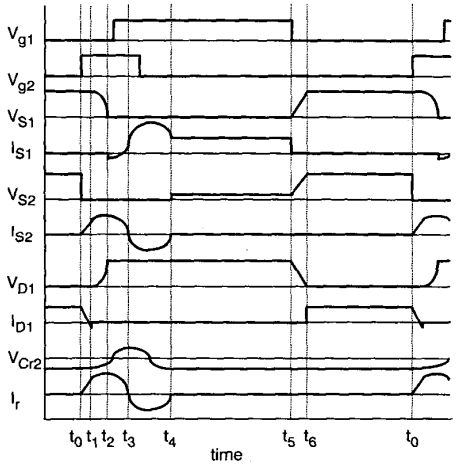

Fig. 8 *Key waveforms of class C ZVT Cúk converter*

The features of the class C ZVT topology are summarised as follows:

Advantages

• Soft switching for all semiconductor devices: The major disadvantage of the class A and class B ZVT topologies is that the auxiliary switches and diodes operate under hard switching. In the class C ZVT topology, the auxiliary switch turns off after its body diode is conducting to achieve ZCS turn-off. All semiconductor devices are commutated under soft switching.

• No need to isolate the drive circuit: Unlike the other three topologies, the drive circuit of the class C ZVT topology requires no isolation. Since the synchronisation problem between the control signals of the main switch and the auxiliary switch is very important in ZVT topologies, reliability is much improved without the requirement of an isolated drive circuit, and circuit cost is also reduced.

Disadvantages

• Energy accumulated in resonant snubber cell: It can be seen from Fig. 8, that the energy in the resonant snubber cell keeps constant from t_2 to t_0, because either the voltage across or the current through the snubber cell is ideally zero. However, from t_0 to t_2, the energy increases because both the voltage and the current are positive. It is clear that the energy in the resonant snubber cell accumulates during $t_0 - t_2$ every switching cycle. Since the snubber energy is stored in C_{r2}, power dissipative components are required to prevent unacceptable high voltage across C_{r2}. This undesirable feature reduces not only efficiency but also practicability.

• Turn-on current spike of the main switch: The penalty for applying soft switching to all semiconductor devices is the turn-on current spike of the main switch S_1. It increases conduction losses and sometimes increases the current stress of S_1, as the current spike is approximately twice that of the inductor current during turn-on. The increased current stress of S_1 can be reduced to only 33.3% of the average current with properly selected inductor values of L_1 and L_2. It is much less than that in the discontinuous conduction mode where the current stress of S_1 is over 200% of the average current. However, the increased conduction losses indeed reduce the efficiency, and the increased current stress of S_1 raises the circuit cost.

• Increased voltage stress of the auxiliary switch: The voltage stress of the auxiliary switch S_2 is increased by V_{Cr2}. Since V_{Cr2} varies over a wide range, the voltage stress of S_2 is increased, to at most, two times that of S_1, which not only increases circuit costs but also decreases stability.

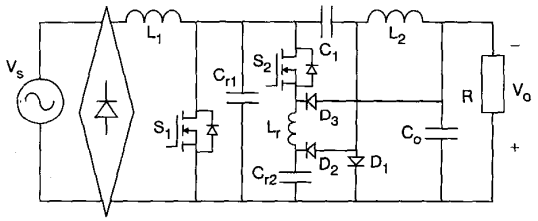

Fig. 9 *Circuit diagram of class D ZVT Cúk converter*

2.4 Class D ZVT topology

The class D ZVT Cúk converter is shown in Fig. 9. It is the modified version of the ZVT topology proposed by the authors in [9], which can be seen as the amelioration of the class C ZVT topology. An auxiliary diode D_2 is added to the discharge resonant capacitor C_{r2}. The energy in the resonant snubber cell is reset to zero every switching cycle by adding D_2. The increased voltage stress of the auxiliary switch is also prevented in the class D ZVT topology. Diode D_3 is added to clamp the voltage across S_2 to the output voltage when S_2 is off. It prevents a high voltage spike of S_2, due to resonant ringing, when the body diode of S_2 is turned off at t_4. This diode can sometimes be removed since the voltage spike of S_2 is generally small. As in the class C ZVT topology, all semiconductor devices in the class D ZVT topology, including D_2 and D_3, also operate under soft switching. Based on the circuit analysis in [9], key waveforms of the class D ZVT topology are shown in Fig. 10.

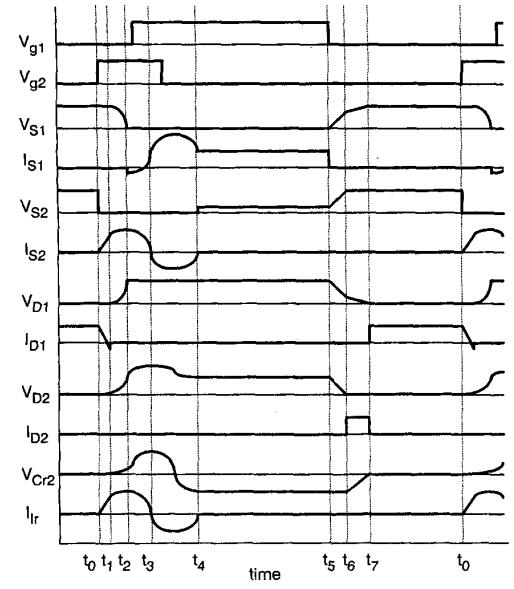

Fig. 10 *Key waveforms of class D ZVT Cúk converter*

The features of the class D ZVT topology are summarised as follows:

Advantages

- Soft switching for all semiconductor devices: As in the class C ZVT topology, all semiconductor devices in the class D ZVT topology also operate under soft switching. Switching losses and EMI noises are reduced to a minimum.

- Energy in the resonant snubber cell reset every switching cycle: It is shown in Fig. 10 that the current through L_r (I_{Lr}) and the voltage across C_r (V_{Cr}) are reset to zero before S_1 turns on in every switching cycle. Although the energy temporarily stored in L_r and C_r still varies during different switching cycles, it is reset to zero every time before S_1 tums on. No energy can be accumulated in the resonant snubber cell. The problem of the class C ZVT topology is resolved by adding an auxiliary diode D_2. The increased voltage stress of the auxiliary switch of the class C ZVT topology is also prevented. This desirable feature guarantees that the class D ZVT topology is eligible to be employed under long-term operation.

Disadvantages

- Turn-on current spike of the main switch: As described in the class C ZVT topology, the penalty for applying soft switching to all semiconductor devices in the class D ZVT topology is the turn-on current spike of the main switch S_1.

- Increased voltage stress of the auxiliary diode: Although the voltage stress of the auxiliary switch S_2 is not increased as in the class C ZVT topology, the voltage stress of the auxiliary diode D_2 is increased by V_{Cr2}. Since V_{Cr2} in the class D ZVT topology is limited to a comparatively small value, the voltage stress of D_2 does not increase too much, besides, the increased voltage stress of D_2 appears for only a short period of time. A power diode with a slightly larger voltage rating is sufficient.

2.5 Voltage and current stresses of four ZVT topologies

To further compare the four ZVT topologies presented above, the voltage and current stresses of the power devices are shown in Table 1. In Table 1, $I_L = I_{L1} + I_{L2}$, $V_C = VS + V_O$, $I_{Dis} = (C_r/L_r)^{0.5} V_C$ = discharge current of C_r.

3 Experimental results

In order to provide an experimental comparison of the topologies described in this paper, prototypes of four 400W, 200V DC output, 50kHz ZVT Cúk converters have been built in the laboratory to verify the analysis presented. The component specifications of these four circuits are listed in Table 2. A hard switching Cúk converter with the same specifications is also built. The efficiency, at 400W loading, of the class A, B, C and D ZVT topologies and the hard switching counterpart are 95.0%, 95.2%, 94.3%, 94.7% and 88.7%, respectively.

Table 2: Part lists of four ZVT Cúk converter prototypes

	Class A	Class B	Class C	Class D
L_1	800μH	800μH	800μH	800μH
L_2	800μH	800μH	800μH	800μH
C_1	4.7μF	4.7μF	4.7μF	4.7μF
C_O	660μF	660μF	660μF	660μF
S_1	2SK2198	2SK2198	2SK2198	2SK2198
D_1	HFA15TB60	HFA15TB60	HFA15TB60	HFA15TB60
S_2	2SK2198	2SK2198	2SK2198	2SK2198
D_2	HFA15TB60	HFA15TB60	N/A	HFA15TB60
L_r	15μH	60μH	12μH	12μH
$C_r(C_{r1})$	3.3nF	3.3nF	3.3nF	3.3nF
C_{r2}	N/A	N/A	22nF	22nF

Key oscillograms of the class A, B, C and D ZVT topologies are shown in Figs. 11–22, respectively. Switch commutation oscillograms of the hard switching converter are also shown in Fig. 23. It is clearly seen from the oscillograms of V_{S1} and I_{S1} that the main switch in each topology operates under ZVS. The major difference of the commutation waveforms of the main switches is that the I_{S1}s of the class C and class D ZVT topologies have turn-on current spikes. The current spikes increase conduction losses and current stresses of the main switches. Although no current spikes appear on I_{S1} in the class A and class B ZVT topologies, the auxiliary switches operate under hard switching,

Table 1: Voltage and current stresses of power devices in four ZVT Cúk converters

	S_1		S_2		D_1		D_2	
	V stress	I stress	V stress	I stress	V stress	I stress	V stress	I stress
A	V_C	I_L	V_C	$I_L + I_{Dis}$	V_C	I_L	V_C	$I_L + I_{Dis}$
B	V_C	I_L	V_C	$I_L + I_{Dis}$	V_C	I_L	$V_C + V_O$	$I_L + I_{Dis}$
C	V_C	$2I_L + I_{Dis}$	V_C	$I_L + I_{Dis}$	V_C	I_L	N/A	N/A
D	V_C	$2I_L + I_{Dis}$	V_C	$I_L + I_{Dis}$	V_C	I_L	$V_C + V_{Cr2}$	I_L

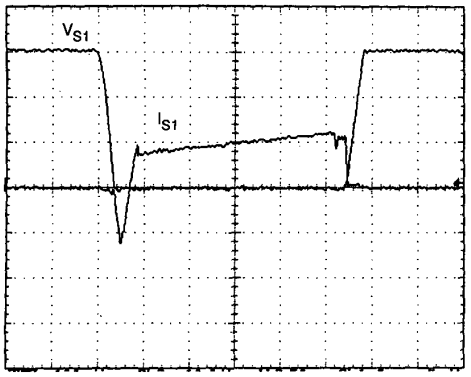

Fig. 11 *Key oscillograms of class A ZVT Cúk converter: V_{S1} and I_{S1}*
100V/div; 4A/div; 2μs/div

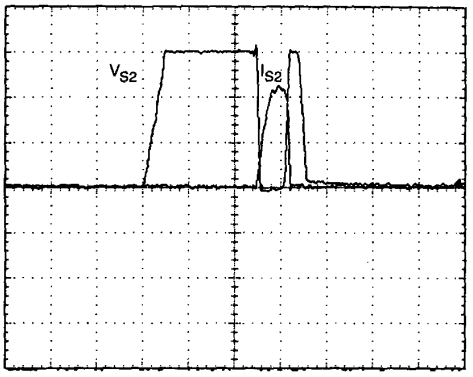

Fig. 12 *Key oscillograms of class A ZVT Cúk converter: V_{S2} and I_{S2}*
100V/div; 4A/div; 2μs/div

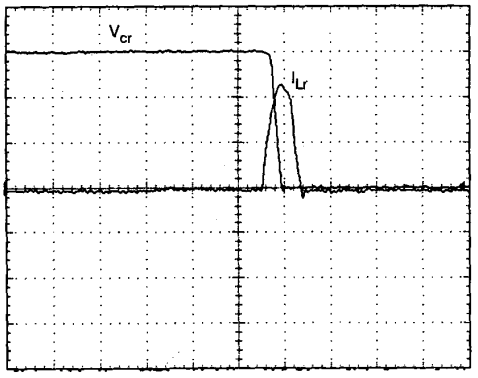

Fig. 13 *Key oscillograms of class A ZVT Cúk converter: V_{Cr} and I_{Lr}*
100V/div; 4A/div; 2μs/div

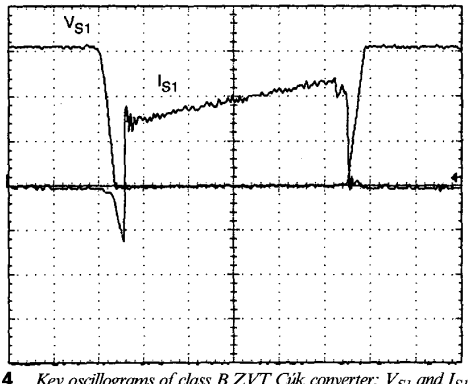

Fig. 14 *Key oscillograms of class B ZVT Cúk converter: V_{S1} and I_{S1}*
100V/div; 4A/div; 2μs/div

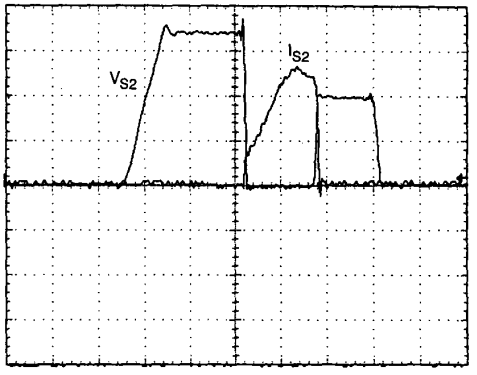

Fig. 15 *Key oscillograms of class B ZVT Cúk converter: V_{S2} and I_{S2}*
100V/div; 4A/div; 2μs/div

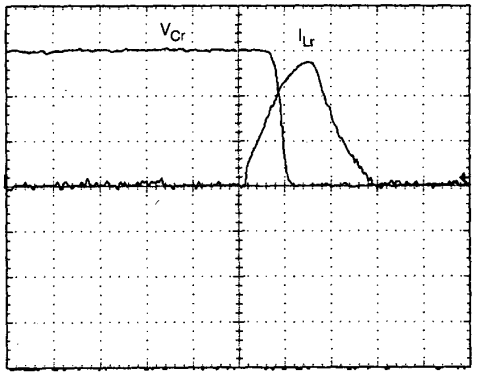

Fig. 16 *Key oscillograms of class B ZVT Cúk converter: V_{Cr} and I_{Lr}*
100V/div; 4A/div; 2μs/div

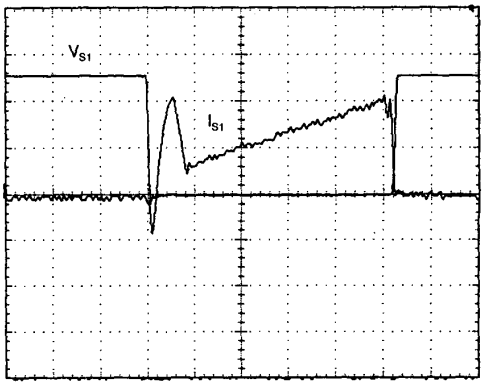

Fig. 17 *Key oscillograms of class C ZVT Cúk converter: V_{S1} and I_{S1}*
100V/div; 4A/div; 2μs/div

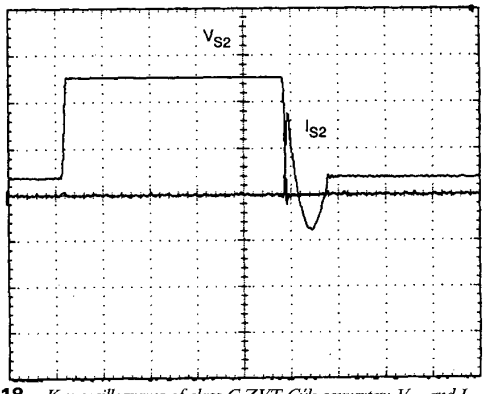

Fig. 18 *Key oscillograms of class C ZVT Cúk converter: V_{S2} and I_{S2}*
100V/div; 4A/div; 2μs/div

increasing switching losses and EMI noise. A choice has to be made between the increased switching losses and EMI noise caused by the hard switching of S_2 (topologies A and B) and the increased conduction losses and current stresses caused by the turn-on current spikes of S_1 (topologies C and D).

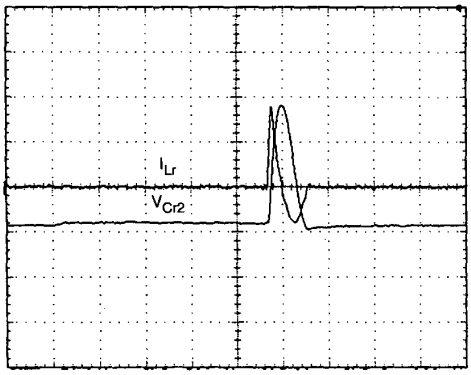

Fig. 19 *Key oscillograms of class C ZVT Cúk converter: V_{Cr2} and I_{Lr}*
50V/div; 4A/div; 2μs/div

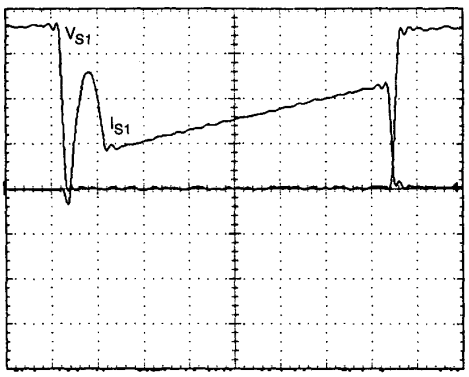

Fig. 20 *Key oscillograms of class D ZVT Cúk converter: V_{S1} and I_{S1}*
100V/div; 4A/div; 2μs/div

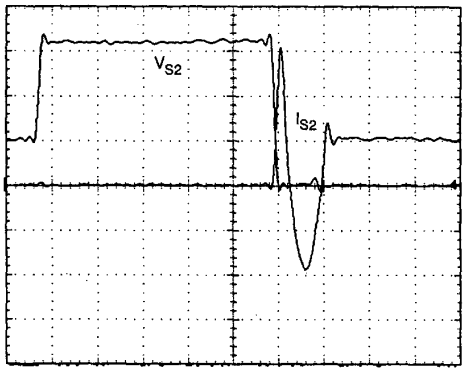

Fig. 21 *Key oscillograms of class D ZVT Cúk converter: V_{S2} and I_{S2}*
100V/div; 4A/div; 2μs/div

Comparing the waveforms shown in Figs. 11–16, it can be seen that the waveforms of the class A and class B ZVT topologies are quite similar. However, since the class B ZVT topology has a more robust discharge of the resonant inductor and a shorter ZVT time, it is recommended compared with the class A ZVT topology. Comparing the waveforms shown in Figs. 17–22, it can also be seen that the waveforms of the class C and class D ZVT topologies are quite similar. Although the class C ZVT topology is easily implemented, because the drive circuit requires no isolation, it has a serious problem in that the energy is accumulated in the resonant snubber cell. This problem is solved in the class D ZVT topology by simply adding an auxiliary diode. An optional diode D_3 can also be added to prevent the voltage spike across S_2 caused by resonant ringing. The class D ZVT topology is recommended compared with the class C ZVT topology.

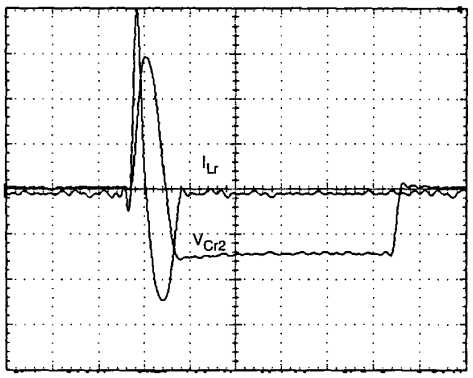

Fig. 22 *Key oscillograms of class D ZVT Cúk converter: V_{Cr2} and I_{Lr}*
50V/div; 4A/div; 2μs/div

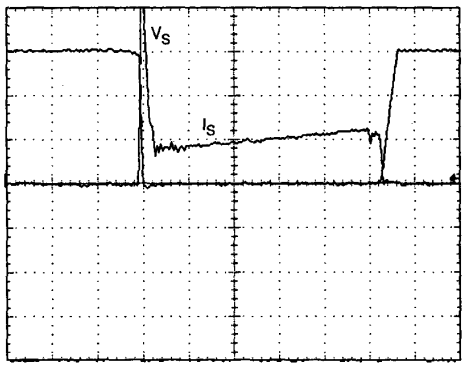

Fig. 23 *Commutation oscillograms of the hard switching Cúk converter*
100V/div; 4A/div; 2μs/div

4 Conclusion

Four classes of newly proposed ZVT topologies for Cúk converters have been presented in this paper. Comparison of these four ZVT topologies is accomplished through qualitative descriptions and experimental waveforms. The characteristics of each ZVT topology are summarised in Table 3. The major disadvantage of the class A and class B topologies is the hard switching of the auxiliary switch and diode. It increases switching losses and EMI noises. In contrast, soft switching is applied to all semiconductor devices, including auxiliary switches and diodes, in the class C and class D topologies. However, the penalty is the turn-on current spike of the main switch, which becomes the major disadvantage of the class C and class D topologies, increasing conduction losses and current stress of the main switch. A choice must be made between the increased switching losses and EMI noise caused by hard switching of S_2 (topologies A and B) and the increased conduction losses and current stresses caused by turn-on current spikes of S_1 (topologies C and D). Since the discharge path of the resonant converter is modified in the class B ZVT topology, a shorter ZVT time and more robust discharge of the resonant inductor make the class B ZVT topology superior to the class A ZVT topology. Since the class D ZVT topology

prevents the energy from being accumulated in the snubber cell by adding an auxiliary diode, the class D ZVT topology is deemed superior to the class C ZVT topology.

Table 3: Comparison of four ZVT Cúk converters

	Class A	Class B	Class C	Class D
Snubber components	4	4	4	5
ZVT time	mid	short	long	long
Hard switching devices	S_2, D_2	S_2, D_2	none	none
Increased stresses	none	V_{S2}, V_{D2}	I_{S1}, V_{S1}	I_{S1}, V_{D2}
Snubber energy accumulated	no	no	yes	no
Isolated drive circuit required	yes	yes	no	yes
Saturable reactor required	yes	no	no	no
Specified control IC	yes	yes	no	no
L_r discharge limited by S_1	yes	no	yes	yes

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