Locally Matching Design for Flip-Chip Transition

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This paper presents a locally matching design for a single flip chip transition. By a suitable layout deform along the lateral direction, the design is aimed to compensate the parasitic effect of the transition and achieve a good match over a wide frequency band. Simulation results by FDTD are represented to validate the design idea.

1 Introduction

Detailed simulation has shown that the flip-chip can yield better performance and lower surface wave loss. However, the traditional flip chip design suffers from high return loss as frequency goes higher. Analysis to the single chip transition has depicted that the reflection can be reduced by increasing the width of via or reducing its length, and by eliminating the conductor on the motherboard below the chip [1]. Some efforts were made to investigate the influences on the transition characteristics due to the positions or cross sections of vias, and the shape of the metal [2],[3]. Another transition design employed dual flip-chip connection to achieve resonance and control the occurrence of the minimum reflection in the desire frequency band [4].

To elaborate furthermore in the design, the equivalent circuits of the flip-chip for the millimeter-wave circuit design was also established [5],[6]. In most practical cases, the transition is found to be capacitive. In view of this capacitive nature, a set of high impedance line has been inserted in the transmission line to compensate the capacitance [7]. This design, as the aforementioned methods, accomplishes the layout design in the longitudinal direction of propagation. To minimize the transition area, this paper proposes a locally matching design, which can produce a wide band transition but involves a small area in the transverse direction.

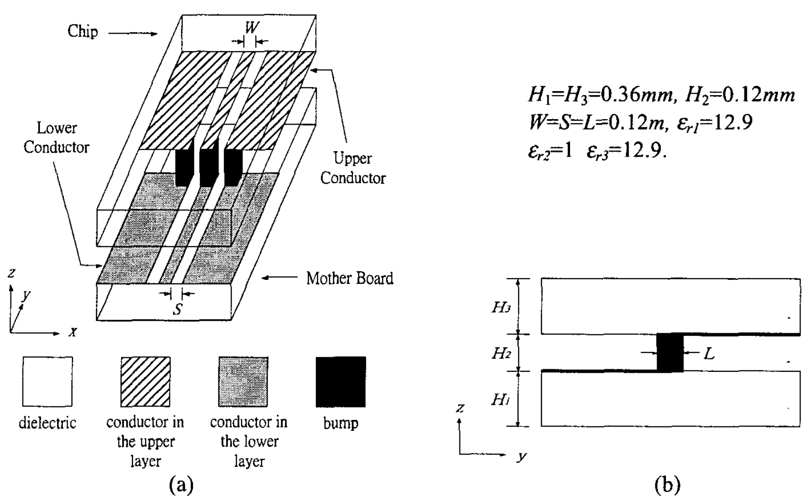

Fig.1 The configuration of conventional flip-chip transition. (a) three-dimensional view and (b) side view.

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2 Conventional Design

Circuit performance of flip-chip transitions has been investigated in the literature [5]. A typical configuration shown in Fig.1 has geometry parameters $H_1=H_3=0.36mm$, $H_2=0.12mm$, $W=S=L=0.12mm$, $\varepsilon_{r1}=\varepsilon_{r3}=12.9$, $\varepsilon_{r2}=1$. The substrates and conductors under analysis are assumed to be infinite and lossless. To investigate scattering characteristics of the flip-chip transition, we use the in-house developed FDTD combined with PML absorbing boundary conditions. Fig.2(a) shows the calculated return loss (RL) versus frequency. The calculated results with solid lines are in excellent agreement with those reprinted from [5, fig.12]. As shown in the figure, it can be seen that the RL becomes larger as the frequency increases.

To look into more details, Fig.2(b) shows the frequency response of S_{11} on the Smith chart. It can be seen from this chart that this transition moves nearly on a constant conductance ($^1/_{50\,\Omega}$) circle as frequency sweeps from 0GHz to 50 GHz. This depicts that the transmission line can be treated as in a shunt connection with capacitance. As frequency goes higher, the capacitive effect is more significant to degrade the return loss [see Fig.2(a)].

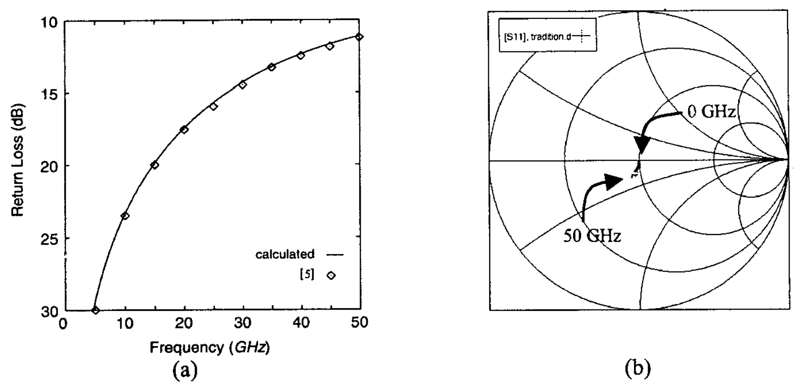


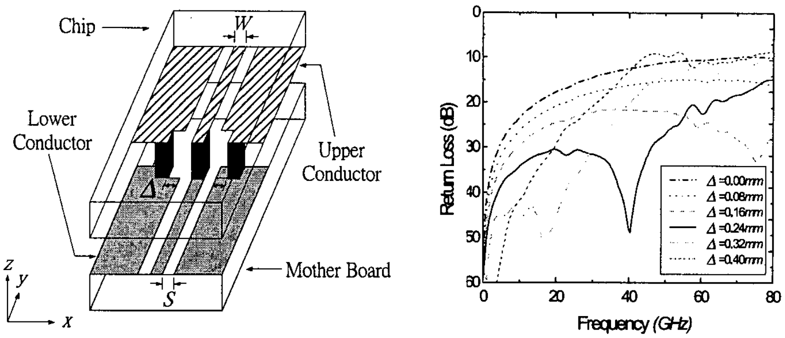
Fig.2 Transition of the conventional flip-chip design. (a) return loss versus frequency (b) reflection coefficients on the Smith chart

3 Locally Matching Design

It is straightforward to design a transition along the transmission line for the impedance matching. However, it may become too costly if the transition occupies too much area. When the frequencies goes higher such that the transition size is larger than one-tenth of the guided wavelength, the parasitic effect may be severe and the transition response may be worse. Based on the above reasoning, the area of transition should be as small as possible.

In view of the capacitive nature of the transition, one can either increases the inductance or reduces the capacitance of the transition. For the first way, the bump height was increased to enhance the inductance and the return loss is good over a wide frequency band [5, p.2547]. However, the bump height may not be increased as desired in general fabrication process. For the second way, a locally matching technique is proposed here to reduce the local capacitance of the transition. The whole view of the structure is shown in Fig.4(a) and the parameters are the same as Fig1. The ground conductors both on the mother board and chip are retreated by a lateral shift of Δ near the transition area, and so is the ground vias connection accordingly. Choosing suitable Δ, the capacitance of the flip-chip transition can be reduced accordingly.

Fig.4(b) shows the return loss versus frequency with different values of Δ as a parameter. From this figure, we can see that the return loss is larger than 30dB from DC up to 45GHz with $\Delta=0.24mm$ and larger than 20dB from DC up to 80GHz with $\Delta=0.16mm$. With properly chosen Δ, the impedance can be matched to achieve good transition over a wide frequency band. Another benefit is that this structure only occupies small area in the transverse direction, not occupying any area in the longitudinal direction. A back to back test structure to verify the present idea is under fabrication process. The simulation and measured results will be presented at the conference.



(a) (b)

Fig.3 The locally matching design. (a) whole view and (b) frequency response of return loss.

4 Summary

A new flip-chip design based on the idea of locally matching was proposed and simulated by the FDTD method. This structure is not restricted by the allowable ratio of bump cross section and height in the fabrication process and saves areas in the longitudinal direction of propagation. By suitably choosing the lateral shift Δ, the impedance can be matched to achieve a good transition over a wide bandwidth.

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