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考慮邊際電場效應之次九十奈米互補金氧半超大型積電精簡元件模型(2/3)
期中進度報告(精簡版)

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Analysis of the Gate–Source/Drain Capacitance Behavior of a Narrow-Channel FD SOI NMOS Device Considering the 3-D Fringing Capacitances Using 3-D Simulation

Chien-Chung Chen, James B. Kuo, *Fellow, IEEE*, Ke-Wei Su, and Sally Liu

***Abstract*—This paper reports an analysis of the gate–source/drain capacitance behavior of a narrow-channel fully depleted (FD) silicon-on-insulator (SOI) NMOS device considering the three-dimensional (3-D) fringing capacitances. Based on the 3-D simulation results, when the width of the FD SOI NMOS device is scaled down to 0.05 μm, the inner-sidewall-oxide fringing capacitance ($C_{\rm FIS}$), due to the fringing electric field at the edge of the mesa-isolated structure of the FD SOI NMOS device biased at $V_G = 0.3$ V and $V_D = 1$ V, is the second largest contributor to the gate–source capacitance ($C_{\rm GS}$). Thus, when using nanometer CMOS devices with a channel width smaller than 0.1 μm, $C_{\rm FIS}$ cannot be overlooked for modeling gate–source/drain capacitance ($C_{\rm GS}/C_{\rm GD}$).**

***Index Terms*—Capacitance, CMOSFETs, modeling, silicon-on-insulator (SOI) technology, simulation.**

I. Introduction

SILICON-ON-INSULATOR (SOI) technology has been regarded as a major technology for integrating CMOS VLSI in the nanometer regime [1]. For small-geometry sub-100-nm SOI CMOS devices, narrow-channel effects are important in determining the performance [2], [3]. For analyzing the narrow-channel effects of a nanometer small-geometry device, three-dimensional (3-D) analysis is necessary, which is difficult to carry out. Compact modeling of the narrow-channel effects of the small-geometry fully depleted (FD) SOI CMOS devices in terms of the threshold voltage and the current conduction derived from 3-D analysis has been reported [4]–[6]. 3-D analysis of the source/drain capacitance of the small-geometry SOI CMOS devices has been done [7]. However, the gate–source/drain capacitance ($C_{\rm GS}/C_{\rm GD}$) behavior of a narrow-channel FD SOI NMOS device considering the 3-D fringing electric-field effects has not been reported. In fact, the 3-D fringing electric effects may bring impacts on the capacitance behavior substantially. In addition to the fringing electric field near the inner sidewall of the mesa-isolation structure in a narrow-channel FD SOI NMOS device, the fringing electric field in the source/drain sidewall is also important for affecting the device performance. In this paper, the $C_{\rm GS}/C_{\rm GD}$ behavior of a narrow-channel FD SOI NMOS device considering 3-D fringing electric-field effects is described. It will be shown that when the width of the FD SOI NMOS device is scaled down to below 0.1 μm, its gate–source/drain capacitance is substantially affected by the 3-D fringing electric-field-induced effects near the inner oxide sidewall and the source/drain sidewall. In the following sections, the capacitance behavior is described first, which is followed by discussion and conclusion.

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II. Capacitance Behavior

Fig. 1 shows the 3-D cross section of the FD SOI NMOS device under study. It has a gate oxide of 5 nm, a thin film of 15 nm doped with a p-type doping density of 5×10^{17} cm^{-3}, a channel length of 0.18 μm, and a buried oxide of 400 nm. A mesa-isolation structure with the n^+ gate polysilicon covering a width-direction inner-sidewall oxide of 8 nm in thickness has been used. In order to facilitate analysis, next to the polysilicon gate, it is filled with oxide. A total of 17 640 grids have been generated for this device using a 3-D device simulator—Davinci [8]. Each set of the simulation for the $C_{\rm GS}/C_{\rm GD}$ of the device took about 190-min CPU time based on a 900MIPs workstation.

Fig. 2 shows the two-dimensional (2-D) electric-field contours in the $x-y$ and $y-z$ cross sections of the FD SOI NMOS device with a channel width of 0.1 μm biased at the drain voltage of $V_D = 1$ V and the gate voltage of $V_G = 1$ V. As shown in the $x-y$ cross section along the channel length direction (x-direction), the fringing electric field in the source and drain sidewalls is not negligible, which may affect $C_{\rm GS}/C_{\rm GD}$ substantially. In addition, in the $y-z$ cross section in the channel-width direction (z-direction) in the inner-sidewall oxide at the edge of the mesa-isolated structure, the fringing electric field is also not negligible, which may also affect $C_{\rm GS}/C_{\rm GD}$ to some extent. In the following analysis, an analysis in terms of the contributions from the fringing electric fields in the inner oxide sidewall and the source/drain sidewall to the

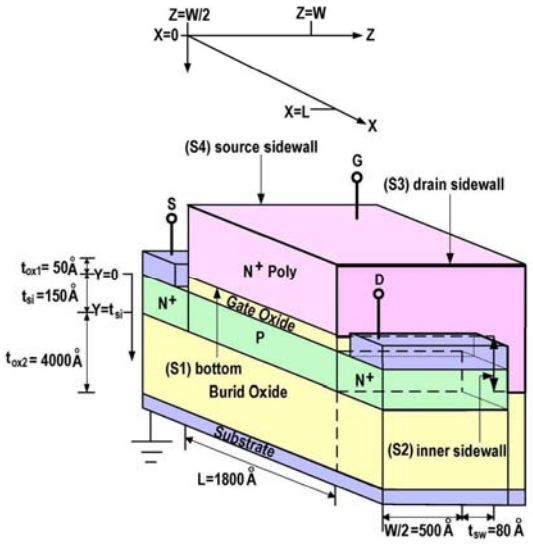

Fig. 1. Three-dimensional cross section of the mesa-isolated FD SOI NMOS device under study.

gate–source/drain capacitance of the narrow-channel FD SOI NMOS device is described.

As the $C_{\rm GS}/C_{\rm GD}$ is defined as the derivative of the gate charge with respect to the source/drain voltage $C_{\rm GS} = dQ_G/dV_S$, $C_{\rm GD} = dQ_G/dV_D$ [8], [9], where Q_G is the total gate charge. From Gauss' Law, the gate charge Q_G could be obtained by the surface integral of the displacement over the four surfaces of the poly gate—$(S1)$ is the bottom surface of the poly gate above the gate oxide, $(S2)$ is the inner surface next to the oxide sidewall, $(S3)$ is the right surface next to the drain sidewall, and $(S4)$ is the left surface next to the source sidewall as shown in Fig. 1. Thus, one obtains

$$Q_G = \iint_{S1} \epsilon_{\rm ox} E_y dx\, dz + \iint_{S2} \epsilon_{\rm ox} E_z dx\, dy + \iint_{S3} \epsilon_{\rm ox} E_x dy\, dz + \iint_{S4} \epsilon_{\rm ox} E_x dy\, dz \quad (1)$$

where x is in the lateral channel direction, y is in the substrate direction, and z is in the channel width direction. $\epsilon_{\rm ox}$ is the oxide permittivity. E_y is the y-direction electric field at the bottom surface of the poly gate in the gate oxide $(S1)$. E_x is the x-direction electric field at right (drain) and the source (left) edge of the poly gate in the oxide side $(S3/S4)$. E_z is the z-direction electric field at the inner surface of the poly gate next to the oxide sidewall $(S2)$. From the above equation, the total gate charge Q_G can be expressed as the combination of the intrinsic gate charge (Q_I) in $S1$, the bottom of the poly gate, the inner-sidewall fringing gate charge $(Q_{\rm FIS})$ in $S2$, the inner surface of the poly gate next to the oxide back sidewall, the drain-sidewall fringing gate charge $(Q_{\rm FDS})$ in $S3$ and the source sidewall fringing gate charge $(Q_{\rm FSS})$ in $S4$. Therefore, one obtains

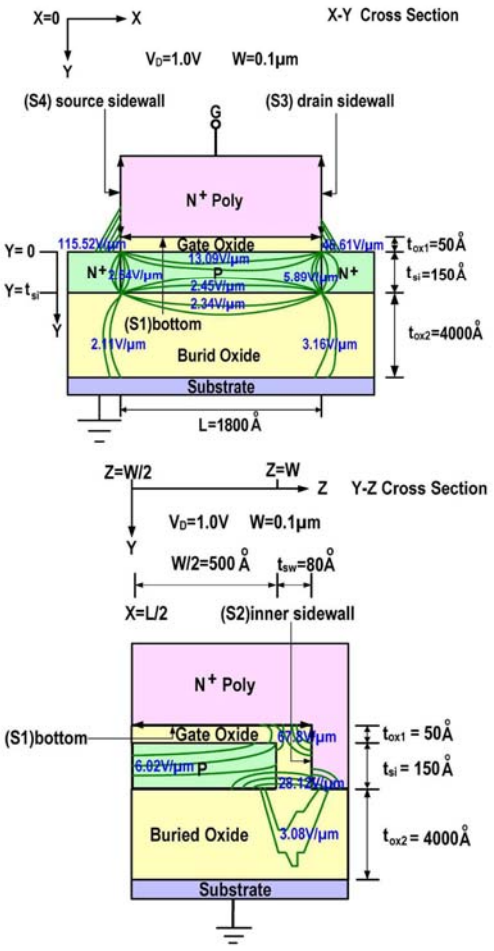

Fig. 2. 2-D electric-field contours in the $x-y$ and $y-z$ cross sections of the FD SOI NMOS device with a channel width of 0.1 μm, biased at $V_G = 1$ V and $V_D = 1$ V.

$$C_{\rm GS} = C_I + C_{\rm FIS} + C_{\rm FDS} + C_{\rm FSS} \quad (2)$$

where the intrinsic gate capacitance in $S1$ is defined as the derivative of the intrinsic gate charge with respect to the source voltage: $C_I = dQ_I/dV_S$. The inner oxide sidewall fringing capacitance in $S2$ is defined as: $C_{\rm FIS} = dQ_{\rm FIS}/dV_S$. The drain-sidewall fringing capacitance in $S3$ is defined as $C_{\rm FDS} = dQ_{\rm FDS}/dV_S$. The source sidewall fringing capacitance in $S4$ is defined as $C_{\rm FSS} = dQ_{\rm FSS}/dV_S$. By the same token, the gate-drain capacitance could be defined in a similar way as

$$C_{\rm GD} = C'_I + C'_{\rm FIS} + C'_{\rm FDS} + C'_{\rm FSS} \quad (3)$$

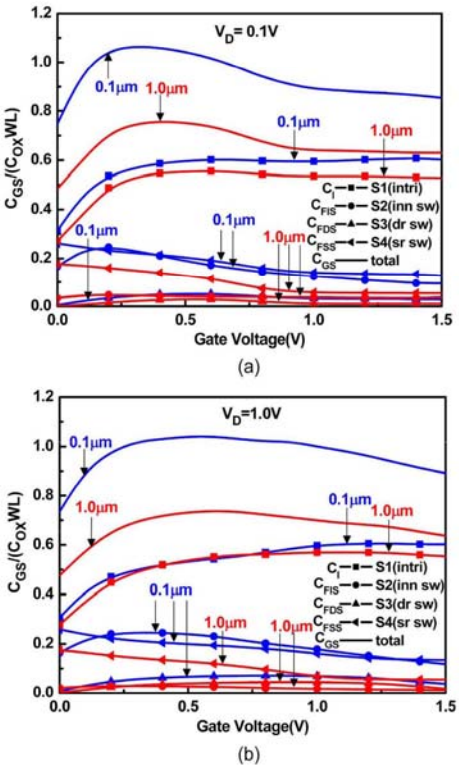

Fig. 3. Gate–source capacitance ($C_{\rm GS}$) versus the gate voltage (V_G) of the mesa-isolated FD SOI NMOS device with channel widths of 0.1 and 1 μm, biased at V_D of (a) 0.1 V and (b) 1 V, considering the contributions from $S1$—the intrinsic gate capacitance (C_I), $S2$—the inner-sidewall fringing capacitance ($C_{\rm FIS}$), $S3$—the drain-sidewall fringing capacitance ($C_{\rm FDS}$), and $S4$—the source sidewall capacitance ($C_{\rm FSS}$).

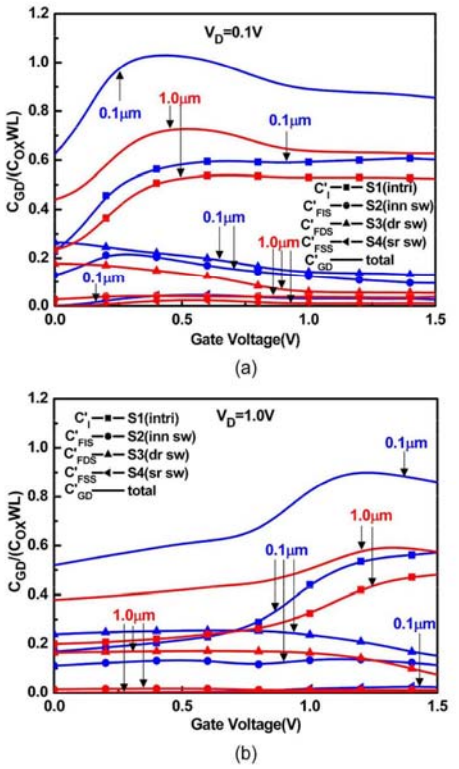

Fig. 4. Gate-drain capacitance ($C_{\rm GD}$) versus the gate voltage (V_G) of the mesa-isolated FD SOI NMOS device with channel widths of 0.1 and 1 μm, biased at V_D of (a) 0.1 V and (b) 1 V, considering the contributions from $S1$—the intrinsic gate capacitance (C'_I), $S2$—the inner-sidewall fringing capacitance ($C'_{\rm FIS}$), $S3$—the drain-sidewall fringing capacitance ($C'_{\rm FDS}$), and $S4$—the source sidewall capacitance ($C'_{\rm FSS}$).

where $C'_I = dQ_I/dV_D$, $C'_{\rm FIS} = dQ_{\rm FIS}/dV_D$, $C'_{\rm FDS} = dQ_{\rm FDS}/dV_D$, and $C'_{\rm FSS} = dQ_{\rm FSS}/dV_D$. Thus, via carrying out the differentiation of the integral of the charge in four surfaces ($S1 - S4$) of the poly gate at different biasing voltages based on the Davinci simulation results, the gate–source/drain capacitance of the device has been found.

Fig. 3 shows the gate–source capacitance ($C_{\rm GS}$) versus the gate voltage (V_G) of the mesa-isolated narrow-channel FD SOI NMOS device with channel widths of 0.1 and 1 μm, biased at V_D of 0.1 V [Fig. 3(a)] and 1 V [Fig. 3(b)]. Note that $C_{\rm GS}$ has been normalized by the $WLC_{\rm ox}$ of the device, where W/L is the channel width/length and $C_{\rm ox}$ is the unit-area gate-oxide capacitance. As shown in the figures, the contributions from $S1$—the intrinsic gate capacitance (C_I), $S2$—the inner-sidewall fringing capacitance ($C_{\rm FIS}$), $S3$—the drain-sidewall fringing capacitance ($C_{\rm FDS}$), and $S4$—the source sidewall capacitance ($C_{\rm FSS}$) are also plotted. Fig. 4 shows the gate-drain capacitance ($C_{\rm GD}$) versus the gate voltage (V_G) of the mesa-isolated FD SOI NMOS device with channel widths of 0.1 and 1 μm, biased at V_D of 0.1 V [Fig. 4(a)] and 1 V [Fig. 4(b)]. Note that various contributions–C'_I, $C'_{\rm FIS}$, $C'_{\rm FDS}$, and $C'_{\rm FSS}$–are also included. As shown in Fig. 3, with a narrower channel width (0.1 μm), the intrinsic gate capacitance (C_I) due to the electric field in $S1$ at the bottom of the poly gate becomes larger as compared to the 1-μm case due to the fringing electric field at the edges of the intrinsic gate region. With a narrower channel width (0.1 μm), the inner-sidewall fringing capacitance ($C_{\rm FIS}$) due to the electric field in $S2$, the inner back sidewall is also larger. A similar trend exists for the drain/source sidewall fringing capacitance ($C_{\rm FDS}/C_{\rm FSS}$) due to the electric field in $S3/4$—the drain/source sidewall. The source sidewall fringing capacitance $C_{\rm FSS}$ is greater than the drain-sidewall fringing capacitance $C_{\rm FDS}$. Considering the three fringing capacitances–$C_{\rm FIS}$, $C_{\rm FDS}$, $C_{\rm FSS}$–and the intrinsic gate capacitance (C_I), the total gate–source capacitance $C_{\rm GS}$ is larger for the case with a smaller channel width of 0.1 μm. As shown in Fig. 3, the intrinsic gate capacitance (C_I) is larger than the inner-sidewall fringing capacitance ($C_{\rm FIS}$). Among three fringing components, both the source sidewall fringing capacitance ($C_{\rm FSS}$) and the inner-sidewall capacitance ($C_{\rm FIS}$) are the dominant factors. As shown in Fig. 4, the contributions of the three fringing capacitances to $C_{\rm GD}$ are similar except

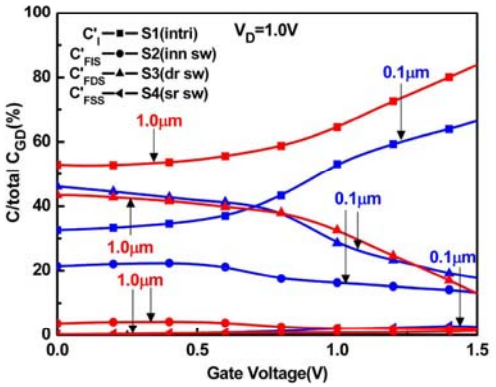

Fig. 5. Percentage contributions to the gate-drain capacitance ($C_{\rm GD}$) from $S1$—the intrinsic gate capacitance in the bottom of the poly gate (C'_I), $S2$—the inner-sidewall fringing capacitance ($C'_{\rm FIS}$), $S3$—the drain-sidewall capacitance ($C'_{\rm FDS}$), and $S4$—the source sidewall capacitance ($C'_{\rm FSS}$) versus the gate voltage (V_G) of the mesa-isolated FD SOI NMOS device with channel widths of 0.1 and 1 μm, biased at V_D of 1 V.

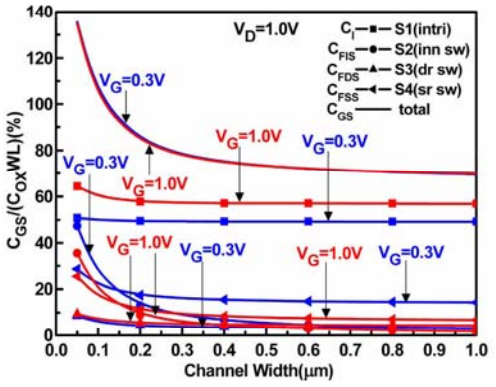

Fig. 6. Gate–source capacitance ($C_{\rm GS}$) versus channel width of the FD SOI NMOS device biased at $V_D = 1$ V and $V_G = 0.3$ V and 1 V, considering the contributions from $S1$—the intrinsic gate capacitance (C_I), $S2$—the inner-sidewall fringing capacitance ($C_{\rm FIS}$), $S3$—the drain-sidewall fringing capacitance ($C_{\rm FDS}$), and $S4$—the source sidewall capacitance ($C_{\rm FSS}$).

that the source sidewall fringing capacitance ($C'_{\rm FSS}$) is smallest. From Figs. 3 and 4, the 3-D fringing electric-field effects are important while considering $C_{\rm GS}/C_{\rm GD}$ of a narrow-channel FD SOI NMOS device. From the 3-D simulation analysis, the importance of the 3-D fringing electric-field effects, especially the fringing electric-field effects in the source/drain sidewall as well as that in the inner oxide sidewall, has been observed. Note that the influence of $C_{\rm FSS}/C'_{\rm FSS}$ and $C_{\rm FDS}/C'_{\rm FDS}$ depends on the choice of the sidewall structure, which is determined by technology considerations.

III. Discussion

More insight into the relative importance of the fringing capacitances could be obtained by studying the percentage contributions to $C_{\rm GD}$ from $S1$—the intrinsic gate capacitance (C'_I), $S2$—inner-sidewall capacitance ($C'_{\rm FIS}$), $S3$—the drain-sidewall capacitance ($C'_{\rm FDS}$), and $S4$—the source sidewall capacitance ($C'_{\rm FSS}$) versus the gate voltage of the mesa-isolated FD SOI NMOS device with channel widths of 0.1 and 1 μm, biased at V_D of 1 V, as shown in Fig. 5. In general, the intrinsic gate capacitance (C'_I) always dominates the gate-drain capacitance ($C_{\rm GD}$). With a narrower channel width, the dominance of the intrinsic gate capacitance recesses, indicating the more influence of the fringing capacitances. When the gate voltage is smaller, C'_I from $S1$ becomes less important in contributing to $C_{\rm GD}$, and $C'_{\rm FDS}$ from $S3$ becomes more important. With a narrower channel width of 0.1 μm, the contribution of $C'_{\rm FDS}$ from $S3$ is even higher than that of C'_I in $S1$. At V_G of 0.3 V, $C'_{\rm FDS}$ occupies 43% of the total $C_{\rm GD}$ while C'_I does only 33%. In addition, $C'_{\rm FIS}$ from $S2$ rises to 22%. This implies that the fringing electric field in $S2$ (the inner-sidewall oxide at the edge of the mesa-isolated structure) and $S3$ (the drain sidewall) dominates $C_{\rm GD}$.

Fig. 6 shows $C_{\rm GS}$ versus channel width of the FD SOI NMOS device, biased at $V_D = 1$ V and $V_G = 1$ V and 0.3 V.

C_{GS}

Length 0.18μm	Width	C_I(S1)	C_{FIS}(S2)	C_{FDS}(S3)	C_{FSS}(S4)
V_D=0.1V V_G=0.5V	0.1μm	57.29%	18.24%	4.89%	19.58%
	0.18μm	64.82%	11.90%	4.50%	18.78%
	1.0μm	73.61%	5.55%	3.81%	17.03%

(a)

C_{GS}

Length 90nm	Width	C_I(S1)	C_{FIS}(S2)	C_{FDS}(S3)	C_{FSS}(S4)
V_D=0.1V V_G=0.5V	0.1μm	56.59%	16.65%	6.36%	20.40%
	1.0μm	74.23%	6.06%	4.98%	14.73%

(b)

Fig. 7. Contributions from $S1$—the intrinsic gate capacitance (C_I), $S2$—the inner-sidewall fringing capacitance ($C_{\rm FIS}$), $S3$—the drain-sidewall fringing capacitance ($C_{\rm FDS}$), and $S4$—the source sidewall fringing capacitance ($C_{\rm FSS}$) to the gate–source capacitance ($C_{\rm GS}$) of the FD SOI NMOS device (a) with a channel length of 0.18 μm and channel widths of 0.1, 0.18, and 1 μm and (b) with a channel length of 90 nm and channel widths of 0.1, and 1 μm, biased at $V_D = 0.1$ V and $V_G = 0.5$ V.

As shown in the figure, when the channel width is greater than 0.4 μm, $C_{\rm GS}$ and all components–C_I, $C_{\rm FIS}$, $C_{\rm FDS}$, and $C_{\rm FSS}$–are almost constant, insensitive to variation in channel width. When the channel width is scaled down to below 0.1 μm, all contributing components–the inner-sidewall-oxide fringing capacitance ($C_{\rm FIS}$), the source sidewall fringing capacitance ($C_{\rm FSS}$), the drain-sidewall fringing capacitance ($C_{\rm FDS}$), and the gate intrinsic capacitance (C_I)–increase due to the more fringing electric field. As a result, the total $C_{\rm GS}$ may exceed 100% of $WLC_{\rm ox}$. Specifically, with a channel width of 0.05 μm, the inner-sidewall-oxide fringing capacitance ($C_{\rm FIS}$) occupies 35% of the total $C_{\rm GS}$, only next to the gate intrinsic capacitance (C_I), which occupies 37.5%, followed by

the source sidewall fringing capacitance ($C_{\rm FSS}$) with 21.1%, and the drain-sidewall fringing capacitance ($C_{\rm FDS}$) with 6.4%. Therefore, the importance of the fringing electric field in the inner-sidewall at the edge of the mesa-isolated structure cannot be overlooked while using the nanometer CMOS devices with a channel width of smaller than 0.1 μm. Fig. 7 shows the contributions from $S1$—the intrinsic gate capacitance (C_I), $S2$—the inner-sidewall fringing capacitance ($C_{\rm FIS}$), $S3$—the drain-sidewall fringing capacitance ($C_{\rm FDS}$), and $S4$—the source sidewall fringing capacitance ($C_{\rm FSS}$) to the gate–source capacitance ($C_{\rm GS}$) of the FD SOI NMOS device, with a channel length of 0.18 μm and channel widths of 0.1, 0.18, and 1 μm [Fig. 7(a)] and with a channel length of 90 nm and channel widths of 0.1 and 1 μm, biased at $V_D = 0.1$ V and $V_G = 0.5$ V [Fig. 7(b)]. As shown in Fig. 7(a), when the channel width is scaled down, the contribution from $S2$–the inner-sidewall fringing capacitance ($C_{\rm FIS}$)–increases from 5.55% at $W = 1$ μm to 11.9% at $W = 0.18$ μm and 18.24% at $W = 0.1$ μm. As shown in Fig. 7(b), with a smaller channel length of 90 nm, $C_{\rm FIS}$ increases from 6.06% at $W = 1$ μm to 16.65% at $W = 0.1$ μm. Thus, a smaller channel width leads to a more contribution of the inner-sidewall fringing capacitance ($C_{\rm FIS}$) to the gate–source capacitance ($C_{\rm GS}$).

IV. Conclusion

In this paper, an analysis of the $C_{\rm GS}/C_{\rm GD}$ behavior of a narrow-channel FD SOI NMOS device considering the 3-D fringing capacitances has been reported. Based on the 3-D simulation results, when the width of the FD SOI NMOS device is scaled down to 0.05 μm, the $C_{\rm FIS}$, due to the fringing electric field at the edge of the mesa-isolated structure of the FD SOI NMOS device biased at $V_G = 0.3$ V and $V_D = 1$ V, is the second largest contributor to the $C_{\rm GS}$. Thus, when using nanometer CMOS devices with a channel width smaller than 0.1 μm, $C_{\rm FIS}$ cannot be overlooked for modeling $C_{\rm GS}/C_{\rm GD}$.

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References

[1] J. B. Kuo and S. C. Lin, *Low-Voltage SOI CMOS Devices and Circuits*. New York: Wiley Interscience, 2001.

[2] J. B. Kuo, Y. G. Chen, and K. W. Su, "Sidewall-related narrow channel effect in mesa-isolated fully-depleted ultrathin SOI NMOS devices," *IEEE Electron Device Lett.*, vol. 16, no. 9, pp. 379–381, Sep. 1995.

[3] H. Wang, M. Chan, Y. Wang, and P. K. Ko, "The behavior of narrow-width MOSFET's with MESA isolation," *IEEE Trans. Electron Devices*, vol. 47, no. 3, pp. 593–600, Mar. 2000.

[4] K. W. Su and J. B. Kuo, "Analytical threshold voltage formula including narrow channel effects for VLSI MESA-isolated FD ultrathin SOI NMOS devices," *Jpn. J. Appl. Phys.*, vol. 34, no. 8A, pp. 4010–4019, Aug. 1995.

[5] ——, "Compact current model for mesa-isolated FD SOI NMOS devices considering sidewall-related narrow channel effects," in *Proc. IEEE SOI Conf. Dig.*, 1997, pp. 84–85.

[6] G. Katti, N. DasGupta, and A. DasGupta, "Threshold voltage model for Mesa-isolated small geometry fully depleted SOI MOSFETs based on analytical solution of 3-D Poisson's equation," *IEEE Trans. Electron Devices*, vol. 51, no. 7, pp. 1169–1177, Jul. 2004.

[7] K. Kumagai, H. Iwaki, A. Yoshino, and S. Kurosawa, "A 3-D analysis of source/drain capacitance in SOI MOSFET for practical circuit design," in *Proc. IEEE SOI Conf.*, Oct. 1994, pp. 15–16.

[8] *Three-Dimensional Device Simulator Program*. Palt Alto, CA: Technology Modeling Associates, Inc. , 1996.

[9] P. Yang and P. K. Chatterjee, "SPICE modeling for small geometry MOSFET circuits," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. CAD-1, no. 4, pp. 169–182, Oct. 1982.

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行政院國家科學委員會補助專題研究計畫

考慮邊際電場效應之次九十奈米互補金氧半超大型積電精簡元件模型(2/3)

計畫類別：□x 個別型計畫　　□ 整合型計畫

計畫編號：NSC 95-2221-E-002-369

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計畫主持人：郭正邦

出席國際學術會議心得報告及發表之論文各一份

執行單位：台大電機系

中　華　民　國　96　年　　5　月　27　日

此次補助出席了四月下旬於溫哥華舉行的加拿大電機電子會議(CCECE)發表論文: Triple-Threshold Static Power Minimization Technique in High-Level Synthesis for Designing High-Speed Low-Power SOC Applications Using 90nm MTCMOS Technology. 將出席六月於北京舉行的 IEDST 發表 invited paper: Modeling the Gate Tunneling Current Effects of Sub-100nm NMOS Devices with an Ultra-thin (1nm) Gate Oxide”此次演講係清華大學及 IEEE Electron Devices Society 共同舉辦 此演講亦是 IEEE Electron Devices Society 的傑出演獎(distinguished lecture). 兩次出席國際會議 收獲很多 感謝國科會支持.

Modeling the Gate Tunneling Current Effects of Sub-100nm NMOS Devices with an Ultra-thin (1nm) Gate Oxide

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Abstract

This paper reports the modelling the gate tunneling current effects of sub-100nm NMOS devices with an ultra-thin (1nm) gate oxide. As verified by the experimentally measured data, the compact gate tunneling current model considering the distributed effect provides an accurate prediction of the gate, source, and drain currents for the device biased in triode and saturation regions. Based on the compact model, the negative gate current could be successfully explained as a result of the opposite direction of the local vertical electric field in the gate oxide near drain.

1. Introduction

Gate leakage current due to direct tunneling through the gate oxide may cause serious problems for nanometer CMOS devices with an ultra-thin gate oxide [1][2]. Gate tunneling current, which is distributed along the lateral channel, may bring in difficulties in modeling of it. For effective calculation of the gate tunneling current effects, an accurate compact gate tunneling current model is necessary. In this paper, following a double integral approach as for deriving the partitioned-charge model [3], the compact gate tunneling gate current model considering the distributed effect for an NMOS device with a 1nm gate oxide is described.

2. Compact Model

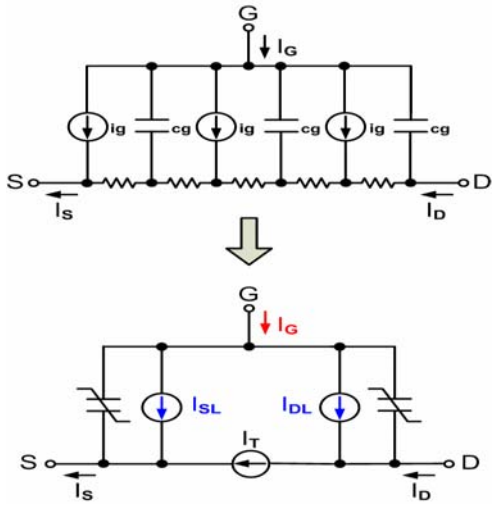

Fig. 1 (a) Distributed and (b) partitioned gate tunneling current models.

Fig. 1 shows (a) distributed and (b) compact gate tunneling current models for the nanometer NMOS device with an ultra-thin gate oxide under study as shown in Fig. 2. As shown in Fig. 1(a), the local gate tunneling current varies depending on the location in the channel. In the compact gate tunneling current model as shown in Fig. 1(b), the total gate current is divided into two lumps-(1) the source-side part I_{SL} and (2) the drain-side part I_{DL}: $I_G=I_{SL}+I_{DL}$ as Eq.(1) in Fig. 3. Following the approach for deriving the partitioned charge model for MOS devices [3], the partitioned gate tunneling current at source/drain I_{SL}/I_{DL} is expressed as Eq.(2)/(3) in Fig. 3, where

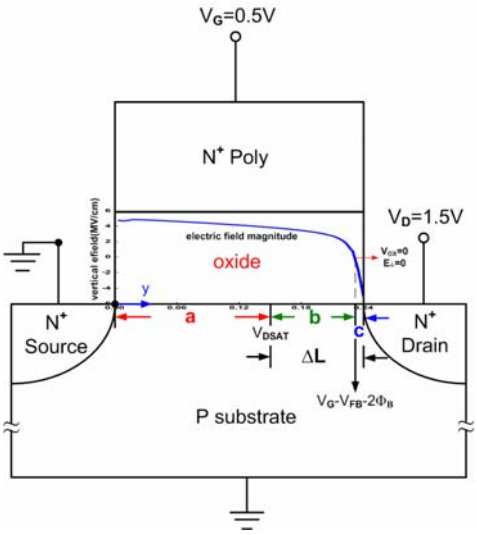

Fig. 2 Cross section of the NMOS device with an ultrathn gate oxide under study.

$J_G(y)$ is the local gate tunnel current at location y in the channel: $J_G(y) = J_{G0}e^{-B^*V(y)}$. When biased in the saturation, the lateral channel could be divided into three segments as shown in Fig. 2: Segment a- before the velocity saturation with its channel potential between 0V and V_{dsat} ($0<V(y)<V_{dsat}$), Segment b- after velocity saturation and zero vertical electric field in the gate oxide ($V_{dsat}<V(y)<V_G-V_{fb}-2\varphi_b$), and Segment c- $V_G-V_{fb}-2\varphi_b <V(y)<V_D$. In Segment a, the triode region formula [4] could be used to find its total gate current I_{Ga} with L replaced by L-ΔL and V_D by V_{dsat}, where ΔL is the length of the post-saturation region. In Segments b and c- post-saturation region, the local gate tunnelling current density is $J_G(y)=J_{G0}$ exp(-$2B^*$($V_G-V_{fb}-2\varphi_b$- 0.5V)). The total gate current I_{Gb}/I_{Gc} in Segment b/c has been found- Eq.(10)/(13). Thus, the total gate current is $I_G=I_{Ga}+I_{Gb}+I_{Gc}$. Source current is $I_S=I_T+I_{SL}$ Eq.(5) and drain current is $I_D=I_T-I_{DL}$ Eq.(6), where $I_{SL}=I_{SLa}+I_{SLb}+I_{SLc}$ and $I_{DL}=I_{DLa}+I_{DLb}+I_{DLc}$ with components as shown in Fig. 3. This completes the compact model of the gate tunnelling current for the NMOS device considering the distributed effect.

$$I_G = I_{SL} + I_{DL} = W\int_0^L J_G dy \quad (1)$$

$$I_{SL} = \frac{W}{L}\int_0^L \int_0^y J_G(y')dy'dy = W\int_0^L \left(1-\frac{y}{L}\right) J_G(y)dy \quad (2)$$

$$I_{DL} = W\int_0^L \frac{y}{L} J_G(y)dy \quad (3)$$

$$I_T = \mu_n C_{ox}\frac{W}{L}\left[(V_G - V_T)V_{DS} - \frac{m}{2}V_{DS}^2\right] \quad (4)$$

$$I_S = I_T + I_{SL} \quad (5)$$

$$I_D = I_T - I_{DL} \quad (6)$$

$$I_{Ga} = \frac{J_{G0}W(L-s\Delta L)}{B^*\left[(V_G-V_T)V_{dsat} - \frac{m}{2}V_{dsat}^2\right]}\left\{V_G - V_T - \frac{m}{B^*} + e^{-B^*V_{dsat}}\left[mV_{dsat} - (V_G - V_T) + \frac{m}{B^*}\right]\right\} \quad (7)$$

$$I_{SLa} = W\int_0^{L-s\Delta L}\left(1-\frac{y}{L}\right)J_G dy \quad (8)$$

$$I_{DLa} = W\int_0^{L-s\Delta L}\frac{y}{L}J_G dy = I_{Ga} - I_{SLa} \quad (9)$$

$$I_{Gb} = W\int_{L-s\Delta L}^{L-s\Delta L+y_1} J_G(y')dy = W\int_0^{y_1} J_{G0}\exp\left[-B^*\left(V_{dsat} + lE_{sat}\sinh\frac{y'}{l}\right)\right]dy' \quad (10)$$

$$I_{SLb} = W\int_{L-\Delta L}^{L-\Delta L+y_1}\left(1-\frac{y}{L}\right)J_G dy = I_{SLb0} - W\int_0^{y_1}\frac{y'+L-\Delta L}{L}J_{G0}\exp\left(-B^*V\right)dy' \quad (11)$$

$$I_{DLb} = W\int_{L-\Delta L}^{L-\Delta L+y_1}\frac{y}{L}J_G(y)dy = I_{Gb} - I_{SLb} \quad (12)$$

$$I_{Gc} = -W\int_{L-\Delta L+y_1}^{L} J_{G0}\exp\left[-B^*(2V_g - V(y))\right]dy \quad (13)$$

$$I_{SLc} = -W\int_{L-\Delta L+y_1}^{L}\left(1-\frac{y}{L}\right)J_G dy = I_{Gc} + W\int_{L-\Delta L+y_1}^{L}\frac{y}{L}J_G dy \quad (14)$$

$$I_{DLc} = -W\int_{L-\Delta L+y_1}^{L}\frac{y}{L}J_G dy = I_{Gc} - I_{SLc} \quad (15)$$

Fig. 3. Key equations of the gate tunneling current model.

3. Model Evaluation

The effectiveness of this compact model of the gate tunneling current considering the distributed effect for the NMOS device with an ultra-thin gate oxide has been evaluated with the experimentally measured data of the test device with the gate oxide 1nm. Fig. 4 shows total gate current I_G, the partitioned gate currents at the source side I_{SL} and at the drain side I_{DL} versus the drain voltage of the NMOS device with the 1nm gate oxide and with the channel width of (a) 10um, (b) 0.24um and (c) 100nm, based on the compact model with and without considering the distributed gate tunneling current and the experimentally measured data. As shown in the figure, as verified by the experimentally measured data, the compact gate tunneling current model provides an accurate prediction of I_G, I_{SL}, and I_{DL} in both the triode and the saturation regions. Without the compact gate tunneling current model, I_G, I_{SL}, and I_{DL} couldn't be modeled. Fig. 5 shows the total gate current versus V_D of the NMOS device with the 1nm gate oxide and with the channel length of 10um, 0.24um and 100nm, biased at V_G=0.5V and 0.7V in the saturation region, based on the compact

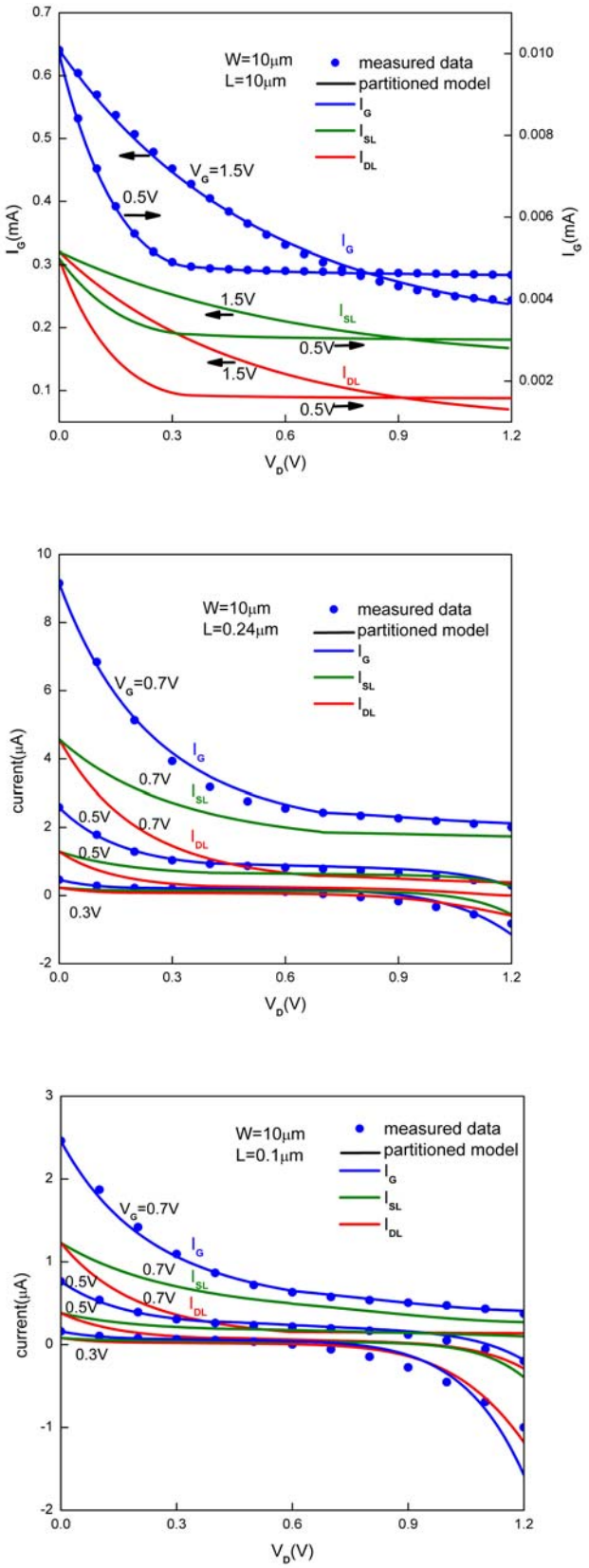

Fig. 4 $I_G/I_{SL}/I_{DL}$ versus V_D of the NMOS device with the gate oxide of 1nm and (a) L=10um, (b) L=0.24um and (c)100nm.

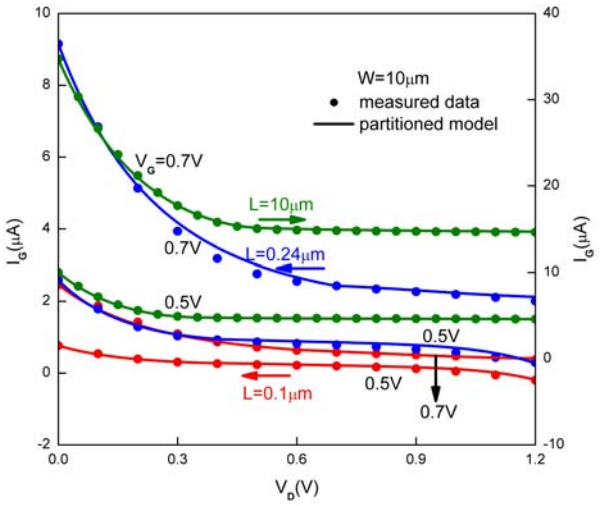

Fig. 5 I_G versus V_D of the device with L=10/0.24/0.1um

model with and without considering the distributed gate tunneling current and the experimentally measured data. As shown in the figure, the compact model considering the distributed gate tunneling current could predict the total gate current as verified by the experimentally measured data. Fig. 6 shows the source and the drain currents versus the drain voltage of the NMOS device with the 1nm gate oxide and with the channel length of 10μm, 0.24um and 100nm, biased at (a) V_G=1.1V and (b) V_G=0.5V, based on the compact model with and without considering the distributed gate tunneling current and the experimentally measured data. As shown in the figure, without considering the distributed gate tunneling effect, a substantial error exists between the model result and the experimentally measured data, especially when V_D is large.

4. Discussion

More insights into device operation could be obtained by the studying the currents in each segment of the device.

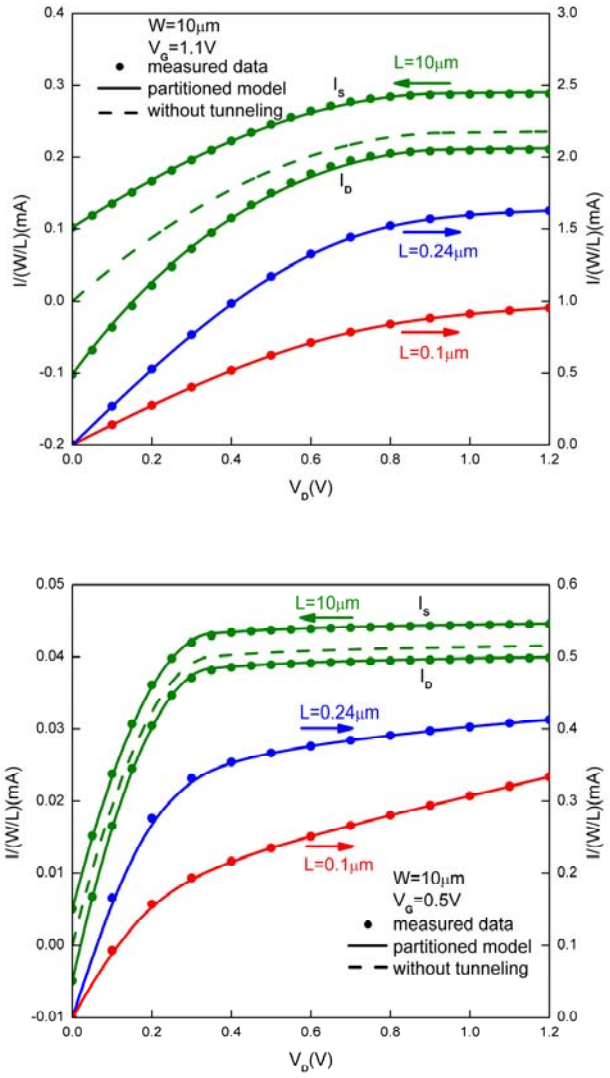

Fig. 6 I/(W/L) versus V_D of the device with the gate oxide of 1nm biased at (a) V_G=1.1V and (b) V_G=0.5V

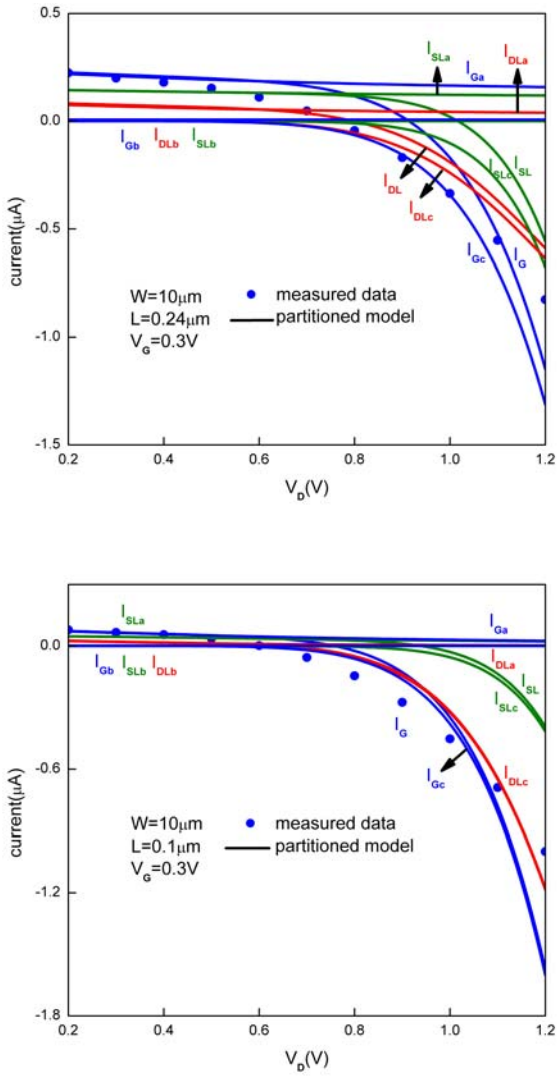

Fig. 7 Current components versus V_D of the device with the gate oxide of 1nm and with (a)L=0.24um and (b) L=100nm.

Fig. 7 shows the total gate current (I_G) with its components in Segments A, B and C, the source-end partitioned gate current (I_{SL}) and its components, and the drain-end partitioned gate current (I_{DL}) and its components versus V_D of the NMOS device with the 1nm gate oxide and the channel length of (a) 0.24um and (b) 100nm biased at V_G=0.3V based on the partitioned gate tunneling current model. As shown in the figure, at a large V_D, I_{SLc}, I_{DLc}, and I_{Gc} in Segment C become negative and dominating. Using the partitioned gate tunneling current model, this complex phenomenon could be modeled accurately.

References

[1] C. Choi et al, "Impact of Gate Direct Tunneling Current in Circuit Performance," IEEE TED pp. 2823-29, Dec 1000.

[2] W.Lu et al, "Modeling CMOS Tunneling Curr Thru Ultrathin Gate Oxide Due to Tunneling," IEEE TED, pp.1366-73, 01.

[3] D.Ward et al, "A Charge-Oriented Model for MOS Transistor Capacitances," IEEE JSSC, pp. 703-08, 1978.

[4] C. Lin et al, "Partitioned Gate Tunneling Current Model Considering Distributed Effect," Elec Lett, pp. 182-84, 2006.

Triple-Threshold Static Power Minimization Technique in High-Level Synthesis for Designing High-Speed Low-Power SOC Applications Using 90nm MTCMOS Technology

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Abstract— **This paper reports a novel triple-threshold static power minimization technique in high-level synthesis of high-speed low-power SOC applications. Using 90nm multi-threshold CMOS (MTCMOS) technology, we evaluate the performance and power dissipation of benchmark circuits synthesized using transistors with different threshold voltages. Using static timing analysis, we determine the timing requirements of cells and place cells with low and standard threshold voltages in the critical paths. Cells with a high threshold voltage are placed in non-critical paths to minimize the static power with no overall timing degradation. From the timing and power analysis, we determine the optimal placement of high, standard and low threshold voltage cells. Applying the new triple-threshold technique to optimize 20 circuits originating from the ISCAS'99 benchmark, we have achieved an average saving of 85.3% in the static power compared to conventional all-LVT circuits, and 39.6% saving compared to the dual-threshold (HVT+LVT) technique.**

Keywords-triple-threshold, high speed, low power, high-level synthesis, digital CMOS VLSI

I. INTRODUCTION

Advances in CMOS technology allow MOS transistor sizes to be continuously scaled down in progressively smaller technology nodes. As transistor sizes become smaller, supply voltages can be lowered to reduce the power dissipation. In order to achieve high speed with low supply voltages, the threshold voltage must be reduced accordingly. A fast submicron CMOS transistor designed for 1V operation typically has a threshold voltage of 0.1-0.2V, which enables higher switching speeds albeit at the expense of dissipating more static power due to subthreshold leakage currents. To alleviate the problem, device manufacturers usually supply standard cell libraries built of MOS transistors with high, standard, and low threshold voltages (HVT, SVT, and LVT). The HVT cells (or gates) operate at the slowest speed but dissipate the least amount of static power, whereas the LVT cells can operate at faster speeds but dissipate much larger static power. Traditionally, VLSI designers build circuits using transistors with only one threshold voltage. With the availability of multi-threshold CMOS (MTCMOS) technology, the optimal placement of transistors with different threshold voltages becomes important for low-power circuits.

II. RELATED WORK

In CMOS technology, the total dissipated power consists of dynamic and static power. The static power becomes more dominant as CMOS technology progresses towards deep sub-micron nodes [1]. Typical attempts to minimize static power rely on the use of HVT transistors in non timing-critical paths and LVT transistors in paths where a high speed is necessary. Dual threshold-voltage techniques have been proposed [2]-[6] to determine the optimal placement of the HVT and LVT cells.

The previous reported approaches [2] and [3] minimize static power during high-level synthesis, while [4]-[6] minimize static power at the transistor level. Transistor-level designs typically use SPICE modelling to determine accurate timing waveforms and current flows for each transistor. Since large designs usually consist of repetitive building blocks such as inverters and NAND gates, the circuit simulation time can be reduced if the modelling is performed at the gate level instead. For high-level synthesis, device manufacturers supply standard sets of cell libraries with corresponding timing and power dissipation information, and commercial tools from vendors such as Cadence™ and Synopsys™ are available to synthesize the circuits. Circuits can be designed by specifying the exact placement of gates using a gate-level RTL language such as Verilog, or by describing circuit functionalities with a high-level language such as VHDL. High-level synthesis requires less simulation time compared to transistor-level modelling, and developing appropriate methodologies for optimizing the placement of MTCMOS gates during high-level synthesis is necessary.

As it has been proposed in [2], a circuit is first synthesized using only HVT cells. Each HVT cell in the critical path is temporarily replaced by its LVT counterpart cell to record the amount of reduction in the delay time. The cell that produces the largest delay time reduction is changed permanently from

HVT to LVT. This method is effective for small designs, but may be inefficient for large designs since timing analysis has to be repeated for a large number of cells in the critical paths. In [3], only the highest cost cells in the critical paths are changed from HVT to LVT, where the cost is defined as the number of critical paths passing through the cell. Although this approach may not result in the lowest static power dissipation, we have found designs produced using this technique to be close to optimal. The approach described in [3] is faster to perform than [2] and is thus more suitable for large designs.

Triple-threshold techniques have also been used to minimize the static power [7][8]. Previous attempts use HVT transistors as sleep transistors for logic blocks. Within each logic block, the circuits are optimized using the dual-threshold technique, placing SVT transistors in non-critical paths and LVT transistors in critical paths. Since HVT cells dissipate static power that is an order of magnitude less than the static power dissipation of SVT cells, a new triple-threshold technique has been proposed that places HVT cells within the logic blocks in addition to SVT and LVT cells [9].

In this paper, we present the results of optimizing the ISCAS'99 benchmark circuits with the new triple-threshold technique [9]. HVT cells are placed in non-critical paths while SVT and LVT cells are placed in critical paths to achieve the fastest clock speed and the lowest static power dissipation. All of the benchmark circuits optimized using the triple-threshold technique have resulted in the lowest static power dissipations.

III. Comparison of the Standard Cell Libraries

A. Characterizing Standard Cell Libraries

Synopsys Design Compiler™ is used to synthesize a 16-bit Wallace-tree multiplier, which contains 1123 cells in total. Timing analysis is performed with Synopsys PrimeTime™ to extract the longest delay paths and obtain the clock speed information. Design Compiler™ is used to report the circuit's static power dissipation. The multiplier circuit is synthesized three times: with the HVT library only, with the SVT library only, and with the LVT library only. Based on the simulation result, we determine the relative performance and static power dissipation of the three libraries, as shown in Table I.

The simulation results indicate that there is an order of magnitude difference in the static power between each cell library. The HVT design dissipates the lowest static power, and the LVT design dissipates static power that is two orders of magnitude larger than the HVT design. For large SOC designs, minimizing the use of SVT and LVT cells would thus lead to significant savings in the static power dissipation. The triple-threshold technique will allow designs to run at the fastest clock speed as the LVT design while minimizing static power.

B. Static Power Calculations

All static power dissipation values in the simulations in this paper are obtained from Design Compiler™. For each cell, the 90nm standard cell library contains a static power value for each possible input state. Design Compiler™ calculates a cell's static power by multiplying the static power value for each state by the percentage of the total simulation time at that state. The total static power of a circuit is then calculated by summing the static power of each cell in the circuit.

TABLE I. Performance comparison of a 16-bit Wallace tree multiplier synthesized using HVT, SVT and LVT libraries

Library	HVT	SVT	LVT
NMOS V_T [V]	0.32	0.24	0.18
PMOS V_T [V]	-0.36	-0.29	-0.24
Longest Delay [ns]	3.4	2.6	2.1
Max Clock Speed [MHz]	294.1	384.6	476.2
Static Power [μW]	0.75506	14.4600	270.7120

IV. Power Minimization Methodology

We adopt the triple-threshold technique proposed in [9]. The triple-threshold technique relies heavily on static timing analysis for selecting critical paths. A critical path is a path from an input to an output where the total delay exceeds the timing constraint. We define the cost of a cell as the number of critical paths passing through the cell. A circuit is first synthesized using the LVT library. Using PrimeTime™ for static timing analysis, we determine the shortest clock period that can be attained. In the 16-bit LVT multiplier example, the shortest clock period is 2.1 ns. We change the all-LVT circuit to its all-HVT version, and set the timing constraint to 2.1 ns. Since the HVT multiplier can only run at a clock period of 3.4 ns, timing violation occurs and we can use PrimeTime™ to determine the critical paths in the design.

Starting with the constrained HVT design, at each iteration, the highest cost HVT cell is replaced by its SVT counterpart to improve timing. Static timing analysis is repeated to determine the highest cost cell for the next iteration. Since the SVT multiplier only runs at a clock period of 2.6 ns and cannot meet the timing constraint of 2.1 ns, all HVT cells in the critical paths will be replaced by SVT cells and timing violation will occur. At subsequent iterations, the highest cost SVT cells in the critical paths will be replaced by LVT cells until the timing constraint is met. Fig. 1 shows a flow chart of the algorithm.

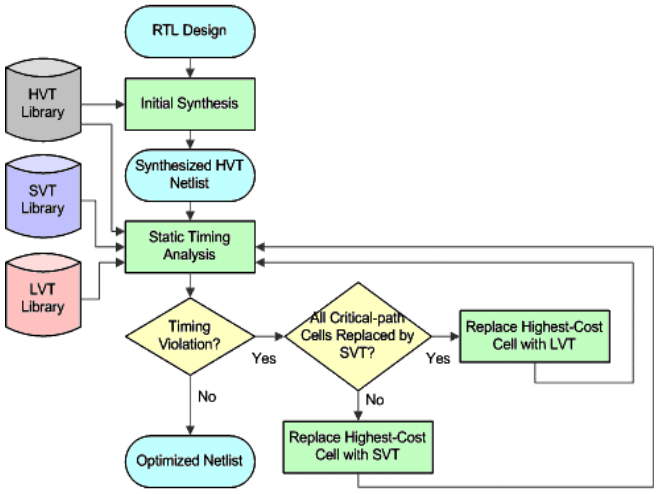

Figure 1. Triple-threshold power minimization flow [9]

V. Simulation of Benchmark Circuits

We synthesized 20 ISCAS'99 benchmark circuits using the conventional method (LVT only), and optimize the circuits using the dual-threshold (HVT+LVT) and the triple-threshold techniques. The circuits in VHDL code are synthesized with Design Compiler™ and saved as Verilog files for static timing analysis in PrimeTime™. Timing constraint is set to the shortest clock period attainable with the all-LVT circuit for each design. The results are shown in Tables II and III.

The schematics of the circuit B02 optimized with the dual- and triple-threshold techniques are shown in Fig. 2. The dual-threshold optimized circuit (Fig. 2a) contains 11 HVT cells (shaded in black stripes) and 7 LVT cells (shown in red outline). The triple-threshold optimized circuit (Fig. 2b) contains 7 HVT cells, 7 SVT cells (shaded in blue dots), and 4 LVT cells. The triple-threshold circuit has reduced 30.17% of static power compared to the dual-threshold circuit by reducing the number of LVT cells and using additional SVT cells to meet the timing requirements.

TABLE II. Static Power Savings for Triple-Threshold Circuits

Circuit	# of Gates	Clock Period (ns)		Static Power (µW)				% Saving vs. LVT		Tri-Vt % Sav. vs. Dual-Vt
		HVT	*LVT*	*HVT*	*LVT*	*Dual-Vt*	*Tri-Vt*	*Dual-Vt*	*Tri-Vt*	
B02	18	0.45	0.28	0.0091	3.164	1.591	1.111	49.73	64.89	30.17
B01	29	0.61	0.38	0.0145	4.997	2.060	1.838	58.77	63.21	10.78
B06	41	0.67	0.43	0.0226	7.972	2.945	1.893	63.06	76.26	35.73
B09	87	1.04	0.65	0.0614	22.071	10.427	4.754	52.76	78.46	54.41
B03	90	1.23	0.77	0.0688	24.049	5.766	2.890	76.02	87.98	49.89
B08	91	1.32	0.83	0.0606	20.861	4.763	2.707	77.17	87.03	43.17
B10	109	1.08	0.68	0.0603	20.680	4.854	3.532	76.53	82.92	27.23
B13	175	0.83	0.53	0.1307	45.712	9.004	6.457	80.30	85.88	28.29
B07	189	1.43	0.89	0.1262	43.718	10.603	6.052	75.75	86.16	42.92
B11	211	2.26	1.39	0.1294	45.003	15.803	8.695	64.88	80.68	44.98
B04	310	1.32	0.83	0.1835	62.347	20.590	12.880	66.98	79.34	37.44
B05	334	2.15	1.36	0.1656	55.328	16.042	12.325	71.01	77.72	23.17
B12	636	1.89	1.17	0.3792	131.733	7.240	3.488	94.50	97.35	51.83
B14	3125	6.79	4.27	2.5048	846.744	98.073	48.893	88.42	94.23	50.15
B15	3269	8.89	5.60	1.8091	618.743	75.076	61.863	87.87	90.00	17.60
B21	6509	6.82	4.29	5.2047	1759.100	208.238	74.567	88.16	95.76	64.19
B20	6556	6.85	4.33	5.2104	1763.200	206.720	59.766	88.28	96.61	71.09
B22	9826	6.88	4.36	7.8914	2676.900	317.651	82.446	88.13	96.92	74.05
B17	10081	9.00	5.67	5.7131	1956.900	214.189	184.386	89.05	90.58	13.91
B18	29202	9.17	5.78	18.6098	6314.900	486.794	380.093	92.29	93.98	21.92
Avg.				2.4178	821.206	85.921	48.032	76.48	85.30	39.65

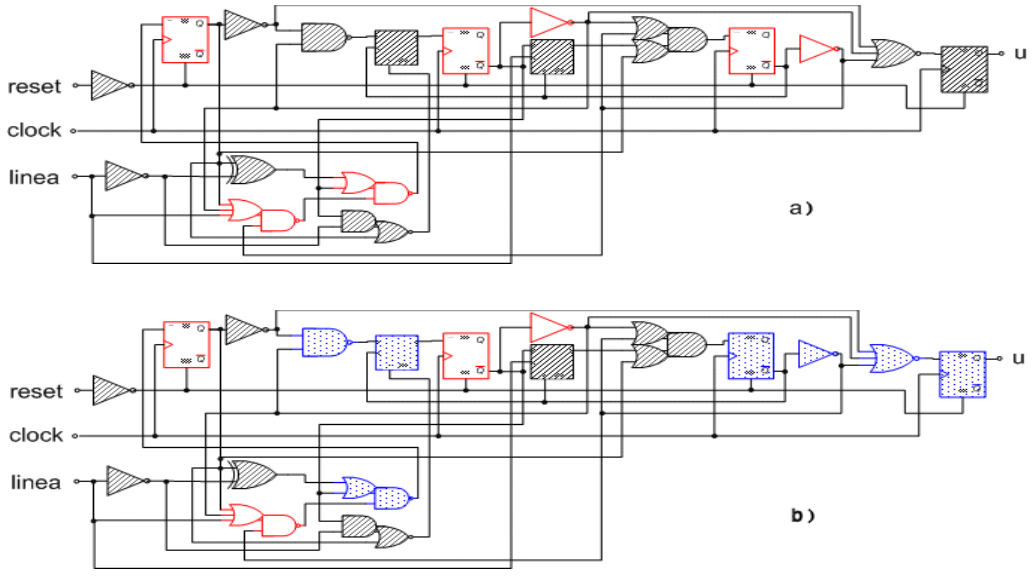

Figure 2. Circuit B02 optimized with a) the dual-threshold technique and b) the triple-threshold technique

TABLE III. COMPOSITION OF GATES IN OPTIMIZED CIRCUITS

Circuit	Total # Gates	Dual-Vt # Gates		Tri-Vt # Gates		
		HVT	*LVT*	*HVT*	*SVT*	*LVT*
B02	18	11	7	7	7	4
B01	29	19	10	12	8	9
B06	41	29	12	18	15	8
B09	87	49	37	54	14	19
B03	90	69	21	45	32	13
B08	91	68	23	66	10	15
B10	109	76	33	46	40	23
B13	175	142	33	119	35	21
B07	189	152	37	123	49	17
B11	211	141	70	115	58	38
B04	310	222	88	183	75	52
B05	334	265	69	251	34	49
B12	636	594	42	551	66	19
B14	3125	2826	299	2541	436	148
B15	3269	2961	308	2697	374	198
B21	6509	5883	626	5280	995	234
B20	6556	5921	635	5388	974	194
B22	9826	8856	970	8049	1513	264
B17	10081	9173	908	8362	1141	578
B18	29202	27104	2098	2566	2312	1230

The static power for each circuit is plotted in Fig. 3. As expected, the static power increases as the total number of gates within a circuit increases. The number of LVT cells for each circuit is plotted in Fig. 4. For the dual-threshold and triple-threshold circuits, since most of the static power is dissipated by the LVT cells, it becomes obvious that the number of LVT cells in a circuit correlates to the amount of static power dissipated by the circuit.

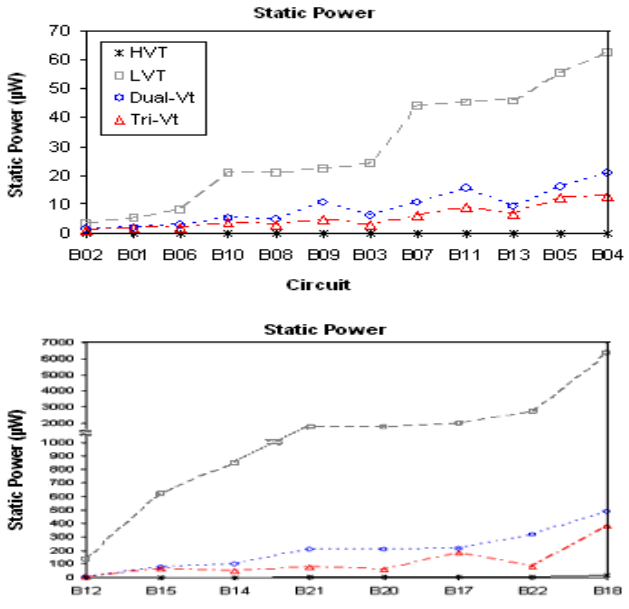

Figure 3. Static power dissipation of benchmark circuits

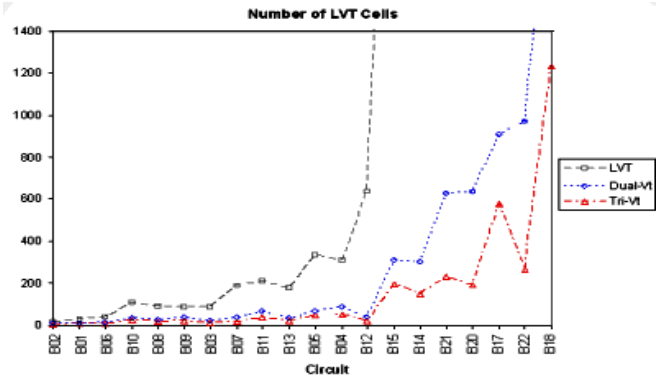

Figure 4. Number of LVT cells in each circuit

VI. CONCLUSIONS

We have presented a novel triple-threshold static power minimization technique for high-level synthesis of large digital circuits. We apply the technique to optimize 20 ISCAS'99 benchmark circuits, and have achieved on average 85.3% less static power compared to the conventional method using only LVT cells. With the seven largest circuits, the average saving becomes 94%. Compared with the dual-threshold (HVT+LVT) technique, the triple-threshold circuits dissipate on average 39.4% less static power. The presented triple-threshold technique optimizes circuits to maintain their operation at the highest possible speed while saving the most static power compared with other techniques known in literature.

REFERENCES

[1] N.S. Kim, T. Austin, D. Baauw, T. Mudge, K. Flautner, J.S. Hu, M.J. Irwin, M. Kandemir, and V. Narayanan, "Leakage current: Moore's Law meets static power," IEEE Computer, pp. 68–75, December 2003.

[2] K. Shin and T. Kim, "Leakage power minimization in arithmetic circuits," Electronics Letters, Vol. 40, pp. 415–417, April 2004.

[3] B. Chung and J.B. Kuo, "Gate-level dual-threshold static power optimization methodology (GDSPOM) for designing high-speed low-power SOC applications using 90nm MTCMOS technology," ISCAS, 2006.

[4] L. Wei, Z. Chen, K. Roy, M.C. Johnson, Y. Ye, and V.K. De, "Design and optimization of dual-threshold circuits for low-voltage low-power applications," IEEE Trans. on VLSI Systems, pp. 16–24, March 1999.

[5] M. Anis, S. Areibi, and M. Elmasry, "Design and optimization of multithreshold CMOS (MTCMOS) circuits," IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems, pp. 1324–1342, October 2003.

[6] M. Srivastav, S.S.S.P. Rao, and H. Bhatnagar, "Power reduction technique using multi-Vt libraries," System-on-Chip for Real-Time Applications, pp. 363–367, July 2005.

[7] K. Fujii, T. Douseki, and M. Harada, "A sub-1 V triple-threshold CMOS/SIMOX circuit for active power reduction," ISSCC Digest of Technical Papers, pp. 190–191, February 1998.

[8] K. Fujii and T. Douseki, "A 0.5-V, 3-mW, 54×54-b multiplier with a triple-Vth CMOS/SIMOX circuit scheme," IEEE International SOI Conference, pp. 73–74, October 1999.

[9] H.I.A. Chen, E.K.W. Loo, J.B. Kuo, and M.J. Syrzycki, "Triple-threshold static power minimization in high-level synthesis of VLSI CMOS," Electronics Letters, 2007 (Submitted).