The Effect of Extrinsic Capacitances on the Microwave Performance of $Ga_{0.51}In_{0.49}P/GaAs$ MISFET's (0 nm $\leq$ t $\leq$ 10 nm) Grown by GSMBE

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ABSTRACT

The effect of extrinsic capacitances on the microwave performance of $Ga_{0.51}In_{0.49}P/GaAs$ MISFET's was first studied experimentally and theoretically by varying the thickness of the $Ga_{0.51}In_{0.49}P$ insulating layer. MISFET's with airbridge gate structure showed higher f_t's and f_{max}'s than those of MISFET's with traditional gate structure due to the lower extrinsic capacitances. Moreover, the maximum values of f_t's and f_{max}'s for a 1 μm gate length device all happen when t is between 50 nm and 100 nm. These results demonstrate that $Ga_{0.51}In_{0.49}P/GaAs$ airbridge gate MISFET's with insulator thickness between 50 nm and 100 nm were very suitable for microwave high power device applications.

I. INTRODUCTION

An electronic device with high-linearity, high-power and high-speed performance is very important for microwave power applications. A device with good linear characteristics can reduce the intermodulation of high frequency signals, and therefore the distortion of signals at high power level operation is suppressed. It has been demonstrated that if a low-doped or an undoped layer is inserted between the gate metal and the active channel of a MESFET structure, the linearity, current drivability and breakdown voltage characteristics are greatly improved [1-2]. Even though the transconductance is lower than that of the conventional MESFET's, yet the reduced gate terminal capacitance C_g (i.e., gate-source capacitance C_{gs} plus gate-drain capacitance C_{gd}) makes the ratio, g_m/C_g , higher [3-4], and hence the high frequency performance is also improved. Therefore, we would like to study the performance of the metal-undoped $Ga_{0.51}In_{0.49}P$-n GaAs traditional and airbridge gate MISFET's with different insulator thickness t and compare them with similar MESFET's (t = 0 nm).

II. CRYSTAL GROWTH AND DEVICE TECHNOLOGY

The heterostructures were grown by gas source molecular beam epitaxy (GSMBE) on semi-insulating (100) GaAs substrates. They consisted of a 1000 nm undoped GaAs buffer, followed by a 100 nm GaAs n channel layer (6×10^{17} cm^{-3} , Si doped). Then an undoped $Ga_{0.51}In_{0.49}P$ insulator layer was grown on top of the active channel. Finally, a 40 nm n^+ (2×10^{18} cm^{-3} , Si doped) GaAs cap layer was grown to facilitate the formation of good ohmic contacts. The $Ga_{0.51}In_{0.49}P$ insulator thickness t varies from t = 0, 50 ~ 100 nm, to examine how the insulator thickness affects the the

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devices microwave characteristics. Schematic diagram of the cross section of MISFET's (t = 50 nm-100nm) and MESFET's (t = 0 nm) is shown in Fig. 1.

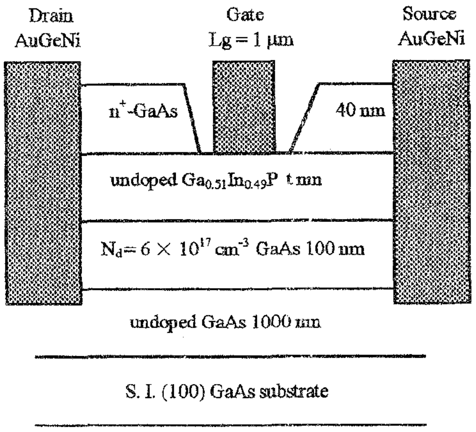

Fig. 1 Device cross section of $Ga_{0.51}In_{0.49}P/GaAs$ MISFET's (t = 50nm-100 nm) and MESFET's (t = 0 nm).

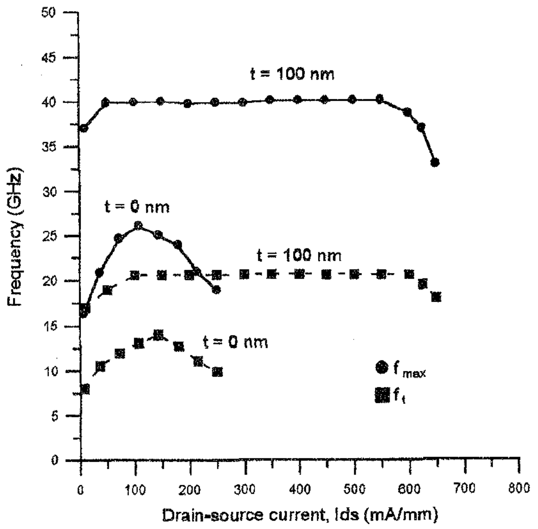

Fig. 2 Microwave characteristics of an airbridge gate MISFET's with insulator thickness t = 100 nm at V_{ds} = 4 V and V_{gs} = 0 V.

III. EXPERIMENTAL RESULTS AND DISCUSSIONS

Microwave on-wafer S-parameters for $Ga_{0.51}In_{0.49}P/GaAs$ MISFET's (t = 50 nm and 100 nm) and MESFET's (t = 0 nm) with 1.0 µm-long gate were measured in common-source configuration from 45 MHz to 40 GHz with an HP8510C network analyzer in conjunction with Cascade probes. Fig. 2 shows the f_{max}'s and f_t's as a function of I_{ds} for MISFET's with t = 100 nm and MESFET's biased at V_{ds} = 4V. As can be seen clearly, f_{max}'s and f_t's of MISFET's are much higher than that of the MESFET's. The flat region of f_{max}'s and f_t's of MISFET's are also much wider than that of the MESFET's. Table I is a summary of the results of f_t's, f_{max}'s and extracted C_g (i.e., $C_{gs}+C_{gd}$) from measured S parameters for all devices biased at V_{ds} =4V, with V_{gs} tuned for a maximum S_{21}. From this table one can find that f_t's and f_{max}'s are greatly improved for all MISFET's and MESFET's with airbridge gate structure compared with that of traditional gate structure. The airbridge gate MISFET's with t = 50 nm exhibited f_t = 20.5±0.3 GHz and f_{max} = 39±0.5 GHz. These valus were roughly 45 % and 49 % higher than those (f_t = 14.1±0.3 GHz and f_{max} = 26.1±0.3 GHz) of the airbridge gate MESFET's (t = 0 nm) but slightly lower than those (f_t = 20.7±0.4 GHz, f_{max} = 40.1 ± 0.5 GHz) of the airbridge gate MISFET's with t = 100 nm. However, the f_t's and f_{max}'s of traditional MISFET's with t = 50 nm were larger than that of traditional MISFET's with t = 100 nm. This can be explained by Fig. 3 and Fig. 4 in which the MISFET model of Ref. [3] was extended to include parasitic gate terminal capacitances C_g^p (i.e., interelectrode capacitance C_g^e plus geometric pad capacitance C_g^{pad}) in the totalcapacitance C_g. That is $C_g = C_g^i + C_g^e + C_g^{pad}$

	t = 0 nm		t = 50 nm		t = 100 nm	
	traditional	airbridged	traditional	airbridged	traditional	airbridged
f_t(GHz)	12.9 ± 0.2	14.1 ± 0.3	17.6 ± 0.2	20.5 ± 0.3	16.2 ± 0.2	20.7 ± 0.4
f_{max}(GHz)	24.6 ± 0.3	26.1 ± 0.3	34.9 ± 0.4	39 ± 0.5	32.8 ± 0.3	40.1 ± 0.5
C_g (fF)	244.1 ± 2	223.9 ± 1.7	139.5 ± 1.4	119.4 ± 1.3	94.1 ± 1	73.9 ± 0.8

Table I Summary of RF characteristics of $Ga_{0.51}In_{0.49}P/GaAs$ airbridge gate and traditional MISFET's (t = 50 nm and 100 nm) and MESFET's (t = 0 nm).

. The parameters used are as follows : surface state density N_{SS} = 6×10^{11} $cm^{-2}eV^{-1}$, electron mobility : 2000 cm^2/V-sec, saturation velocity 1.2 $\times 10^7$ cm/sec, parasitic resistances $R_s = 4.1\ \Omega$, $R_d = 4.05\ \Omega$, interelectrode capacitance $C_g^e = 11.25$ fF, geometric pad capacitance $C_g^{pad} = 19$ fF, $V_{gs} = 0$ V and $V_{ds} = 4$ V. As can be seen clearly from Fig. 3, at small t value (t < 50 nm), even though the transcondunctance g_m decreases monotonic with increasing insulator thickness, yet the reduced gate terminal capacitance C_g makes the ratio, g_m/C_g, higher with increasing insulator thickness. This means f_t's (~ $\frac{g_m}{2\pi C_g}$) will be improved with increasing thickness thickness for small t, as shown in Fig. 4. In theory of Ref. [3-4] only C_g^i is considered, and hence predicted that MISFET's will have slightly higher or nearly the same values of f_t's and f_{max}'s with increasing t even if t is up to 500 nm. But, in real case, C_g^p is a not omittable constant and must be considered in the calculation. The C_g^i decreases with increasing t and hence f_t's and f_{max}'s begin to decay when C_g^p is comparable to C_g^i. The simulated peak of f_t's of traditional structure appears earlier (50 nm) than airbridge gate structure (75 nm) due to the larger C_g^p. For airbridge gate MISFET's, the parasitic geometric pad capacitance C_g^{pad} is negligible and hence its total gate capacitance C_g is approximately equal to instead of $C_g^i + C_g^e$. This value of course is lower than that ($C_g = C_g^i + C_g^e + C_g^{pad}$) of traditional MISFET's as shown in Fig. 3. Therefore, airbridge gate MISFET's exhibit higher f_t's than traditional MISFET's as shown in Fig. 4. In addition, the channel resistance R_i reduce systematically with increasing insulator thickness. Output conductance G_d for MISFET's fabricated in our laboratory is nearly a constant and about 0.062 mS/mm. This implies the f_{max}'s (~ $\frac{f_t}{2\sqrt{G_d R_i}}$) will be improved more than f_t's with increasing insulator thickness at small t value, as shown in Fig. 4. The measured f_t's and f_{max}'s for airbridge gate and traditional MISFET's were also shown in Fig. 4 for

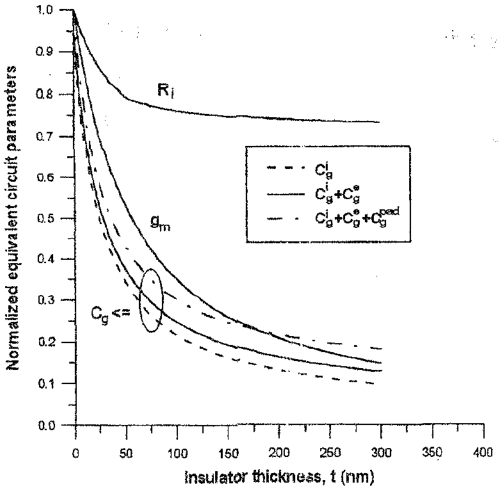

Fig.3 The simulated normalized depedance of the transconductance g_m, gate terminal capacitance C_g and channel resistance R_i versus insulator thickness t.

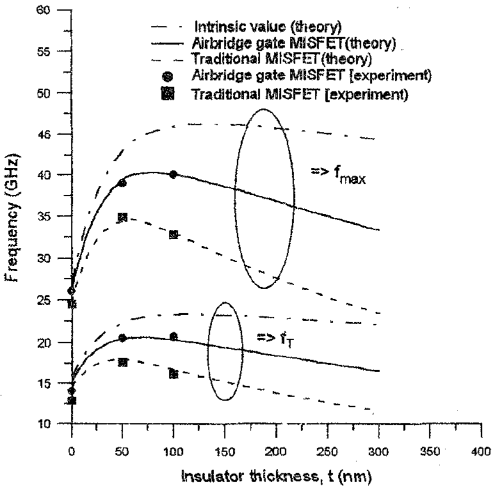

Fig.4 The simulated and measured cutoff frequency f_t's and maximum oscillation frequency f_{max}'s of airbridge gate and traditional MISFET's versus insulator thickness t.

comparison. For proper gate insulator, e.g. , 50 nm, $Ga_{0.51}In_{0.49}P$/GaAs airbridge gate and traditional MISFET's clearly show a performance advantage over a similar MESFET's (t = 0 nm). However, the microwave response (f_t's and f_{max}'s) of airbridge gate and traditional MISFET's with t = 100 nm are comparable to that of devices with t = 50 nm. This is consistent with the simulated data and demonstrate the validity of the simulation. So, we conclude that the state-of-the-art values of $Ga_{0.51}In_{0.49}P$ insulator thickness should be around 50 nm to 100 nm for 100 nm GaAs active layer.

IV. CONCLUSION

The effect of extrinsic capacitances on the microwave performance of $Ga_{0.51}In_{0.49}P$/GaAs traditional and airbridge gate MISFET's were evaluated by varying the thickness of the insulating layer. The f_{max}'s and f_t's of MISFET's using airbridge gate structure were higher than those of MISFET's using traditional gate structure due to the lower parasitic capacitances. The experimental results suggest that the optimized insulator thickness for 100 nm GaAs active layer is around 50 nm to 100 nm. Due to the $Ga_{0.51}In_{0.49}P$ airbridge gate structure, a high current drivability, high breakdown, high linearity, high speed, and low leakage gate current $Ga_{0.51}In_{0.49}P$/GaAs MISFET was achieved. These results showed that the $Ga_{0.51}In_{0.49}P$/GaAs airbridge gate MISFET's were very suitable for microwave high power device applications.

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