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Analysis and Design of CMOS Match-impedance Wide-band amplifiers

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The realization of matched impedance wide-band amplifiers fabricated by TSMC 0.35um CMOS process is reported. The technique of multiple-feedback loops was used to achieve terminal impedance matching and wide bandwidth. The experimental results showed that a small signal gain of 12.7dB and a 3-dB bandwidth of 1.7GHz with in-band input/output return loss less than 10dB were obtained The intrinsic over-damped characteristic of this amplifier was proved and source capacitive peaking was used to remedy this problem. The trade-off between the input impedance matching and bandwidth was also found.

1. INTRODUCTION

Wide-band amplifiers are used in variety of modern electronic systems such as microwave/lightwave communication and instrumentation [1]. Among the many versions of wide-band amplifiers, the so-called Kukielka configuration [2] is one of the popular circuits. It has been fabricated by silicon bipolar, AlGaAs/GaAs HBT and InAlAs/InGaAs HBT processes with excellent performance [3-5]. Recently, CMOS technology has attracted much attention because it is potentially a low cost process. However, no detailed account of the performance of the CMOS wide-band amplifiers with Kukielka configuration was reported in the literature. Therefore in this paper we present the first demonstration of Kukielka wide-band amplifiers using CMOS process. Multiple-feedback loops were used to achieve terminal impedance matching and wide bandwidth simultaneously. Capacitive peaking technique [6] was also used to overcome the intrinsic over-damped frequency response of the Kukielka amplifiers and thus enhance the bandwidth. The experimental results showed that a small signal gain of 12.7 dB and a 3-dB bandwidth of 1.7 GHz with in-band input return loss less than -10dB were achieved.

2. PRINCIPLE OF CIRCUIT DESIGN

The circuit topology of the transimpedance amplifier with multiple feedback loops is shown in Fig 1. The input stage consisting of a single transistor M_1 with local series feedback (R_{S1}) drives the output stage composed of a transistor with local shunt (R_{f2}) and local series feedback (R_{S2}). There is an overall shunt-series feedback loop composed of resistors R_{S2} and R_{f1}. Clearly this amplifier can be approximated by a two-pole system with open loop poles of ω_{p1} and ω_{p2}. Local series feedback resistor R_{S1} is used to adjust ω_{p1} while local shunt R_{f2} and series resistors R_{S2} are used to adjust ω_{p2} so that the two poles are brought to be coincident. Then the global feedback resistor R_{f2} is selected for a required loop gain to attain the maximally flat condition. However, since this amplifier tends to give over-damped characteristics [2], source peaking capacitors C_{S1} and C_{S2} [2,6] are connected in parallel with Rs1 and Rs2, respectively, to overcome this problem.

3. EXPERIMENTAL RESULTS

The schematic of the CMOS wide-band amplifier is shown in Fig 2(a). Compared to the

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circuit in Fig.1, the second stage of the circuit in Fig. 2(a) is replaced with the compound transistor, which has a resistive Darlington configuration consisting of M_{2a} and M_{2b}. The primary motive for use of the compound transistor is to achieve a higher gain-bandwidth product. Simulations were done by Hspice design tools.

The CMOS matched-impedance wide-band transimpedance amplifier was fabricated by 0.35μm process provided by TSMC (Taiwan Semiconductor Manufacturing Corporation). The die photograph of the finished circuit is shown Fig 2(a). Note that the circuit (excluding the patterns for testing) only occupies a very smaller area of 500μmx450μm because no inductor was used. HP8510 network analyzer in conjunction with the cascade probe station was used to measure the characteristics of this wideband amplifier. The measured and simulated results are shown in Figs. 3(a), 3(b) and 3(c) for $|S_{21}|$, noise figure, $|S_{11}|$, $|S_{22}|$, and linearity, respectively. The measured $|S_{21}|$ exhibited a flat response with a gain of 12.7dB, noise figure of 5.7dB, and a 3-dB bandwidth of 1.7GHz. The in band (from DC to 1.7GHz) input return losses $|S_{11}|$ were smaller than –10dB. From Fig.3(c), input 1-dB compression point of –11 dBm and the input IP_3 of – 4 dBm were obtained. These were quite high compared with the typical values of –20 dBm (input P_{1dB}) and –10 dBm (IIP_3) [7]. The results achieved indicate that this multiple feedback amplifier can offer high dynamic range and high linearity in addition to wide bandwidth.

4. CONCLUSION

The first CMOS wide-band amplifier with the Kukielka configuration was designed and fabricated. The experimental results showed that a small signal gain of 12.7 dB and a 3-dB bandwidth of 1.7 GHz were obtained. Input 1-dB compression point of –11 dBm and the input IP_3 of –4 dBm were also achieved. Wide bandwidth, high dynamic range and high linearity were attributed to the multiple feedback technique used.

Acknowledgements

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Rerences

[1] R. G. Meyer and R. A. Blauschild, "A 4-terminal wide-band monolithic amplifier, "*IEEE J. Solid-State Circuits,* vol.sc-16, pp.634-638, Dec. 1981.

[2] C. D. Hull and G. B. Meyer, "Principles of monolithic wideband feedback amplifier design, "*Int. J. High Speed Electronics*, vol.3, pp.53-93, Feb.1992.

[3] I. Kipnis, J. K. Kukielka, J. Wholey, and C. P. Snapp, "Silicon bipolar fixed and variable gain amplifier MMICs for microwave and lightwave applications up to 6 GHz, "*Microwave Symposium Digest, 1989, IEEE MTT-S International,* vol.1, pp.109-112, June. 1989.

[4] K. W. Kobayashi and A. K. Oki, "A DC-10 GHz high gain-low noise GaAs HBT direct-coupled amplifier, "*IEEE Microwave and Guided Wave Lett.*, vol.5, pp.308-310, Sept. 1995.

[5] K. W. Kobayashi, L. T. Tran, J. Cowls, T. R. Block, a. K. Oki , and D. C. Streit, "Low dc power high gain-bandwidth product InAlAs/InGaAs-InP HBT direct-coupled amplifiers, " proceeding of *IEEE GaAs IC Symp.*, pp.141-144, Nov. 1996.

[6] F.T. Chien and Y. J. Chan, "Bandwidth enhancement of transimpedance amplifier by a capacitive-peaking design, "*IEEE J. Solid-State Circuits*, vol.34, pp.1167-1170, Aug. 1999.

[7] B. Razavi, "RF Microelectronics," Prentice Hall, p.16, p.167, 1998.

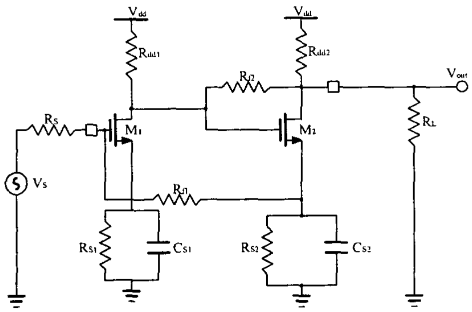
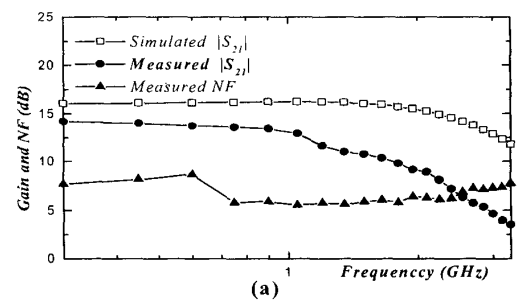
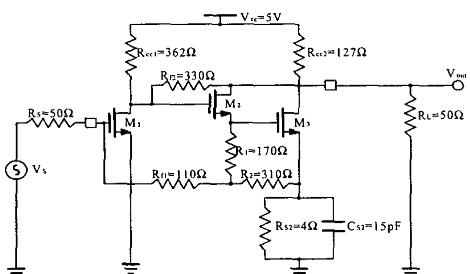


Fig. 1 The schematic of Kukielka circuit.



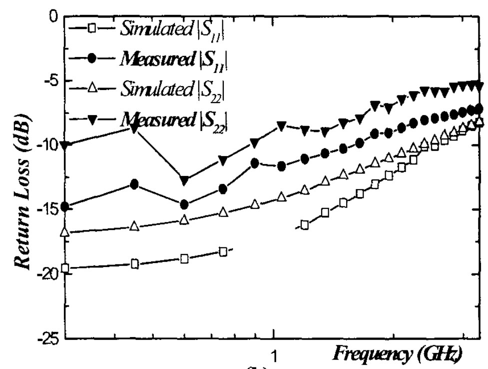
(a)

Fig. 3(a). Measured and simulated S21. The measured noise figure is also shown.



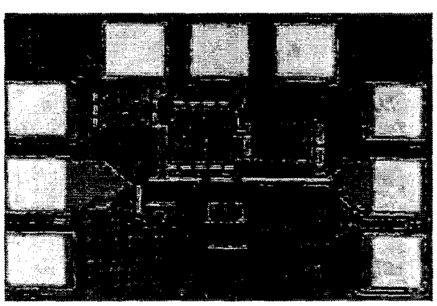
(a)

Fig. 2(a) The schematic of CMOS matched impedance wideband amplifier.



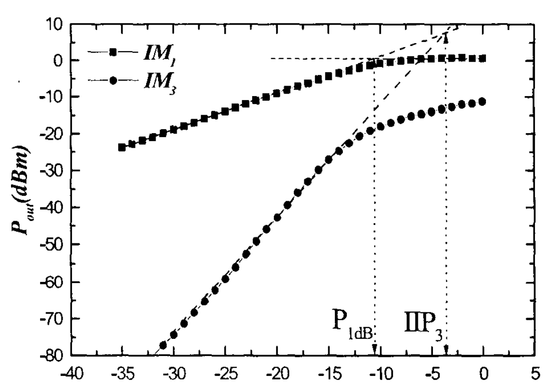
(b)

Fig. 3(b) The measured S11 and S22.



(b)

Fig.2(b) The die photograph of the finished CMOS matched impedance wideband amplifier



(c)

Fig. 3(c) Measured characteristics of the linearity of the CMOS matched impedance wideband amplifier.