# Square-rooting and vector summation circuits using current conveyors 

S.-I. Liu

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#### Abstract

New analogue squaring, square-rooting and vector summation circuits using current conveyors (CCIIs) are presented. They consist of MOS transistors biased in the triode region, a buffered unity-gain inverting amplifier, resistors and CCIIs. A general $n$-input vector summation circuit is also proposed. The proposed squaring, squarerooting circuits and a two-input vector summation circuit have been implemented using commercial CCIIs and transistor arrays. Its -3 dB bandwidth is measured to be about 400 kHz . The proposed circuits are expected to be useful in analogue signal-processing applications.


## 1 Introduction

Vector summation and root-mean-square (RMS) circuits have been found widely useful in instrumentation, communication, and neural computation [1-8]. For example, the computation of the Euclidean distance between two multidimensional vectors are needed in Fourier spectral analysis and most neural network applications [1,5,6]. There are various computing methods for vector summation and RMS functions in the literature [2]. Most of the methods for computing vector summation and RMS values perform the functions of squaring, averaging, and square rooting in a straightforward manner using multipliers and operational amplifiers (op-amps) [3]. The op-amp-based circuits will be limited by the finite gainbandwidth product of the op-amps. Most methods for realising vector summation and RMS functions required the translinear circuits of the bipolar transistors to realise the multiplication [2-4]. They could not be suitable for modern CMOS technologies.

Second-generation current conveyors (CCIIs) had been widely used to realise amplifiers, oscillators, immittances, rectifiers and filters [9-12]. CCIIs can provide not only constant bandwidth independent of closed-loop gain but also high slew-rate capability [10-13]. It will be beneficial to develop various analogue signal-processing circuits using CCIIs. The motivation of this paper is to develop new integrable squaring, square-rooting and vector summation circuits using CCIIs and MOS transistors. Experimental results are obtained to verify the theoretical analysis of the proposed techniques.

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The author is with the Department of Electrical Engineering, National Taiwan University, Taipei, Taiwan 10664, Republic of China

## 2 Circuit description

The characteristics of a CCII [9, 10], shown in Fig. 1, can be modelled as

$$
\left[\begin{array}{l}
V_{X}  \tag{1}\\
I_{Y} \\
I_{Z}
\end{array}\right]=\left[\begin{array}{rrr}
1 & 0 & 0 \\
0 & 0 & 0 \\
0 & 0 & \pm 1
\end{array}\right]\left[\begin{array}{l}
V_{Y} \\
V_{Z} \\
I_{X}
\end{array}\right]
$$



Fig. 1 Circuit symbol for CCII
where the positive and negative signs denote the noninverting CCII (CCII + ) and inverting CCII (CCII-), respectively. The proposed square-rooting circuit is shown in Fig. 2. It consists of a CCII + , two NMOS transistors biased in the triode region (with the substrate connected to the most negative voltage) [7, 14, 15], a resistor $R_{1}$ and a buffered unity-gain inverting amplifier. The drain current of an NMOS transistor in the triode region can be given by [14]


Fig. 2 Proposed square-rooting circuit

$$
\begin{equation*}
I_{D}=K \frac{W}{L}\left[\left(V_{G S}-V_{T}\right) V_{D S}-\frac{V_{D S}^{2}}{2}\right] \tag{2}
\end{equation*}
$$

where $K$ is the transconductance parameter and $V_{T}$ is the threshold voltage. $V_{G S}$ and $V_{D S}$ are the gate-to-source and drain-to-source voltages, respectively. Assume the matched transistors $M_{1}$ and $M_{2}$ in Fig. 2 have the same aspect ratio $\left(=W_{1} / L_{1}\right)$. Since the high-impedance terminal $Y$ of the CCII in Fig. 2 is grounded, the voltage $V_{X}$ will follow the voltage $V_{Y}(=0)$ according to eqn. 1. The transistors $M_{1}$ and $M_{2}$ will have equal source voltage. Thus their threshold voltages will be equal, even if their sub-

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strate is connected to the most negative voltage. Now examine the currents $I_{X}$ and $I_{Z}$ in Fig. 2. A routine circuit analysis yields

$$
\begin{align*}
& I_{X}=\frac{V_{i n}}{R_{1}}+K \frac{W_{1}}{L_{1}}\left[\left(V_{G}-V_{T}\right)\left(-V_{o}\right)-\frac{\left(-V_{o}\right)^{2}}{2}\right]  \tag{3}\\
& I_{Z}=-K \frac{W_{1}}{L_{1}}\left[\left(V_{G}-V_{T}\right) V_{o}-\frac{V_{o}^{2}}{2}\right] \tag{4}
\end{align*}
$$

Since $I_{X}=I_{Z}$, the output voltage $V_{o}$ of this squarerooting circuit can be obtained from eqns. 3 and 4 as

$$
\begin{equation*}
V_{o}=-\left(\frac{V_{i n}}{R_{1} K \frac{W_{1}}{L_{1}}}\right)^{1 / 2} \quad \text { for } V_{i n}>0 \tag{5}
\end{equation*}
$$

For proper operation, the following condition should be satisfied

$$
\begin{equation*}
V_{G}>\left|V_{o}\right|+V_{T} \tag{6}
\end{equation*}
$$

A squaring circuit, shown in Fig. 3, can be realised by using similar techniques [15]. Assume the matched transistors $M_{3}$ and $M_{4}$ in Fig. 3 have the same aspect ratio


Fig. 3 Proposed squaring circuit
( $=W_{3} / L_{3}$ ). According to eqn. 2, the current $I_{x}$ in Fig. 3 can be expressed as

$$
\begin{equation*}
I_{X}=-K \frac{W_{3}}{L_{3}} V_{1}^{2} \tag{7}
\end{equation*}
$$

Since $I_{X}=I_{Z}$ for a CCII, the output current of this squaring circuit can be given as

$$
\begin{equation*}
I_{o}=K \frac{W_{3}}{L_{3}} V_{\mathrm{L}}^{2} \tag{8}
\end{equation*}
$$

In general, Fig. 3 is expandable to accommodate more input variables as shown in Fig. 4. The current $I_{o}$ of Fig. 4 can be obtained as

$$
\begin{equation*}
I_{o}=K \frac{W_{3}}{L_{3}}\left(V_{1}^{2}+V_{2}^{2}+\cdots+V_{n}^{2}\right) \tag{9}
\end{equation*}
$$

where $V_{i}$ (for $i=1,2, \ldots, n$ ) is an input variable. One can combine these circuits to realise the vector summation circuit shown in Fig. 4. Its output voltage can be given as

$$
\begin{equation*}
V_{o}=-\left(\frac{R_{2} \frac{W_{3}}{L_{3}}}{R_{1} \frac{W_{1}}{L_{1}}}\left(V_{1}^{2}+V_{2}^{2}+\cdots+V_{n}^{2}\right)\right)^{1 / 2} \tag{10}
\end{equation*}
$$

In fact, one can directly connect the output current $I_{0}$ of the squaring circuit (Fig. 3) to the low-impedance node $V_{X}$ of the CCII + in Fig. 2 without the resistors $\mathbf{R}_{2}$ and $\mathbf{R}_{1}$. Then a fully integrable vector summation circuit can be realised. However, there is a finite output resistance at the terminal $X$ of a commercial CCII, so Fig. 4 is used experimentally. Moreover, Fig. 4 can also be used to realise an RMS circuit by inserting a simple RC lowpass filter between the squaring and square-rooting circuits.


Fig. 4 Proposed vector summation circuit with $n$ inputs

## 3 Performance analysis and experimental results

The nonideal characteristics of a nonideal CCII and a buffered unity-gain inverting amplifier (in Fig. 2) can be modelled as

$$
\begin{equation*}
I_{Z}=\alpha I_{X}, V_{X}=\beta V_{Y} \quad \text { and } \quad V^{\prime}=-\gamma V_{o} \tag{11}
\end{equation*}
$$

where $\alpha=1-\varepsilon_{1}$ and $\varepsilon_{1}\left(\varepsilon_{1} \ll 1\right)$ and $\beta=1-\varepsilon_{2}$ and $\varepsilon_{2}$ $\left(\varepsilon_{2} \ll 1\right)$ denote the current tracking error and voltage tracking error of a CCII, respectively, and $\gamma=1-\varepsilon_{3}$ and $\varepsilon_{3}\left(\varepsilon_{3} \ll 1\right)$ denotes the voltage tracking error of a buffered unity-gain inverting amplifier. The effect of the voltage tracking error $\varepsilon_{2}$ of a CCII can be neglected, since $V_{Y}=0$ in Fig. 2. A detailed analysis for the transfer function of the square-rooting circuit in Fig. 2 yields

$$
\begin{align*}
& V_{o}= \\
& \\
& \qquad \begin{array}{l}
(1-\alpha \gamma)\left(V_{G}-V_{T}\right) \\
\quad-\sqrt{\left[(1-\alpha \gamma)^{2}\left(V_{G}-V_{T}\right)^{2}+2 \alpha\left(1+\alpha \gamma^{2}\right) \frac{V_{i n}}{R_{1} K} \frac{L_{1}}{W_{1}}\right]}
\end{array}
\end{align*}
$$

If $\alpha=\gamma=1$, eqn. 12 will be the same as eqn. 5 . Hence, the nonideal effects of the CCIIs and the buffered unitygain inverting amplifier will contribute to the gain errors and offset voltages of the output voltage of the squarerooting circuit. The nonideal CCII + will also affect the squaring circuit in Fig. 3. However, it will only contribute to the gain of the output, so the effect is not analysed here.

Assume that the aspect ratios of $\mathbf{M}_{1}$ and $\mathbf{M}_{2}$ in Fig. 2 are

$$
\frac{W_{1}}{L_{1}}\left(=\frac{W}{L}+\Delta \frac{W}{L}\right) \text { and } \frac{W_{2}}{L_{2}}\left(=\frac{W}{L}-\Delta \frac{W}{L}\right)
$$

respectively. The output voltage of the square-rooting
circuit can be rewritten as

$$
\begin{align*}
V_{o}= & \frac{\Delta \frac{W}{L}}{\frac{W}{L}}\left(V_{G}-V_{T}\right) \\
& -\left[\left(\frac{\Delta \frac{W}{L}}{\frac{W}{L}}\right)^{2}\left(V_{G}-V_{T}\right)^{2}+\frac{L V_{i n}}{K W R_{1}}\right]^{1 / 2} \tag{13}
\end{align*}
$$

The effect of the transistor mismatches on the squarerooting ciruit can be improved by using larger aspect ratios.

To verify the proposed circuits, they have been implemented by using commercial CCIIs (AD844) sand CMOS transistor arrays (CD4007). The power supply is $\pm 6 \mathrm{~V}$ and $V_{G}=6 \mathrm{~V}$. The experimental results are summarised as follows. The buffered unity-gain inverting amplifier was realised using the op-amps (LF356) and two $10 \mathrm{k} \Omega$ resistors. The DC transfer functions of the proposed square-rooting circuit were measured and shown in Fig. 5. A triangular signal $V_{\text {in }}$ of 40 kHz was also applied to


Fig. $5 D C$ transfer functions ( $V_{o}$ against $V_{i n}$ ) of proposed squarerooting circuit with $V_{G}=6 \mathrm{~V}$

- $R_{1}=600 \Omega$
$R_{1}=1200 \Omega$
$R_{1}=2400 \Omega$

Fig. 2 with $R_{1}=120 \Omega$ and the output signal $V_{o}$ of the square-rooting circuit was measured in Fig. 6. Its -3 dB bandwidth was measured to be about 400 kHz . The bandwidth limitation of the proposed square-rooting circuit is mainly owing to the op-amps (LF356) and the poor high-frequency property of the discrete MOS transistor arrays.

A sinusoidal signal of 40 kHz was applied to the squaring circuit in Fig. 3. The output voltage was measured with $R_{2}(=1 \mathrm{k} \Omega)$ and is shown in Fig. 7. Finally, the results of the vector sum circuit in Fig. 4 are presented. To cancel the DC offset voltage caused by the nonmatched NMOS transistors, a large-valued variable resistor $R_{\text {off }}(=1 \mathrm{M} \Omega$ ) was added. The upper waveform in Fig. 8 shows the vector summation outut ( $1 \mathrm{~V} / \mathrm{div}$ ) of two synchronised triangular signals of 10 and 20 kHz
(1 V/div) with $R_{1}(=1.9 \mathrm{k} \Omega)$ and $R_{2}(=6 \mathrm{k} \Omega)$. As the input goes through zero, the output appears as a V shape. The -3 dB bandwidth was measured about 400 kHz for two input signals.


Fig. 6 Square-rooting circuit measurements
a Triangular signal of $V_{\text {in }}$
$b$ Output voltage $-V_{s}$


Fig. 7 Square circuit measurements
a Sinusoidal signal of $V_{i}$
b Output voltage $V_{\text {out }}$


Fig. 8 Two-input vector summation circuit measurements
a Input triangular signals of 10 and 20 kHz
$b$ Output voltage $V_{d}$

## 4 Conclusions

New analogue squaring, square-rooting and vector sum circuits using CCIIs have been proposed. Experimental results have been given to verify the theoretical analysis of the proposed circuits including the square and squarerooting circuits. A two-input vector summation circuit was also built and tested. Its -3 dB bandwidth was about 400 kHz . The proposed circuits will be useful in analogue signal processing applications.

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