Frequency doubling and rectification are performed by employing the dual translinear characteristic associated within the current conveyor, where this characteristic has been monitored from the supply-line currents. PSPICE simulation results confirm the performance of the proposed circuit.

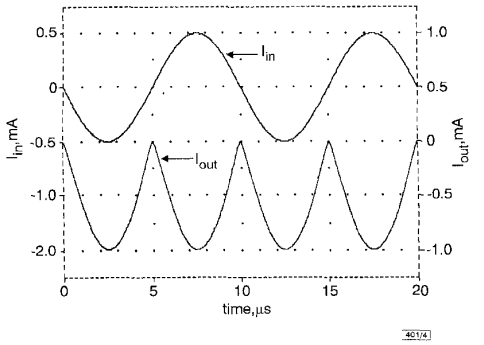

Fig. 4 *Full-wave rectifier simulation response*

Upper trace input: 1mA p-p
Lower trace output: 1mA p-p

Acknowledgments: The authors would like to acknowledge the financial support of this work by grants from the National Science and Technology Development Agency (NSTDA), Thailand and from the National Electronics and Computer Technology Center (NECTEC), Thailand.

27 August 1998
Electronics Letters Online No: 19981456

W. Surakampontorn, K. Anuntahirunrat and V. Riewruja (*The Faculty of Engineering, King Mongkut's Institute of Technology Ladkrabang, Bangkok 10520, Thailand*)

References

1 FABRE, A., DAYOUB, F., DURUISSEAU, L., and KAMOUN, M.: 'High input impedance insensitive second-order filters implemented from current conveyors', *IEEE Trans. Circuits Syst. I*, 1994, **41**, (12), pp. 918–921

2 FABRE, A., SAAID, O., WEIST, F., and BOUCHERON, C.: 'High frequency applications based on a new current controlled conveyor', *IEEE Trans. Circuits Syst. I*, 1996, **43**, (2), pp. 82–91

3 KIRANON, W., KESORN, J., and WARDKEIN, P.: 'Current controlled oscillators based on translinear conveyors', *Electron. Lett.*, 1996, **32**, (15), pp. 1330–1331

4 ABUELMA'ATTI, M.T., and AL-QAHTANI, M.A.: 'A current-mode current-controlled-coveyor-based analogue multiplier/divider', *Int. J. Electron.*, 1998, **85**, (1), pp. 71–77

5 SURAKAMPONTORN, W., JUTAVIRIYA, S., and APAJINDA, T.: 'Dual translinear sinusoidal frequency doubler and full-wave rectifier', *Int. J. Electron.*, 1988, **65**, (6), pp. 1203–1208

6 TOMAZOU, C., and LIDGEY, F.J.: 'Wide-band precision rectification', *IEE Proc. G*, 1987, **137**, (1), pp. 63–77

7 SURAKAMPONTORN, W.: 'Sinusoidal frequency doublers using operational amplifiers', *IEEE Trans.*, 1988, **IM-37**, (2), pp. 259–262

Weak inversion four-quadrant multiplier and two-quadrant divider

Cheng-Chieh Chang and Shen-Iuan Liu

A four-quadrant multiplier and a two-quadrant divider are presented. The proposed circuits are implemented by MOSFETs operating in weak inversion and are therefore suitable for low voltage and low power applications. Their performances were confirmed by HSPICE simulation using a 0.8μm CMOS process. The multiplier can operate under a ±0.75V supply voltage and its linear input range is ~0.125μA with error < 2%. The input range of the divider is 0.5 – 2μA and the error is < 3% for divider current < 60nA.

Introduction: Low power consumption techniques have become more and more important in modern VLSI technologies. To realise low power circuits, one promising solutions is to use MOSFETs which operate in weak inversion. Because of the exponential law of MOSFETs in weak inversion, it is easy to implement the various current-mode circuits, such as one-quadrant multiplier/dividers and square-rooting circuits, etc. [1 – 4]. Moreover, several interesting analogue signal processing circuits using MOSFETs in weak inversion have also been developed [1 – 6]. In this Letter, we propose a circuit which can provide four-quadrant multiplication and two-quadrant division. Simulation results are given to verify the theoretical analysis.

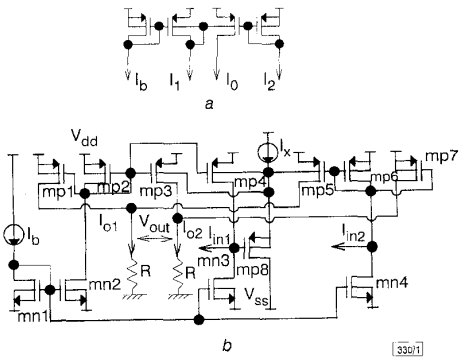

Fig. 1 *Conventional one-quadrant multiplier/divider and proposed four-quadrant multiplier and two-quadrant divider*

a Conventional one-quadrant multiplier/divider
b Proposed four-quadrant multiplier and two-quadrant divider

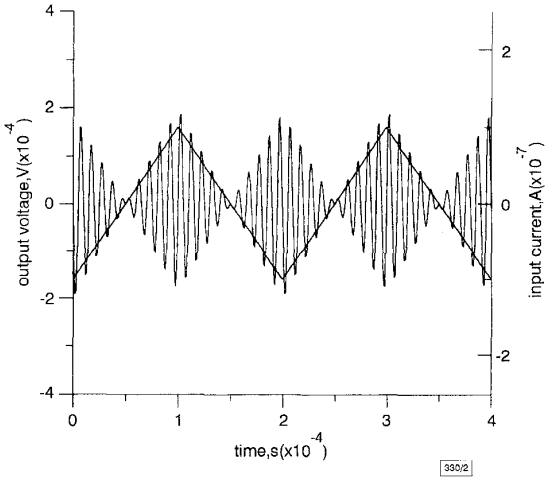

Fig. 2 *Typical time-domain response of proposed multiplier*

Circuit description: The conventional one-quadrant multiplier/divider is shown in Fig. 1*a*. The drain current for a PMOS transistor in weak inversion is given by [1 – 6]

$$I_D = I_{Do} \exp\left(\frac{V_{SG} + (n-1)V_{SB}}{nU_T}\right) \quad (1)$$

where I_{Do} is the leakage current, n is the slope factor and U_T (=kT/q) is the thermal voltage. Assume that all the transistors in Fig. 1*a* operate in weak inversion. According to eqn. 1, the relation

$$I_o I_b = I_1 I_2 \quad (2)$$

can be obtained where currents I_o, I_b, I_1 and I_2 must be positive.

Fig. 1*b* shows the proposed multiplier and divider. The core elements are transistors mp2, mp4, mp5 and mp6. Transistors mp1, mp3 and mp7 duplicate the currents of mp2, mp4 and mp6, respectively, to be I_b, $I_{in1} + I_b$ and $I_{in2} + I_b$. Both I_{in1} and I_{in2} can be positive or negative (if $|I_{in1}|$, $|I_{in2}| < I_b$). The current I_{o1} in Fig. 1*b* can be expressed as

$$I_{o1} = I_{mp1} + I_{mp5} = I_b + (I_{in1} + I_b)(I_{in2} + I_b)/I_b \quad (3)$$

and the current I_{o2} can be given by

$$I_{o2} = I_{mp3} + I_{mp7} = I_{mp4} + I_{mp6} = (I_b + I_{in1}) + (I_{in2} + I_b) \quad (4)$$

Thus the difference between I_{o1} and I_{o2} can be obtained with

$$I_{o1} - I_{o2} = I_{in1} I_{in2} / I_b \quad (5)$$

Multiplication and division can be achieved by subtracting I_{o2} from I_{o1}. The output voltage V_{out} can be defined as

$$V_{out} = R(I_{o1} - I_{o2}) = R I_{in1} I_{in2} / I_b \quad (6)$$

where the resistors R are shown in Fig. 1*b*. Current source I_X and mp8 are used to bias the back gates of mp3, mp4 and mp5 [3, 5, 6]. For multiplier operation, I_b is constant and I_{in1} and I_{in2} are the input signals. For divider operation, I_b is the positive input signal and I_{in1} (or I_{in2}) is another input signal.

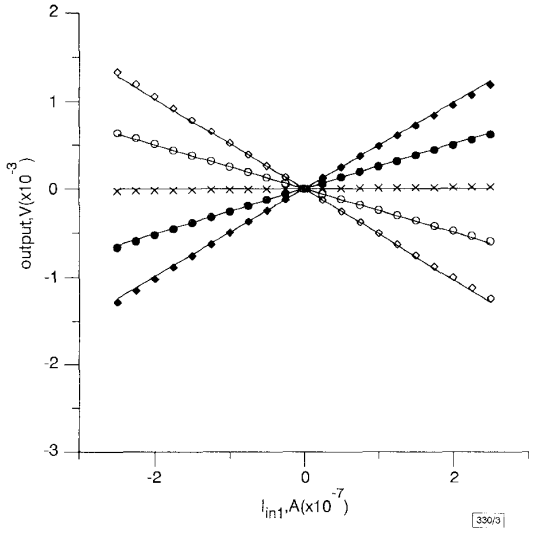

Fig. 3 *Simulated DC transfer functions for proposed multiplier*

$I_b = I_X = 2\mu A$
◆ $I_{in2} = 0.25\mu A$
● $I_{in2} = 0.125\mu A$
× $I_{in2} = 0\mu A$
○ $I_{in2} = -0.125\mu A$
◇ $I_{in2} = -0.25\mu A$
— ideal curve

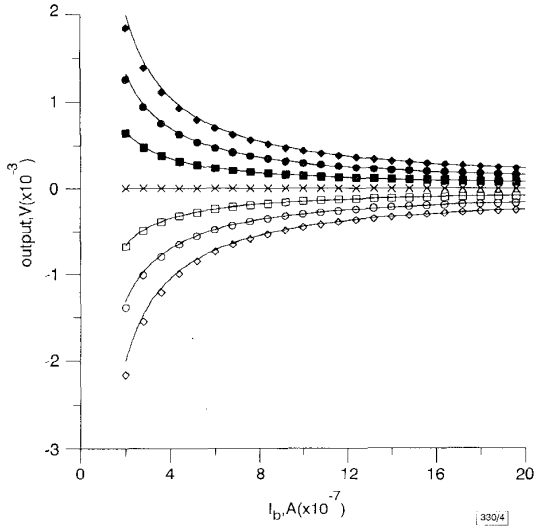

Fig. 4 *Simulated DC transfer functions for proposed divider*

$I_X = 2\mu A$, $I_{in1} = 0.2\mu A$
◆ $I_{in2} = 0.06\mu A$
● $I_{in2} = 0.04\mu A$
■ $I_{in2} = 0.02\mu A$
× $I_{in2} = 0\mu A$
□ $I_{in2} = -0.02\mu A$
○ $I_{in2} = -0.04\mu A$
◇ $I_{in2} = -0.06\mu A$
— ideal curve

Simulation results: The operation of the four-quadrant multiplier and two-quadrant divider in Fig. 1*b* is verified by HSPICE simulation using a 0.8μm CMOS process. The aspect ratios of the NMOS transistors are 1μm/5μm, and those of the PMOS transistors are 5μm/1μm. The power supply is ±0.75V and the output resistors R are 100kΩ. Figs. 2 and 3 are the transient and DC responses of the multiplier, respectively, where both the currents I_b and I_X are 2μA. In Fig. 2, I_{in1} is a 5kHz triangular wave of 0.1μA and I_{in2} is a 100kHz sinusoidal wave of 0.1μA. In Fig. 3, the error is < 2% if both input currents are < 0.125μA.

The simulation results for the divider are described as follows. Current I_b is the divisor and current I_{in1} (or I_{in2}) is the dividend. The DC transfer curves of the divider are shown in Fig. 4. Current I_X is 2μA and current I_{in1} is 0.2μA. The linear input range of I_b is between 0.5 and 2μA with an error of < 3% for I_{in2} < 60nA.

Conclusions: A four-quadrant multiplier and a two-quadrant divider which use transistors in weak inversion have been presented. The operation of the circuits has been confirmed by HSPICE simulation. The proposed circuits will be useful in the realisation of current-mode circuits such as modulators and demodulators.

Acknowledgments: The authors would like to thank the National Science Council, Taiwan, ROC, for financial support. This work was sponsored by NSC-87-2218-E-002-016.

25 August 1998
Electronics Letters Online No: 19981496

Cheng-Chieh Chang and Shen-Iuan Liu (*Department of Electrical Engineering, National Taiwan University, Taipei, Taiwan 10664, Republic of China*)

E-mail: lsi@cc.ee.ntu.edu.tw

References

1 VAN DER GEVEL, M., and KUENEN, J.C.: '$\sqrt{x}$ circuit based on a novel, back-gate-using multiplier', *Electron. Lett.*, 1994, **30**, pp. 183–184
2 VAN DER GEVEL, M., and KUENEN, J.C.: 'Simple low-voltage weak inversion MOS $1/x$ circuit', *Electron. Lett.*, 1994, **30**, pp. 1639–1640
3 MULDER, J., VAN DER WOERD, A.C., SERDIJN, W.A., and VAN ROERMUND, A.H.M.: 'Application of the back gate in MOS weak inversion translinear circuits', *IEEE Trans.*, 1995, **CASI-42**, pp. 958–962
4 ISMAIL, M., and FIEZ, T. (Eds): 'Analog VLSI signal and information processing' (McGraw-Hill, 1994), pp.384–393
5 FRIED, R., and ENZ, C.C.: 'Bulk driven MOST transconductor with extended linear range', *Electron. Lett.*, 1996, **32**, pp. 638–640
6 FRIED, R., and ENZ, C.C.: 'CMOS parametric current amplifier', *Electron. Lett.*, 1996, **32**, pp. 1249–1250

Application of genetic algorithm to sample balance analysis of nonlinear circuits

S. Iezekiel and A. Feresidis

A genetic algorithm has been applied, for the first time, to the sample balance method for nonlinear circuit analysis. Results for a circuit containing an ideal diode show this to be a viable approach which does not suffer from the limitations of other techniques for solving sample balance and harmonic balance equations. The algorithm does not require a good initial estimate nor does it need a Jacobian formulation of the circuit equations.

Introduction: Hybrid methods for the analysis of nonlinear microwave circuits, in which the linear elements are analysed in the frequency-domain while the nonlinearities are handled in the time-domain, have proved to be popular [1]. The harmonic balance method, in particular, has been extensively developed [2], with sample balance receiving less attention [3]. The difference between the two methods lies in the interface between the frequency- and time-domains. Harmonic balance relies on the use of Fourier transform (FT) techniques, while sample balance uses convolution. However, both methods are fundamentally similar in that a system