Device-Level Transient Analysis of a $1\mu m$ Six-Transistor BiCMOS Inverter Circuit Using a Large-Scale Quasi-3D Device Simulator

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Abstract

This paper presents a device-level study on the transient behavior of a $1\mu m$ Six-Transistor BiCMOS inverter circuit using a large-scale quasi-3D device simulator, which is derived from PISCES-2B [1], where layout information of each transistor and an efficient large-scale simulation capability have been added. According to simulation results, the speed performance of the BiCMOS inverter is determined by the charge transport in the base of the pull-up bipolar device, which is controlled by the circuit operating conditions set by the associated NMOS and PMOS devices.

Summary

Currently, the circuit performance associated with a new BiCMOS technology can be simulated based on models with parameters extracted from the device characteristics. For submicron BiCMOS devices, models with extracted parameters are not sufficient for analyzing circuit performance accurately. In addition, this intermediate model-extraction step is the main barrier for direct analysis of a new BiCMOS device structure in terms of its final circuit performance. For efficient device engineering, this is a need to quickly assess the merits of a new BiCMOS device structure in terms of specific circuit performance without this intermediate step. Currently, MEDUSA[2], CODECS[3], and other simulator [4] have shown device/circuit mixed-mode simulation capability. However, the outer-loop iteration method used in those simulators for circuit transient analysis may have difficulties in convergence. In this paper, an efficient large-scale quasi-3D device simulator, which can be used to evaluate transient of a six-transistor BiCMOS inverter circuit, is described.

By modifying the boundary conditions used in the PISCES-2B program, the quasi-3D simulation capability has been built with the width of each device individually programmable. As shown in Fig. 1, the equivalent quasi-3D boundary condition is:

$$\frac{V_{app}-\phi}{R}+C\frac{d}{dt}(V_{app}-\phi)-\sum_{i=1}^{N_b}W_i(J_n+J_p+J_{disp})_i=0$$

where V_{app} is the applied voltage. N_b is the number of grids associated with the electrode. W_i is the width of the boundary. In addition, the grid limit has been increased to 5000 for large-scale transient analysis using the Full Newton method to ensure convergence. Fig. 2(a) shows the device cross section of a BiCMOS inverter circuit based on a $0.8\mu m$ BiCMOS technology[5] used in the study. The NMOS and PMOS devices have an effective channel length of $0.9\mu m$, and a gate oxide thickness of $250\mathring{A}$ and threshold voltages of $0.8V$ and $-0.8V$, respectively. Fig. 2(b) shows the vertical doping profile in the intrinsic and the extrinsic base regions. The intrinsic base has a width of $0.1\mu m$ and a peak concentration of $1\times10^{18}cm^{-3}$. In order to meet the grid limit, NMOS, PMOS and bipolar devices are placed against one another separated by oxide layers. The bases of the two bipolar devices and the source/drain terminals are wired together with parasitic capacitances of $0.1fF$ and a capacitive load is $0.1pF$ at the output. All $1\mu m$-wide MOS transistors except the PMOS device have been used in the BiCMOS inverter circuit. As for the PMOS device, four channel widths ($1\mu m-1P1N, 2\mu m-2P1N, 3\mu m-3P1N, 4\mu m-4P1N$) have been included in the BiCMOS transient study.

By imposing a voltage pulse between 0V and 5V with rise and fall times of 10ps at the input, the pull-up and pull-down transient behavior of the BiCMOS inverter has been obtained. Each transient analysis took about 40 hours on a 28 MIPs computer with 48Mbytes memory. Compared to the previous data [6][7], the transient analysis of the BiCMOS inverter, which requires 3200 grids, is very efficient. Figs. 3 show base voltages of two bipolar devices during transient for the four cases. After the ramp-up period, the BiNMOS transistor and the N2 transistor turn on and the base voltage of the BiPMOS device slews downward toward 0V and the base voltage of the BiNMOS device goes upward. After the input ramp-up period, the 1P1N case shows the fastest decay in the base voltage of the BiPMOS device owing to the smallest parasitic capacitance at the BiPMOS base node. During the pull-up transient after $1ns$, the 4P1N case indicates the quickest turn-on of the BiPMOS device. However, the turn-on speed of the 4P1N case is not proportional to the width of PMOS device. Fig. 4 shows the output voltage of the BiCMOS inverters for the four cases during transient. Among four cases, case 4P1N has the shortest rise time owing to the largest width in PMOS, but its fall time is the longest. Fig. 5 shows the base currents of the BiPMOS device for four cases. During the pull-down transient, after the input ramp-up period, the negative base current implies removal of charge from the BiPMOS area. In the pull-up period, the 4P1N case shows the most drastic change in the base current, which is correlated to the fastest charge build-up and removal process in the base of the BiPMOS device. As shown in Figs. 6, four cases indicate a similar collector current in the pull-down bipolar device. However, during the pull-up transient, the 4P1N case has the largest peak in the

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emitter current of the pull-up bipolar device. Fig. 7 shows the electron concentration contours in the BiPMOS bipolar transistor at the peak of the emitter current. A wider base pushout phenomenon in the lateral base direction can be observed in the cases using wider PMOS devices. Fig. 8 shows the total electrons in the pull-up bipolar device during transient. During turn-on of the BiPMOS bipolar device, the 4P1N case does have the highest peak in total electrons, which is strongly correlated to the fastest turn-on. Fig. 9 shows the the normalized rise/fall time vs. the the width of the PMOS device. As a wider PMOS device is used, the improvement in the rise time is becoming smaller, which can be explained using the following time constant expression for the output waveform during the pullup transient.

$$t_{rc} = (\frac{1}{R_d C_{l2}} + \frac{q_b}{\beta \tau_f} + \frac{C_p}{\tau_f C_{l2}})^{-1}$$

where R_d is the equivalent resistance accounting for the sum of the PMOS channel resistance and the BJT base resistance. C_p is the equivalent capacitance at the BiPMOS base node accounting for the sum of the parasitic capacitances at the PMOS drain and BJT base nodes. C_{l2} is the equivalent capacitance accounting for the sum of the total capacitance at the output node and C_p. β is the current gain and τ_f is the electron forward base transit time. q_b is the normalized majority base charge accounting for high injection and Early effects. As shown in the above equation, the rise time is determined by the BJT-related parameters (τ_f, β, q_b) and the MOS-related parameters — R_d, C_{l2}. As a wider PMOS device is used in the BiCMOS inverter, although R_d can be reduced as a result of a reduction in the PMOS channel resistance, C_{l2} also increases owing to more parasitics from the PMOS drain area. Consequently, the decrease in the rise time using a wider PMOS device in the BiCMOS inverter is not proportional to the width of the PMOS device. On the other hand, as shown in Fig. 8, a wider PMOS device used in a BiCMOS inverter also worsens the fall time owing to the more parasitic capacitance effects.

In conclusion, an efficient large-scale quasi-3D device simulator has been created to analyze a six-transistor BiCMOS inverter circuit. According to simulation results, the speed performance of the BiCMOS inverter is determined by the charge transport of the BiPMOS device.

Acknowledgments

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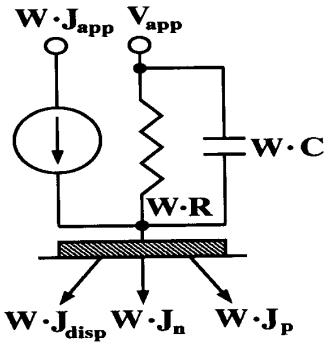


Fig. 1 Boundary condition of an electrode used in the quasi-3D device simulator.

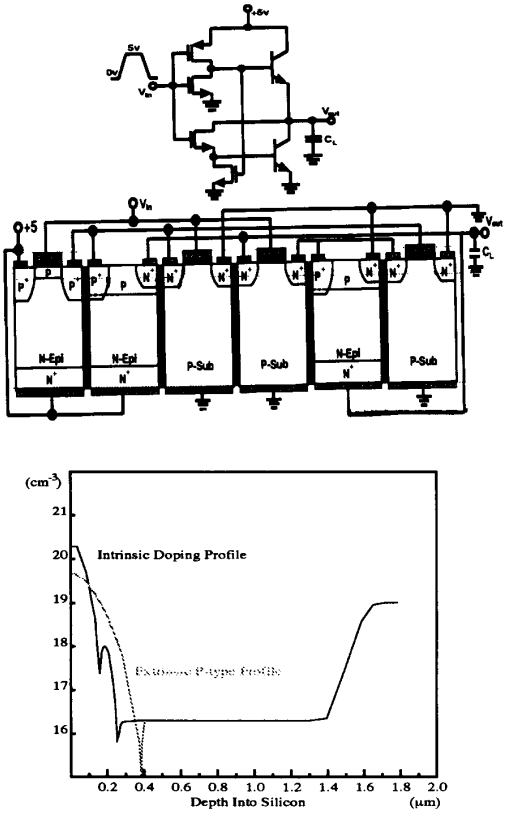
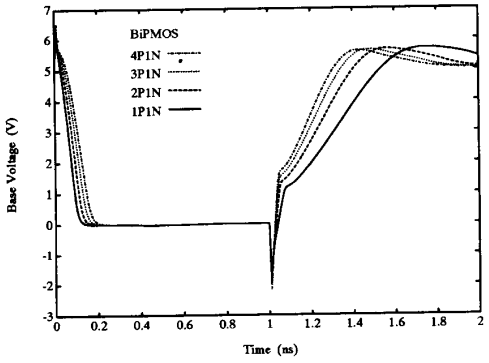


Fig. 2 (a) The six-transistor BiCMOS inverter circuit. (a) The BiCMOS device structure under study. (b) Vertical doping profiles in the intrinsic and the extrinsic base areas.



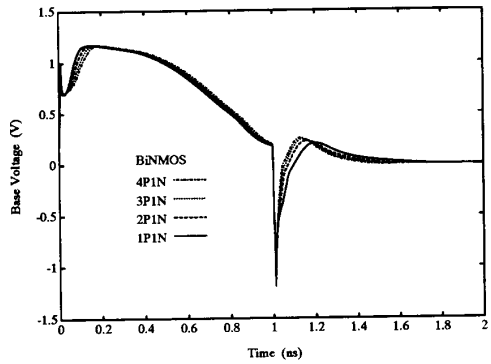


Fig. 3(a)&(b) The base voltages of the BiPMOS and BiNMOS devices during the transient for three cases.

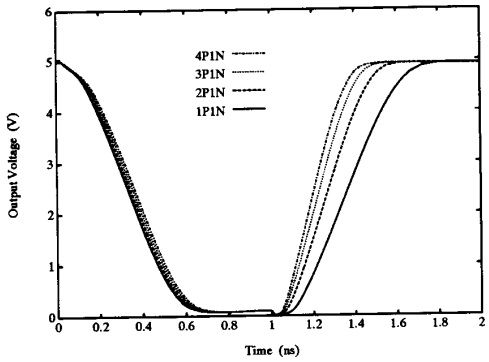


Fig. 4 The output voltages of the BiCMOS with output load of $0.1pf$ during the transient for three cases.

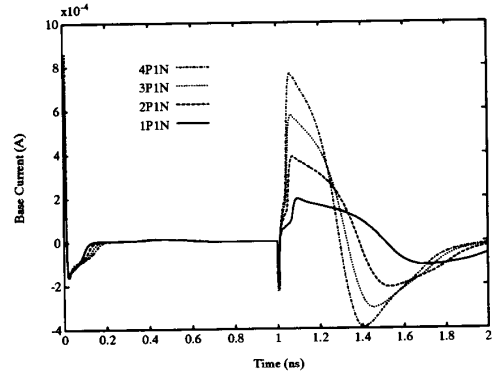


Fig. 5 The base currents of the BiPMOS device during the transient.

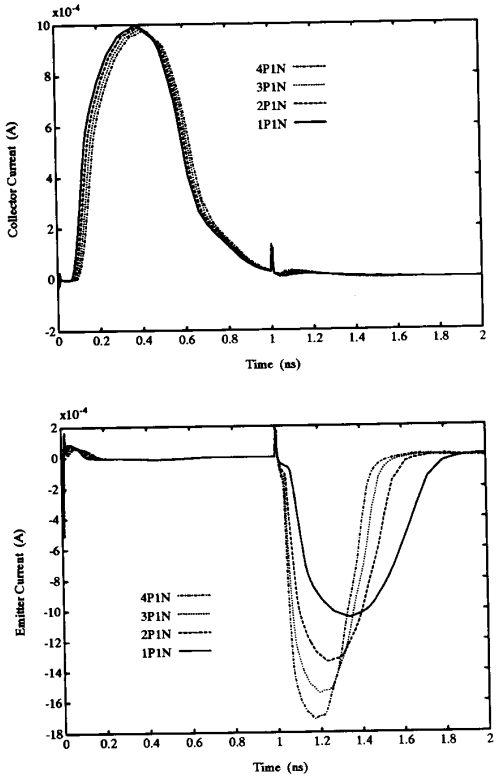


Fig. 6 The collector current of the pull-down bipolar device and the emitter current of the pull-up bipolar device during transient.

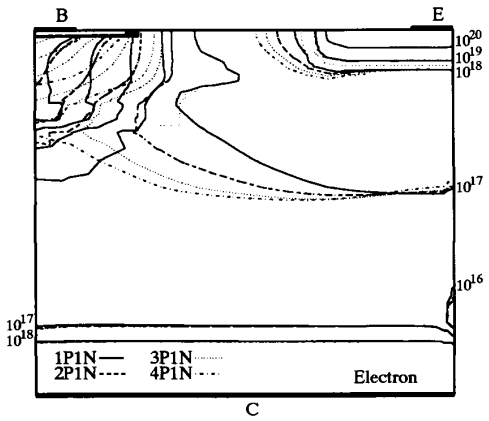


Fig. 7 Electron concentration contours in the pull-up bipolar devices during transient.

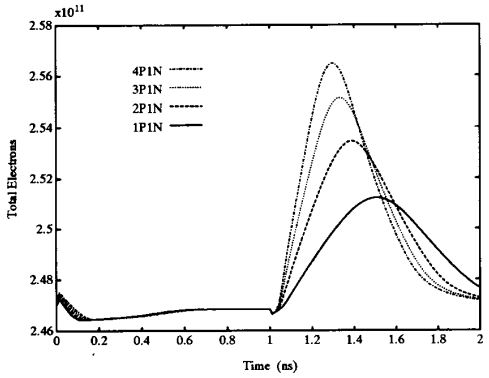


Fig. 8 Total electrons in the pull-up bipolar transistor during transient.

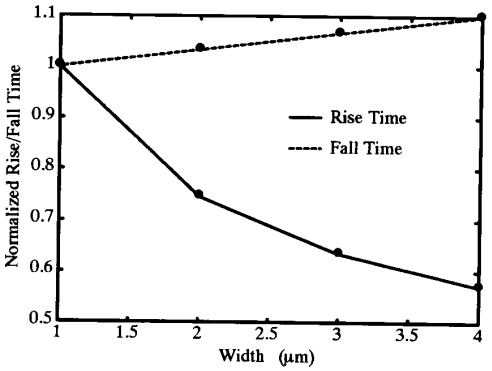


Fig. 9 Normalized rise/fall time vs. channel width of the PMOS device.