A Low Phase Noise Wide Tuning Range CMOS Quadrature VCO using Cascade Topology

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Abstract — **A new fully integrated 2.4GHz CMOS quadrature voltage control oscillator (VCO) is presented. It achieves low phase noise at quadrature outputs using the proposed cascade coupling topology. Digitally-controlled capacitor bank is designed for wide tuning range from 2.4 to 2.9GHz. By a standard 0.25μm single-poly CMOS process with thick top metal, total power consumption of two VCO cores and buffers for generating quadrature signal are 6mA and 12mA respectively. Measured phase noise at 1MHz offset from the center frequency is -114dbc/Hz.**

I. INTRODUCTION

The era of portable personal communication systems is expanding in an unprecedented fashion and rapidly becoming a part of daily lives. The highly integrated single chip transceiver is developed to reduce cost, power consumption and size. Recently, quadrature conversion transceiver is more popular due to its flexibility and high integration. In the design of these transceiver systems, a major challenge is the generation of quadrature local oscillating (LO) signal. High phase accuracy, good gain matching and low phase noise quadrature LO signal is required [1]. Several circuits RC phase shift network and poly-phase network methods are widely used in transceiver to generate quadrature LO signals. But they have restrictions in phase accuracy and gain matching since the inaccuracies in actual values of R and C. Their noise performance and driving capability do not fulfill the system requirements in most cases. Divided-by-two is another approach. But the oscillator and divider have to work at the double carrier frequency, which is either difficult to design or even hungry on power. Multi-stage VCO, like ring-type structure, is a possible way to get quadrature phase output, if its stage number is even. Ring-type VCO however exhibit poorer phase noise performance compared with the LC-type VCO. In general cross-coupled LC-tank VCO is believed to perform low phase noise for quadrature signal generation.

This work demonstrates a CMOS quadrature VCO for low power operation in the 2.45GHz range. Its tuning range has to cover 20% to against process variation. The symmetrical spiral inductors and differential varactors are all on chip to achieve highly integration. A prototype is fabricated in 0.25μm single-poly with thick top metal CMOS process.

The paper is organized as following. Section *II* discusses the design considerations of the proposed quadrature VCO. Section III descripts the VCO tuning circuits. Section IV presents measurement results. Some conclusions of this design are offered in section V.

II. PROPOSED QUADRATURE VCO

Typical quadrature signal generator is shown in Fig.1. It uses two cross-coupled VCOs to generate p/2 phase difference between I (in-phase signal node) and Q (quadrature-phase signal node) at resonant frequency [2]. Even so, this topology associates some drawbacks that limit quadrature VCO phase noise performance. Firstly, the coupling devices consume additional current. Moreover, the noise of coupling devices is easy to arise at outputs [3].

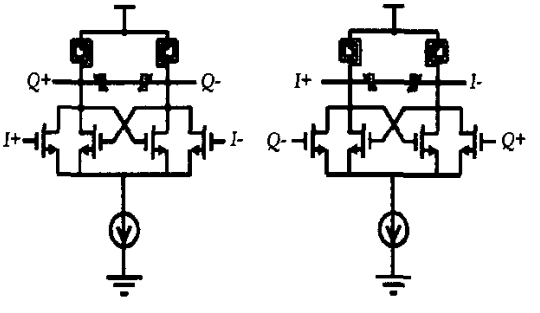

Fig.1 Typical cross coupled quadrature VCO

Fig.2 introduces a linear model for the typical quadrature VCO, where G_m represents the transconductance of

the negative-resistance pair, and G_{mc} is the transconductance of the quadrature signal coupling pair. The limiting factor in maximum oscillation frequency is the parasitic phase shift in transconductance G_{mc} of the linear model. Thus, the oscillation frequency can be descried as following:

$$w_{OSC} = \frac{\beta L_p G_m + 2\sqrt{C_p L_p + (\beta L_p G_m)^2}}{2C_p L_p}$$

where $\beta = \tan(90° - \theta)$ and $\theta = \tan^{-1}(|I_Q|/|I_I|)$ [4]. θ is proportional to the coupling factor.

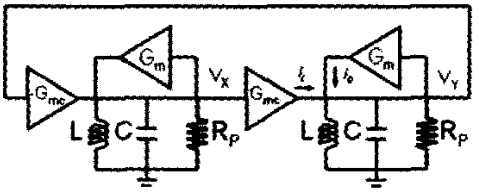

Fig.2 Linear model for a QVCO

Fig. 3 is the combined phaser diagram of the output voltages V_X and V_Y and the currents in the quadrature stage i_I and i_Q. This diagram shows that, in conventional quadrature-coupled LC oscillators, V_X and V_Y phases are shifted by p/2 when i_I and i_Q are equaled. It is noteworthy that the phase and amplitude accuracy of the quadrature outputs is proportional to coupling factors.

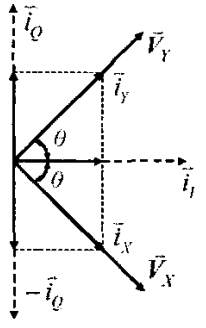

Fig.3 Combine phasor diagram of output voltage V_X and V_Y

The phase noise of typical quadrature VCO is calculated by using the linear model outlined in [5]. The phase noise can be depicted as

$$L(f_m) = \frac{1}{4\times(2Q_P\times\cos(\theta))^2}\left(\frac{f_{OSC}}{\Delta f}\right)^2 \frac{i^2_{noise}}{i^2_{carrier}}$$

where f_{OSC} is the carrier frequency, $i^2_{carrier}$ is the squared rms carrier current and Q_P is the quality factor of the resonator at the resonance frequency. As expected, the phase noise is degraded for higher coupling ratio.

In order to get good phase-noise performance and good image rejection, a cascade-connected topology is adopted [3]. This structure can force two VCO cores to generate currents with correct phase shift. The associated quadrateure phase error will be greatly reduced as the error is almost independent for the coupling stage transconductance. Besides that, this cascade can provide better isolation between the two oscillator cores.

Fig.4 shows the schematic diagram of the proposed VCO. It consists of two identical LC oscillators M1~M8, which inject-lock to each other through n-MOS coupling devices M9~M12. M9~M12 are cascading to the core, to alleviate the problems associated with the conventional approaches such as Fig. 1.

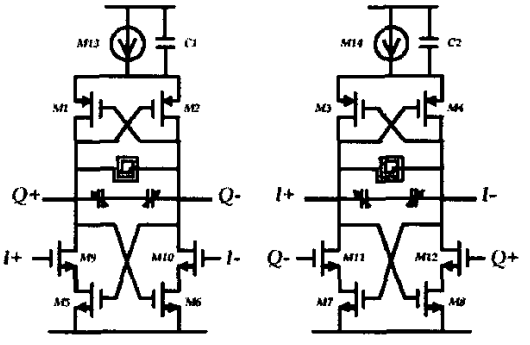

Fig.4 Proposed quadrature VCO schematic

In the VCO core p-MOS M1~M4 and n-MOS M5~M8 form two cross-coupled pairs. These cross-coupled MOS pairs act like negative resistors with their transconductances as:

$$-g_m = 2G_m = \frac{4}{R_P} = \frac{4}{Q_{tank}}\sqrt{\frac{C}{L}}$$

where G_m is the device transconductance in the cross-coupled pairs, R_p is the parallel resistance of the LC tanks at resonance frequency, L and C is the inductance and capacitor, Q_{tank} is the quality factor of the LC tanks.

Parallel p-MOS and n-MOS differential pair achieves larger oscillation amplitude than n-MOS-only, which results in a better phase noise performance for a given tail current. Symmetric rise and fall time are designed carefully to reduce the *1/f* noise upconversion [5]. In addition, large tail capacitors C1 and C2 are added to provide a low impedance path to AC ground at harmonic frequencies. This technique can attenuate high frequency noise coming of tail current, to further improves the phase noise performance of the whole VCO.

Fig.5 shows the symmetrical inductor's layout and the cross section of the differential varactors. These fully differential structures improve the tank's quality factor, reduce chip area, and keep symmetry to the oscillator circuits. All these will help to reduce flicker noise modulation.

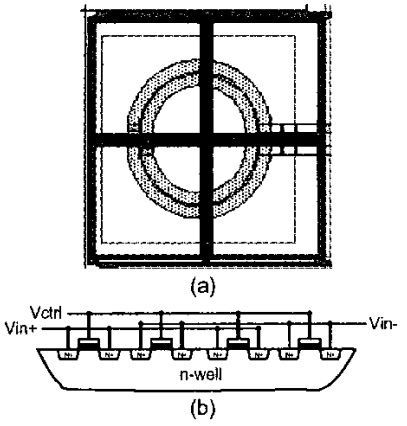

Fig.5 (a) Symmetric spiral inductor layout
(b) The cross section of differential varactors

III. DIGITAL TUNING TECHNIQUE

On-chip varactor can only provide tuning range of 100MHz, or 4% of operation frequency. To extend the tuning range to cover the process spread, Fig. 6 is the proposed digital tuning technique, without increasing the gain of VCO. In this design, digital tuning is used to push the VCO to the lock-in range of synthesizer. The analogue tuning will do the following phase-locking process.

For tuning digitally, both VCO outputs are loaded with differential 5bit binary-weighted switched-capacitor banks. Each capacitor ON/OFF state is controlled by another 5bit binary-weighted decoder. Switch in capacitor bank adopts complementary control to prevent the capacitor floating when it is on OFF state. In order to maintain same quality factor Q for each setting, NMOS switch widths also need to be binary-scaled. These digitally-tuned capacitor banks equate for an additional 500MHz tuning range according to simulations and measurement.

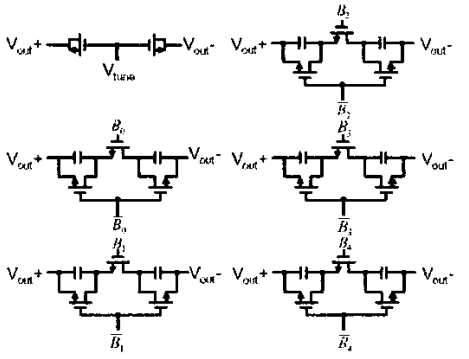

Fig.6 Digital tuning with binary-weighted capacitor bank

IV. MEASUREMENTS

The die microphotograph is shown in Fig.7. The area is 700μm x 700μm, including VCO and binary weighted control decoder. The die was mounted in a standard plastic, low cost, TSSOP package. Each single buffer output is about -10dBm under 50O measurement system. The complete quadrature VCO with buffers draws 18mA from a single 2.5V supply. The oscillator operation range is from 2.4GHz to 2.5GHz, when the control voltage is swept from 0.5V to 2V and digital tuning word is '00000'. This means the analog tuning range is 5% under the center frequency of 2.45GHz. The maximum digital tuning word '11111' sets the VCO with a maximum frequency of 2.9GHz, which yields a 20% tuning range.

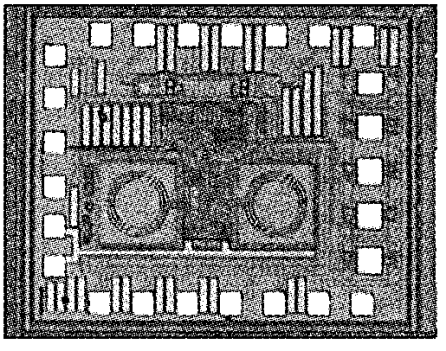

Fig.7 A die microphotograph of quadrature VCO

In-phase output phase noise are presented in Fig.11, the quadrature output has a similar phase noise characteristic. The QVCO has a phase noise of -90dBc/Hz at 100kHz offset, -101dBc/Hz at 300kHz offset, -112dBc/Hz at 1MHz offset from 2.4GHz to 2.9GHz.

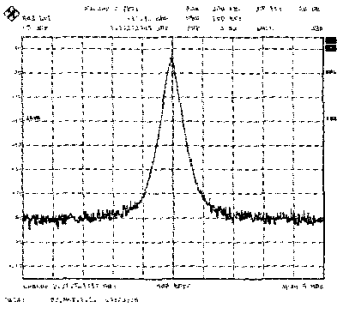

Fig.8 QVCO output spectrum at 2.4GHz

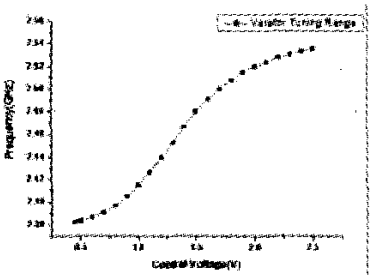

Fig.9 Measured varactors tuning range of QVCO

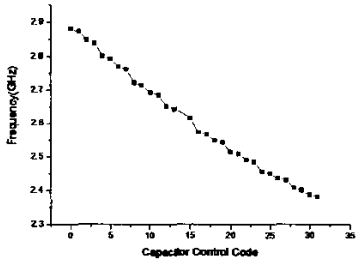

Fig.10 Measured digital tuning range of QVCO

The phase error over the whole tuning range was less than 1.5 degrees. The amplitude error was less than 1dB. Image rejection ratio (IRR) therefore can be better than 50dB.

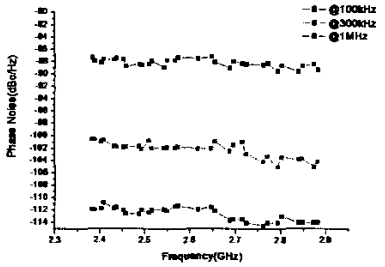

Fig.11 Measured phase noise through whole tuning range

The measurement results of the quadrature VCO with output buffers are summarized in Table I.

Parameter	Performance
Technology	0.25μm 1P5M CMOS
Oscillator Frequency	2.4GHz ~ 2.9GHz
Tuning Range	20%
Phase Noise @ 1 MHz offset	-114dBc/Hz
Phase Error	< 1.5?
Amplitude Error	< 1dB
Power Consumption (W/O Buffer)	6 mA@2.5V

Table 1 Performance summary of the proposed QVCO.

V. CONCLUSION

Cross-coupled structure is widely used for quadrature VCO design. Cascade topology adopted is proven to possess lower phase noise characteristic rather than the conventional parallel-coupled configuration. Based on this insight, a monolithic 2.4GHz CMOS quadrature VCO using 0.25μm technology has been realized. Several techniques like balance N- and P- cross-coupled structure and bypass tail current harmonics are incorporated to further reduce output phase noise. Digitally switched capacitor bank helps on a wide tuning rang. Image rejection ratio is expected to be better than 50dB as the gain and phase mismatch is small. The phase noise is -114dBc/Hz at 1MHz offset over the whole tuning range. This quadrature VCO achieves low phase noise under low power dissipation.

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