

## Composite Effects of reflections and Ground Bounce for Signal Vias in Multi-Layer Environment

Sheng-Mou Lin and Ruey-Beei Wu

Dept. of Electrical Engineering and Graduate Institute of Communication Engineering,  
National Taiwan University, Taipei, Taiwan, 10617, R.O.C.

E-mail: rbwu@ew.ee.ntu.edu.tw

The signal propagating down the vias in a multi-layer environment will suffer from composite effects of reflected noise by via discontinuity and ground bounce between power/ground planes. An equivalent circuit modeling is proposed to simulate these effects, which consists of transmission line for signal line, lumped inductance and capacitance for via discontinuity, and two-dimensional field solver for the region between power and ground planes. Simulations are performed for a four-layer structure and three different cases are considered to characterize both effects. Results show that the via discontinuity is dominant for reflected noise in the early time response, while the ground bounce is dominant in the late time response.

### 1 Introduction

As the switching speed of digital circuits becomes higher, the parasitic effects due to the stray elements of the packaging structure cause an essential concern in the signal integrity issues. For through hole vias, there are two major signal integrity concerns; the reflection from the via discontinuity and the ground bounce which is the voltage fluctuations between power and ground planes of printed circuit boards (PCB) or chips caused by sudden switching currents. As currents flow through signal vias in multi-layer circuits, ground bounce will be generated between metal planes, which will in turn induce noise currents to propagate in signal lines. To accurately model the propagation characteristics of through hole vias and the composite effects of signal reflection and ground bounce becomes more important as the system operating frequencies are steadily increasing.

Although the three-dimensional Finite-Difference Time-Domain (FDTD) method has been used to discuss this problem [1] [2], its prohibitively long computation time and large computer memory space has limited its applications to very simplified structures, especially for multi-layer structures. In view of the structure similarity to parallel-plates, simplified two-dimensional FDTD has been proposed to discuss the voltage fluctuations caused by signal vias [3] [4]. In this paper, the equivalent circuits of the via discontinuities are extract by using quasi-static analysis [5] and are combined with the two-dimensional FDTD method to model the propagation of electromagnetic wave between metal planes and the transmission line theory for signal lines. The 2D FDTD and transmission line simulations can be performed separately and linked together with the discontinuity models at each computation time step. The effects of the discontinuity on signal propagation are thus characterized.

### 2 Theory

A typical through via hole in a multi-layer structure can be shown in Fig. 1. Along the signal flow path, the whole structure can be divided into three parts, the transmission line, via discontinuity, and the parallel plates. Since the separation between two metal planes is typically much less than the size of the planes, the fields between the two metal planes can be assumed to be uniform along the vertical direction. Consequently, the electromagnetic fields between two metal planes are two-dimensional, and can be solved by the two-dimensional FDTD method.

The transmission line structures in most multi-layer packaging are dominantly microstrip line or stripline. Given the propagation constant and characteristic impedance, the signal line is modeled by

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equivalent LC ladder circuits and the signal propagation is simulated by telegraphy equation using central difference discretization.

The via is employed to connect two signal lines in different layers. Depending on the presence of the power or ground planes in between, there are six fundamental configurations of signal vias as shown in Fig. 2. Most complex signal via structures can be decomposed into the superposition of these six fundamental configurations. Because the size of the via discontinuity is much less than the wavelength, it is fairly good to assume a quasi-static field behavior near the discontinuity. The excess charges on the via represents the additional electric energy storage and are modeled by lumped capacitance. On the other hand, the currents flow on the via will cause additional stored magnetic energy and can be modeled by lumped inductance. For the extraction of circuit values, the capacitance is found from a moment-method solution for an integral equation governing the excess charge distribution, while inductance can be derived analytically by employing the idea of partial inductance and assuming a filament current along the via [5]. Computer programs and analytic expressions for C and L, respectively, have been established for all the six basic configurations. Hence, the equivalent circuits of the via discontinuity can be easily constructed from the given geometric parameters of the structures.

### 3 Circuit Modeling and Simulation Results

Take a through hole via in a four-layer structure, shown in Fig. 3(a) as an example. A microstrip line in layer one connects to a microstrip line in layer four by a via through two metal planes. Fig. 3(b) shows a schematic view of the structure where  $I$  denotes the current along the via and  $V_g$  the resultant ground bounce voltage exhibited between the two metal plates. The equivalent circuit model for the structure is shown in Fig. 3(c), where  $Z_1, Z_2$  are the characteristic impedance of the signal lines,  $L_1, C_1$  are the equivalent circuit elements for the via configuration in Fig. 2(b),  $L_2, C_2$  are the circuit elements for the via configuration in Fig. 2(d). The ground bounce voltage  $V_g$  is related to the via current  $I$  by a 2D FDTD solver for the electromagnetic field in the region between the two plates [4]. The transmission line is modelled by the telegraph's equation. The 2-D FDTD solver and the telegraphy equation are performed separately and simultaneously. The values of  $I$  and  $V_g$  are interchanged after each time step.

A typical structure in Fig. 3(a) includes a square PCB ( $x=y$ ) with same height in each layer ( $h_1=h_2=h_3$ ) and the same microstrip lines in the top and bottom layers ( $w_1=w_2, \ell_1=\ell_2$ ). The dimensions are listed in table 1 and the extracted values of the inductance and capacitance are listed in table 2. Three different cases are simulated for comparison, Case I: with via discontinuity model but neglecting ground bounce voltage ( $V_g=0$ ), Case II: with both of the via discontinuity model and ground bounce voltage  $V_g$ , and Case III: with ground bounce voltage  $V_g$  but neglecting via discontinuity model. The signal voltage source is a Gaussian pulse generator in series with an internal resistance of 89ohm. On the other end of the signal line is connected a matched load.

The voltages at point a and b are monitored and the waveforms are shown in Fig. 4(a), while the ground bounce voltage  $V_g$  is shown in Fig. 4(b). As found from the figure, the reflection and ground bounce are noticeable in the time frames 250-450ps and 800-1400ps. When the ground bounce voltage shown in Fig. 4(b) is significant. The waveform time frame between 250ps and 450ps, is enlarged to be shown in Fig. 5(a) while that between 800ps and 1400ps is enlarged and magnified in Fig. 5(b). For the early time response in Fig. 5(a), the results of Case I is close to Case II, meaning that the reflected noise is more significant than the ground bounce noise at the early time when the signal travels down to the via. On the contrary, from Fig. 5(b), the results of Case III is close to Case II, meaning that the ground bounce is responsible for the late-time response.

### 4 Conclusions

This paper presents a comprehensive modelling for the through hole vias in the multi-layer packaging structure. The model includes the equivalent lumped circuits for the via discontinuity and the ground bounce voltage between two metal planes. The influence of via discontinuity can be neglected at late-time but is dominant at early time.

## References

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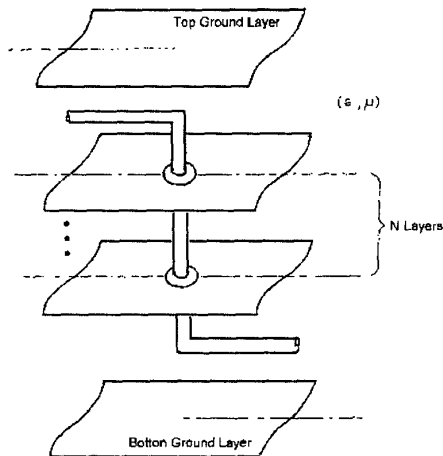


Fig. 1 A typical through via hole in a multi-layer structure

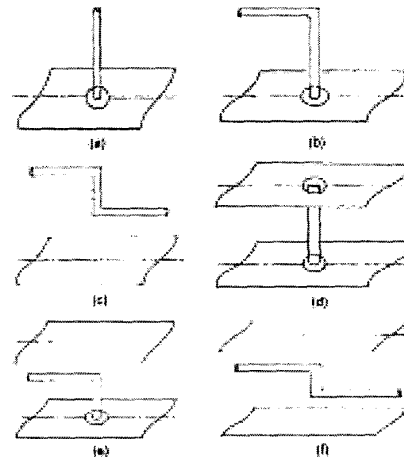
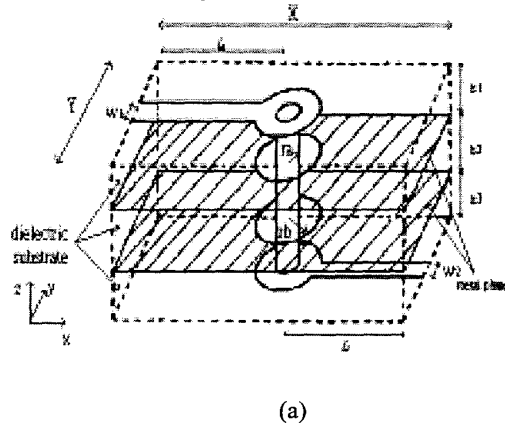
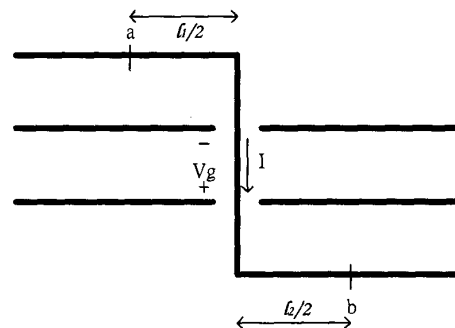


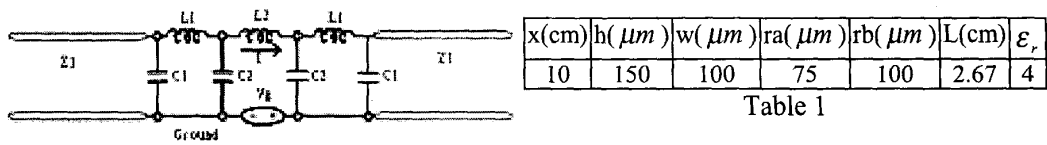
Fig. 2 Six fundamental via configurations in multi-layer packaging structures



(a)



(b)

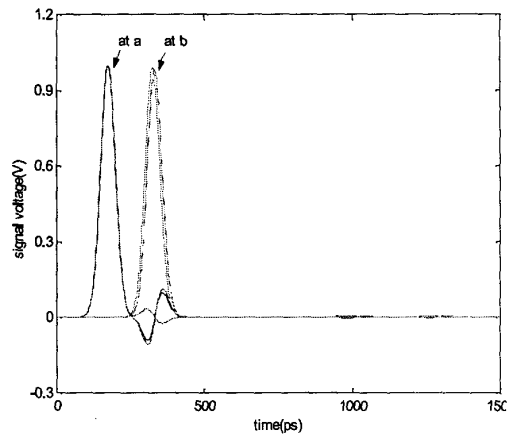


x(cm)	h( $\mu$ m )	w( $\mu$ m )	ra( $\mu$ m )	rb( $\mu$ m )	L(cm)	$\epsilon_r$
10	150	100	75	100	2.67	4

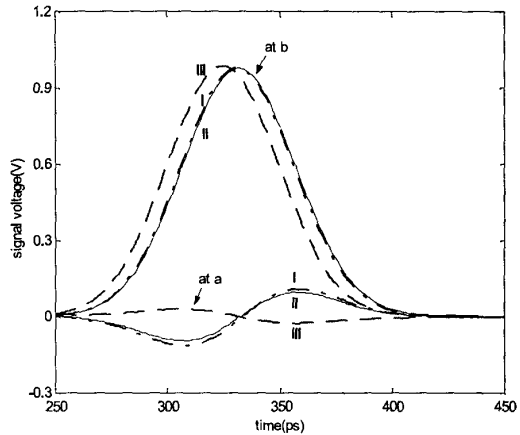
Table 1

Z1(ohm)	L1(pH)	L2(pH)	C1(fF)	C2(fF)
89	31.45	200	20.8	55.5

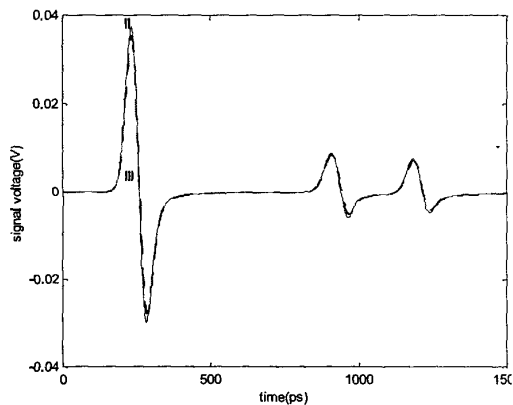
Table 2



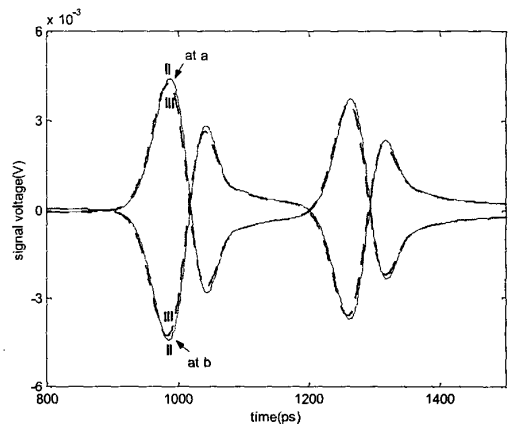
(a)



(b)



(a)



(b)

Fig. 4 (a) voltage waveforms at points a and b  
(b) The generated ground bounce noise

Fig. 5 Enlarged view for the waveforms at  
(a) 250 to 450ps (b) 800 to 1500ps