

# Effects of laser activation on device behaviour for poly-Si thin-film transistors with different channel lengths

C.-L. Fan, T.-H. Yang, Y.-C. Chen and J. Lin

The effects of laser activation on device behaviour for low-temperature-processed poly-Si thin-film transistors (TFTs) is investigated. The source/drain resistance has a different weight on the device behaviour of laser-activated poly-Si TFTs for different channel lengths. When channel resistance is decreased as a result of the lower grain boundary number in short channel lengths, the source/drain resistance has a significant weight on the device on-state resistance, causing obvious sensitivity between device performance and laser activation energy density, compared with devices fabricated with a long channel length. From the manufacturing view, this sensitivity may cause a narrow laser activation process window resulting in device characteristic uniformity issues.

**Introduction:** Low-temperature-processed (LTP) polycrystalline silicon thin-film transistors (poly-Si TFTs) have drawn much attention because of their wide applications to active-matrix flat-panel displays [1]. For LTP poly-Si TFT fabrication using traditional procedures, the implant-annealing used to activate the dopants and remove damage defects is usually carried out using furnace annealing of 600°C for several tens of hours (about 12–24 h) after source/drain implantation [2]. The prolonged activation time causes low throughput LTP poly-Si TFTs mass production. In recent years, many investigations reported that excimer-laser activation after self-aligned implantation can replace furnace activation (FA) to reduce activation time and resistivity of the source/drain regions. However, these reports have focused mainly on the source-drain region activation mechanism for laser-activated LTP TFTs [3, 4]. However, to achieve system-on-panel (SOP) applications, the integrated driver-circuit will require high-performance TFTs with a short channel length. Therefore, it is worthwhile investigating the correlation between device channel length and high-throughput laser-activated process. In this Letter, the effects of laser activation on device behaviour in LTP poly-Si TFTs with different channel lengths is discussed for the first time, particularly for short channel devices.

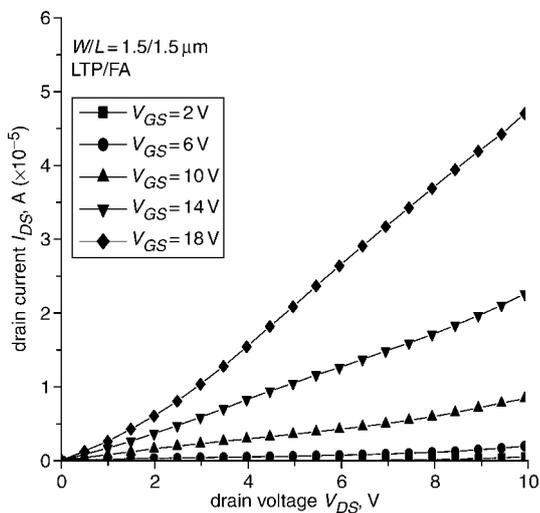


Fig. 1 Typical output curves of LTP poly-Si TFTs activated using FA scheme

**Experiment:** N-channel solid-phase-crystallisation (SPC) poly-Si TFTs using laser activation (LA) were fabricated according to the following procedures. A 110 nm-thick amorphous Si-layer was first deposited on an oxide covered Si-substrate at 550°C using a SiH<sub>4</sub> process. Then, SPC was performed at 600°C for 24 h in N<sub>2</sub> ambient. The average grain size observed by TEM is about 100–200 nm. Individual active regions were patterned and a 120 nm-thick tetraethyl orthosilicate (TEOS) oxide using high density plasma chemical vapour deposition (HDP-CVD) was deposited to serve as the gate insulator. A second poly-Si film was subsequently deposited and patterned to define the device gates. Next, the source/drain and gate

regions were implanted with phosphorus via ion implantation to a dose of  $5 \times 10^{15} \text{ cm}^{-2}$ . The implanted regions were then activated by a KrF excimer laser ( $\lambda = 248 \text{ nm}$ ) with various energy densities at room temperature in a vacuum ambient ( $\sim 10^{-3}$  torr). A passivation layer with 500 nm-thick HDP-CVD TEOS oxide was deposited at 300°C after LA. Contact holes were then opened and 500 nm-thick Al electrodes were deposited and patterned, followed by a sintering process at 400°C for 30 min in N<sub>2</sub> ambient. For comparison, control samples were fabricated following the same process except that the LA was replaced by FA conducted at 600°C for 12 h in N<sub>2</sub> ambient. The devices subjected to FA were denoted as LTP/FA and the others subjected by LA were denoted as LTP/LA.

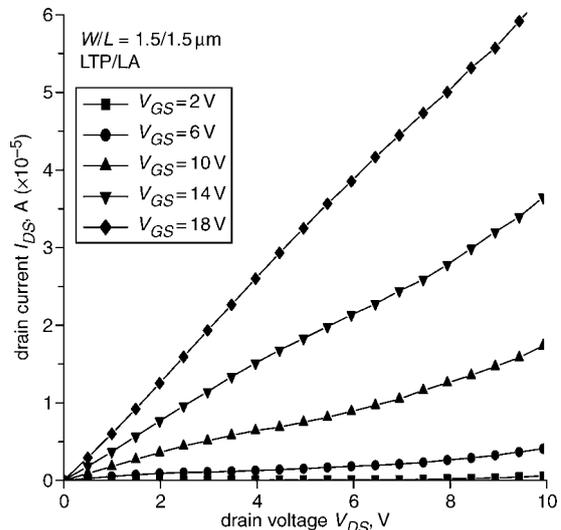
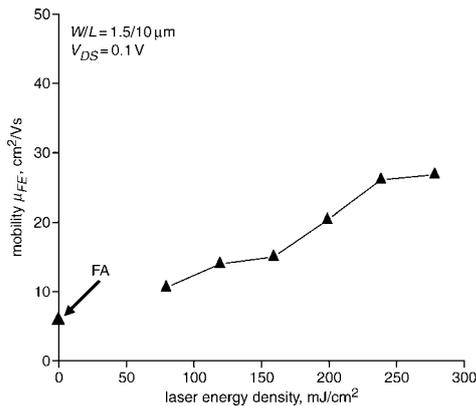


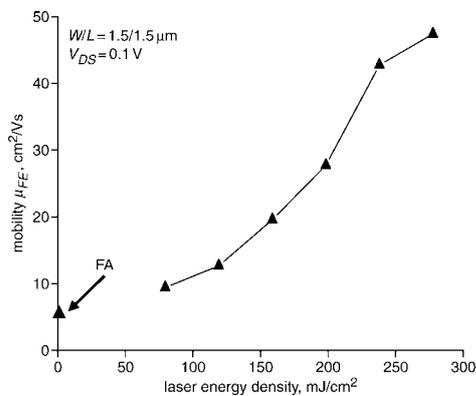
Fig. 2 Typical output curves of LTP poly-Si TFTs activated using LA scheme with laser energy density 200 mJ/cm<sup>2</sup>

**Results and discussion:** Figs. 1 and 2 show the typical output curves of LTP/FA and LTP/LA TFTs with the channel width/channel length = 1.5/1.5 μm, respectively, to distinguish FA from LA scheme activation efficiency. We found that the TFTs fabricated with LA exhibited significantly better turn-on state performance than those fabricated using FA. The measured resistivities were 1.57 and 5.08 mΩ cm for the LA and FA samples, respectively, indicating that a significant reduction in sheet resistivity of source/drain regions was indeed obtained using the LA method. Figs. 3 and 4 show the field-effect mobility ( $\mu_{FE}$ ) against irradiated laser-energy-density with channel length of 10 or 1.5 μm, respectively, for the LTP poly-Si TFTs activated with the LA scheme. It was found that the  $\mu_{FE}$  increases with laser-energy-density for the poly-Si TFTs, as shown in both Figures. This is because an increase in the irradiated laser-energy-density results in an increase in the activation efficiency, causing a decrease in source/drain resistance and hence improved performance with increasing laser-energy-density. However, we found, for the 1.5 μm channel length, the  $\mu_{FE}$  of the LTP/LA samples was significantly improved and very sensitive to increasing laser-energy-density, compared to those with a 10 μm channel length. It has been reported that the TFT turn-on state resistance,  $R_{ON}$ , consists of the channel resistance,  $R_{CH}$ , and the parasitic resistance  $R_{PA}$  [5]. The  $R_{PA}$  is correlated mainly to the source/drain resistance. Thus, we evaluated the activation effect of the source/drain regions on the  $R_{PA}$ . The  $R_{CH}$  is mainly related to the crystallinity of the channel film. The better the crystallinity of the channel film, the lower the  $R_{CH}$  value. Generally, the crystallinity of the channel film is dominated by the grain-boundary density in the channel film. The larger the channel film grain size, the lower the grain-boundary density of the channel film [6], i.e. the density of the grain-boundary in the channel film will dominate the  $R_{CH}$  values. As a result of few grain-boundary numbers in the short channel length, the  $R_{CH}$  is reduced with decreasing channel length and hence the  $R_{PA}$  has an increased  $R_{ON}$  weight. For the LTP/LA devices with short channel length, the  $R_{PA}$  has an increased  $R_{ON}$  weight, resulting in significant sensitivity to the improved  $\mu_{FE}$  with respect to the increasing laser-energy-density, as shown in Fig. 4. In addition, the shorter the device channel length, the larger the  $R_{PA}$  weight on  $R_{ON}$ . Thus, especially for short channel

length devices consisting of few grain-boundary numbers, the sensitivity with regard to increasing the laser-energy-density in performance improvement is obviously increased as a result of the increasing  $R_{PA}$  weight on  $R_{ON}$ . Unfortunately, from the manufacturing view, this sensitivity may result in a narrow laser activation process window, causing the device characteristic uniformity issues. Thus, for LTP poly-Si TFTs produced using the LA scheme, the optimal trade-off between channel length, laser activation energy density and device characteristic uniformity should be carefully and simultaneously designed. Moreover, note that if the grain size is sufficiently large and/or comparable to the different channel length, the amount of grain-boundary in the channel will be nearly identical to the various channel lengths. Thus, for devices with different channel lengths, the difference in sensitivity between improved performance and increasing laser-energy-density will decrease as a result of the small difference in  $R_{CH}$  values.



**Fig. 3** Field-effect mobility ( $\mu_{FE}$ ) against irradiated laser-energy-density for LTP poly-Si TFTs with channel width/channel length = 1.5/10  $\mu\text{m}$ . Data of poly-Si TFT using FA scheme included for comparison



**Fig. 4** Field-effect mobility ( $\mu_{FE}$ ) against irradiated laser-energy-density for LTP poly-Si TFTs with channel width/channel length = 1.5/1.5  $\mu\text{m}$ . Data of poly-Si TFT using FA scheme included for comparison

**Conclusions:** We investigated the laser activation effects on LTP poly-Si TFTs with different channel lengths. As a result of the few grain-boundary numbers in short channel lengths, the channel resistance is decreased, resulting in source/drain resistance with increasing weight on the device turn-on resistance. Thus, for devices with short channel length, the sensitivity between device performance and laser activation energy density is significantly increased, compared with those devices with long channel length. This sensitivity will cause a narrow laser activation process window that produces device characteristic uniformity issues.

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