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A VELOCITY-OVERSHOOT CAPACITANCE MODEL FOR 0.1 μm MOS TRANSISTORS

J. B. KUO*, Y. W. CHANG and C. S. LAI

Rm 338, Department of Electrical Engineering, National Taiwan University, Roosevelt Rd, Sec. 4, #1, Taipei, Taiwan 106-17

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Abstract—This article discusses an analytical velocity-overshoot capacitance model for a 0.1 μm MOS transistor. As verified by 2D simulation results, compared to the conventional model the analytical capacitance model considering velocity overshoot shows a smaller C_{SG} and C_{DG} value, because in velocity overshoot a smaller amount of electrons exist in the channel region. Compared to the C_{SG} case, the larger decrease in C_{DG} when considering velocity overshoot at high V_D is the result of higher electron velocity in the post-saturation region. Copyright © 1996 Elsevier Science Ltd

1. INTRODUCTION

For decades the evolution of MOS devices has already been consistently continued. Sub-0.1 μm MOS devices for next generation VLSI have been reported[1]. Since the supply voltage can't be scaled down sufficiently for deep submicron MOS devices, a large electric field is unavoidable in some regions of the lateral channel. Therefore traditional drift-diffusion models are not adequate for describing its device characteristics. In order to account for a high-electric-field effect, the energy transport equation for analyzing the electron temperature distribution in the channel has been included in an analytical DC model for MOS transistors[2–4]. For deep submicron MOS devices designed with a large electron mobility, electrons in some region of its very short channel may be traveling at a velocity higher than the saturated velocity (the velocity overshoot phenomenon[5–9]). For a deep submicron NMOS device with velocity overshoot behavior, its device model is further complicated. Recently an analytical DC drain current formula for deep submicron NMOS devices considering velocity overshoot phenomenon has been reported and the effect of velocity overshoot on the drain current has been evaluated[10]. For a deep submicron MOS device, the drain current alone cannot describe the device performance. Capacitance is also very important in determining the overall performance of such a device. In the past MOS capacitance models have been discussed in-depth for transient analysis of MOS devices[11]. An analysis of capacitances in MOS devices considering velocity saturation has been reported[12]. However a capacitance model of a MOS device considering velocity overshoot has not been reported. In this paper an analytical source-gate and drain-gate capacitance model considering velocity overshoot for a 0.1 μm NMOS device is described. In the following sections, the derivation of the analytical model is described first, followed by a verification of the model and a discussion.

2. MODEL DERIVATION

In this section a velocity-overshoot capacitance model for a 0.1 μm MOS device is derived. Consider a 0.1 μm NMOS device with its origin at the source end and its y-axis in the lateral channel direction. In order to simplify the analysis, the gate fringing capacitance and the gate-source and the gate-drain overlap capacitances[13,14] are not considered. Based on the partitioned-charged capacitance model[11], the source charge and the drain charge are given by:

$$Q_S = W\int_0^L \left(1-\frac{y}{L}\right)n(y)\mathrm{d}y, \tag{1}$$

$$Q_D = W\int_0^L \frac{y}{L}n(y)\mathrm{d}y, \tag{2}$$

respectively, where W is the width, L is the effective channel length and $n(y)$ is the unit-area induced charge density at location y in the channel. Using eqns (1) and (2), the source-gate and drain-gate capacitances are defined as:

$$C_{SG} \equiv -\frac{\partial Q_S}{\partial V_G}\frac{1}{WL},$$

$$C_{DG} \equiv -\frac{\partial Q_D}{\partial V_G}\frac{1}{WL}, \tag{3}$$

respectively.

*To whom correspondence should be addressed.

2.1. Energy transport

For an NMOS device the energy balance equation [15] is:

$$\frac{dS}{dy} = JE - 2n\frac{k(T_n - T_0)}{\tau_\epsilon}, \tag{4}$$

where y is the lateral direction, J is the electron current density, E is the lateral electric field, k is the Boltzmann constant, T_n is the electron temperature, T_0 is the ambient temperature, n is the electron density, τ_ϵ is the energy relaxation time, S is the electron energy flux and $2kT_n$ is the average kinetic energy per electron arising from current flow. The electron energy flux is expressed as:

$$S = -\kappa\frac{dT_n}{dy} - 2J\frac{kT_n}{q}, \tag{5}$$

where κ is the thermal conductivity, q is the electron charge. In the NMOS device the electron current, which is mainly composed of drift current, is:

$$J = nq\mu_n(T_n)E, \tag{6}$$

where $\mu_n(T_n)$ is the temperature-dependent electron mobility[15]:

$$\mu_n(T_n) = \mu_s\left(\frac{T_n}{T_0}\right)^{-0.5}, \tag{7}$$

where μ_s is the surface electron mobility[16]:

$$\mu_s = \frac{\mu_0}{1 + \theta(V_G - V_T)}.$$

From eqns (4)–(7) by neglecting the second order derivative term, one obtains a differential equation in terms of the electron temperature:

$$\frac{dT_n}{dy} = -\frac{qE}{2k} + \frac{(T_n - T_0)}{\tau_\epsilon\mu_s E}\left(\frac{T_n}{T_0}\right)^{0.5}. \tag{8}$$

However, at steady state, the electron mobility is also field dependent[17]:

$$\mu_n(E) = \frac{\mu_s}{\left[1 + \left(\frac{\mu_s E}{v_{sat}}\right)^2\right]^{1/2}}, \tag{9}$$

where v_{sat} is the electron saturated velocity[18]:

$$v_{sat} = \frac{2.4 \times 10^7}{1 + 0.8 \times \exp(T_0/600)}\ (\text{cm sec}^{-1}). \tag{10}$$

At steady state the electron temperature dependent mobility is equal to the electric-field dependent mobility ($\mu_n(T_{nss}) = \mu_n(E)$). Therefore from eqns (7) and (9), the steady-state electron temperature is:

$$T_{nss} = T_0\left[1 + \left(\frac{\mu_s E}{v_{sat}}\right)^2\right]. \tag{11}$$

Since the energy relaxation time is related to the difference between the steady-state electron temperature (T_{nss}) and the ambient temperature and the electric field, as for instance

$$\tau_\epsilon = \frac{2k(T_{nss} - T_0)}{qEv_{ss}}, \tag{12}$$

from eqns (11) and (12) one obtains:

$$\tau_\epsilon = \frac{2kT_0\mu_s^2}{q\mu_n(E)v_{sat}^2} = \frac{2kT_0\mu_s^2}{q\mu_n(T_n)v_{sat}^2}. \tag{13}$$

Next from eqns (13) and (8) a differential equation in terms of the electron temperature is obtained:

$$\frac{dT_n}{dy} = -\frac{qE}{2k} + \frac{(T_n - T_0)qv_{sat}^2}{2kT_0E\mu_s^2}. \tag{14}$$

The electric field in the lateral channel between source and the saturation point has been assumed to be linear:

$$E(y) = E_0 + ay, \tag{15}$$

where E_0 and a are defined as:

$$E_0 = -\frac{\eta V_{DSAT}}{L - \Delta L},$$

$$a = -\frac{2(1-\eta)V_{DSAT}}{(L - \Delta L)^2}. \tag{16}$$

From eqns (14) and (15) in this case one obtains:

$$\frac{dT_n}{dy} = -\frac{q(E_0 + ay)}{2k} + \frac{(T_n - T_0)qv_{sat}^2}{2kT_0(E_0 + ay)\mu_s^2}. \tag{17}$$

Solving eqn (17) with the boundary condition that at the source end the electron temperature is equal to the ambient temperature ($T_n(y = 0) = T_0$), the distribution of the electron temperature in the lateral channel of the device is given by

$$T_n(y) = T_0 + \frac{B}{A+2}(E_0 + ay)^2\left[1 - \left(\frac{E_0}{E_0 + ay}\right)^{A+2}\right],$$

$$A = -\frac{qv_{sat}^2}{2akT_0\mu_s^2},$$

$$B = -\frac{q}{2ak}. \tag{18}$$

As η is small, $(E_0/E_0 + ay)^{A+2}$ can be neglected. Therefore the electron temperature distribution becomes:

$$T_n(y) \cong T_0 + \frac{B}{A+2}(E_0 + ay)^2. \tag{19}$$

2.2. Drain current

Using Ref.[19], the drain current is given by

$$I_D = \mu_{eff}C_{ox}\frac{W}{L - \Delta L}[(V_{GS} - V_T)V_{DX} - \tfrac{1}{2}V_{DX}^2], \tag{20}$$

where V_T is the threshold voltage considering drain induced barrier lowering effect: $V_T = V_{t0} - \sigma V_{DS}$, where V_{t0} is the zero bias threshold voltage, σ is a coefficient. μ_{eff} is the effective electron mobility. Using a unified formula for both triode and saturation regions, V_{DX} is organized as:

$$V_{DX} = V_{DS} + V_{DSAT} - (V_{DS}^3 + V_{DSAT}^3)^{1/3}. \tag{21}$$

From eqn (21), in the triode region, $V_{DX} \rightarrow V_{DS}$. In the saturation region, $V_{DX} \rightarrow V_{DSAT}$, where V_{DSAT} is defined as:

$$V_{DSAT} = \frac{V_{DSAT1} V_P}{V_{DSAT1} + V_P}, \tag{22}$$

in which V_P is determined by the pinchoff point: ($V_P = V_G - V_T$), and V_{DSAT1} is determined by the velocity saturation point. As the drain voltage reaches $V_D = V_{DSAT1}$, the electric field at the drain equals

$$E(y = L) = \frac{-(2-\eta)V_{DSAT1}}{L}. \tag{23}$$

Under this condition, the electron velocity at the drain just reaches the saturated velocity. Therefore

$$\mu_n(E(y=L))|E(y=L)| = \frac{\mu_s|E(y=L)|}{\sqrt{1+\left(\frac{\mu_s E(y=L)}{v_{sat}}\right)^2}} = \eta_1 v_{sat}. \tag{24}$$

According to eqns (23) and (24) V_{DSAT1} becomes:

$$V_{DSAT1} = \frac{\eta_1 v_{sat} L}{(2-\eta)\sqrt{1-\eta_1^2}\mu_s}. \tag{25}$$

From Ref.[3] the distance between the saturation point and drain is found to equal

$$\Delta L = s\lambda \ln\left[\frac{-(V_{DS} - V_{DX} - a_1\lambda^2) - \sqrt{(V_{DS} - V_{DX} - a_1\lambda^2)^2 + \lambda^2(E_1^2 - a_1^2\lambda^2)}}{\lambda(E_1 + a_1\lambda)}\right],$$
$$\lambda = \sqrt{\frac{\epsilon_{Si} x_j t_{ox}}{\epsilon_{ox}}},$$
$$a_1 = -\frac{2(1-\eta)V_{DX}}{L^2},$$
$$E_1 = -\frac{\eta V_{DX}}{L}. \tag{26}$$

Since in the triode region $V_{DX} \rightarrow V_{DS}$, $\Delta L \rightarrow 0$.

The effective electron mobility is expressed as:

$$\mu_{eff} = \frac{L - \Delta L}{\int_0^{L-\Delta L} \frac{1}{\mu_n} dy}. \tag{27}$$

From eqns (7) and (27) by considering the electron temperature distribution in the channel the effective mobility is expressed as:

$$\mu_{eff} = \frac{\mu_s(L - \Delta L)}{\int_0^{L-\Delta L} \left(\frac{T_n}{T_0}\right)^{1/2} dy}. \tag{28}$$

Using the electron temperature profile formula (eqn (19)), eqn (28) becomes

$$\mu_{eff} = \frac{\mu_s T_0^{1/2}(L - \Delta L)}{\int_0^{L-\Delta L} \sqrt{T_0 + \frac{B}{A+2}(E_0 + ay)^2} dy}. \tag{29}$$

Finally by carrying out the integral of eqn (29) the effective electron mobility becomes:

$$\mu_{eff} = \frac{\sqrt{\frac{A+2}{B}} a\mu_s T_0^{1/2}(L - \Delta L)}{\left[\frac{E}{2}\sqrt{E^2 + \frac{T_0(A+2)}{B}} + \frac{T_0(A+2)}{2B}\ln\left(E + \sqrt{E^2 + \frac{T_0(A+2)}{B}}\right)\right]\Bigg|_{E=E(y=0)}^{E=E(y=L-\Delta L)}}, \tag{30}$$

$$E(y = L - \Delta L) = -\frac{(2-\eta)V_{DX}}{L - \Delta L}. \tag{31}$$

2.3. Capacitances

Based on the drain current model and the partitioned-charge model, the source-gate and drain-gate capacitances of the 0.1 μm NMOS device are derived in this section.

The lateral channel is divided into two sections: (1) the pre-saturation section ($0 < y < L - \Delta L$), and (2) the post-saturation section ($L - \Delta L < y < L$). Therefore, Q_S and Q_D as indicated in eqns (1) and (2) can be expressed as:

$$Q_S = Q_{S1} + Q_{S2}, \tag{32}$$

$$Q_D = Q_{D1} + Q_{D2}, \tag{33}$$

where Q_{S1} and Q_{D1} are defined as:

$$Q_{S1} = W\int_0^{L-\Delta L}\left(1 - \frac{y}{L}\right)n(y)dy, \tag{34}$$

$$Q_{D1} = W\int_0^{L-\Delta L}\frac{y}{L}n(y)dy, \tag{35}$$

and Q_{S2} and Q_{D2} are defined as:

$$Q_{S2} = W\int_{L-\Delta L}^{L}\left(1-\frac{y}{L}\right)n(y)\mathrm{d}y, \quad (36)$$

$$Q_{D2} = W\int_{L-\Delta L}^{L}\frac{y}{L}n(y)\mathrm{d}y. \quad (37)$$

2.3.1. Pre-saturation region. In the presaturation region ($0 \leqslant y \leqslant L-\Delta L$), the unit-area charge density at location y in the channel is:

$$n(y) = -C_{ox}(V_G - V_T - V(y)), \quad (38)$$

where $V(y)$ is the potential at location y in the channel. Using the channel electric field distribution formula as shown in eqn (15), the channel potential becomes:

$$V(y) = \int_0^y -(E_0 + ay')\mathrm{d}y' = -E_0 y - \frac{1}{2}ay^2. \quad (39)$$

From eqns (34, 35, 38 and 39), one obtains Q_{S1} and Q_{D1} in the presaturation region to equal

$$Q_{S1} = -C_{ox}W\left[(V_G - V_T)(L-\Delta L) + \frac{1}{2}\left(E_0 - \frac{V_G - V_T}{L}\right)(L-\Delta L)^2 + \frac{1}{3}\left(\frac{1}{2}a - \frac{E_0}{L}\right)(L-\Delta L)^3 - \frac{1}{8}\frac{a}{L}(L-\Delta L)^4\right], \quad (40)$$

$$Q_{D1} = -C_{ox}\frac{W}{L}\left[\frac{1}{2}(V_G - V_T)(L-\Delta L)^2 + \frac{1}{3}E_0(L-\Delta L)^3 + \frac{1}{8}a(L-\Delta L)^4\right]. \quad (41)$$

2.3.2. Post-saturation region. In the post-saturation region ($L-\Delta L \leqslant y < L$), the electrons are travelling at the velocity at the saturation point ($y = L-\Delta L$). From eqn (31), at the saturation point ($y = L-\Delta L$), the electric field is:

$$E(y = L-\Delta L) = -\frac{(2-\eta)V_{DX}}{L-\Delta L}. \quad (42)$$

From eqn (19), at the saturation point ($y = L-\Delta L$), the electron temperature is:

$$T_n(y = L-\Delta L) = T_0 + \frac{B}{A+2}(E(y = L-\Delta L))^2. \quad (43)$$

From eqn (7), at the saturation point ($y = L-\Delta L$), the electron velocity is

$$v_n(y = L-\Delta L) = \mu_s\left(\frac{T_n(y = L-\Delta L)}{T_0}\right)^{-0.5} E(y = L-\Delta L). \quad (44)$$

In the post-saturation region, the effective charge density is $n(y) = (I_D/Wv_n(y = L\text{-}\Delta L))$. Therefore from eqns (36, 37, 44) one obtains:

$$Q_{S2} = \frac{I_D\Delta L^2}{2Lv_n(y = L-\Delta L)}, \quad (45)$$

$$Q_{D2} = \frac{I_D}{v_n(y = L-\Delta L)}\left(\Delta L - \frac{\Delta L^2}{2L}\right). \quad (46)$$

Eqns (1–3, 32, 33, 40, 41, 45, 46) are closed-form analytical C_{SG} and C_{DG} formulas for the 0.1 μm NMOS device considering velocity overshoot.

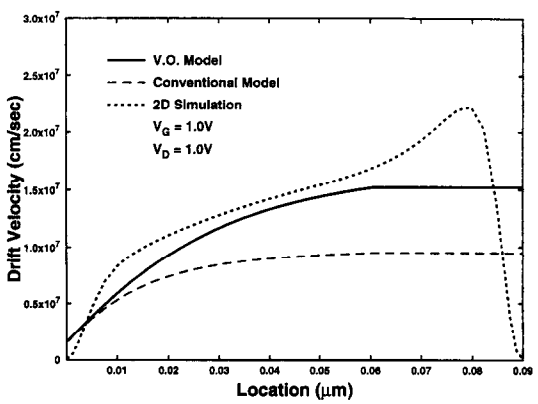

Fig. 1. Electron drift velocity distribution in the lateral channel direction of the NMOS device biased at $V_D = 1$ V and $V_G = 1.0$ V, according to 2 D simulation results, the analytical velocity overshoot model, and the conventional model, respectively. $\mu_0 = 450\ \mathrm{cm^2\,V^{-1}\,sec^{-1}}$.

Table 1. Parameters of the device under study

Parameter	Value
L	0.09 μm
V_{t0}	0.2 V
s	0.35
t_{ox}	75 Å
η	0.1
η_1	0.94
μ_0	450 $\mathrm{cm^2\,V^{-1}\,sec^{-1}}$
x_j	0.11 μm
σ	0.12

3. MODEL VERIFICATION

In order to evaluate the effectiveness of the analytical velocity overshoot model, the analytical model results for C_{SG} and C_{DG} have been compared to 2D simulation results[20]. As shown in Table 1, the NMOS device under study has an effective channel length of 0.09 μm, a gate oxide thickness of 75 Å and a S/D junction depth of 0.11 μm. The zero bias threshold voltage of the device is 0.2 V.

Figure 1 shows the electron drift velocity distribution in the lateral channel direction of the NMOS device biased at $V_D = 1$ V and $V_G = 1.0$ V, based on the 2D simulation results and on the analytical velocity overshoot model. $\mu_0 = 450\ \mathrm{cm^2\,v\,sec^{-1}}$. As shown in the figure, the electron drift velocity distribution of the model result is well correlated to the 2D simulation result. At $V_D = 1$ V and $V_G = 1.0$ V, in

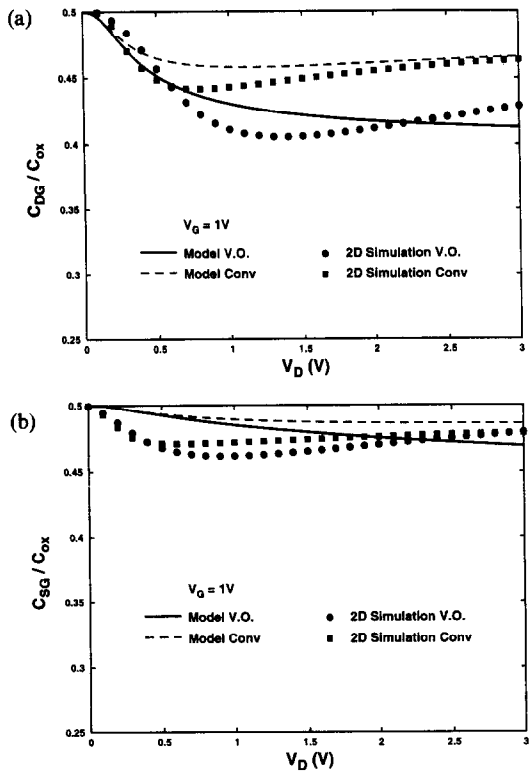

Fig. 2. (a) C_{DG} and (b) C_{SG} vs V_D of the NMOS device with a channel length of 0.09 μm, biased at $V_G = 1$ V, based on the analytical model considering velocity overshoot and without considering it, and 2D simulation results, respectively.

most parts of the lateral channel, the drift velocity is higher than the saturated velocity (10^7 cm sec^{-1}). Using the analytical velocity overshoot model, velocity overshoot behavior can be observed. However using the conventional model, velocity overshoot behavior cannot be identified.

Figures 2(a) and 2(b) show C_{DG} and C_{SG} vs V_D of the NMOS device (biased at $V_G = 1$ V) according to both analytical models and 2D simulation. As shown in the figures, at small V_D with and without considering velocity overshoot, a similar result can be observed for both C_{SG} and C_{DG}. When V_D becomes large, a difference in C_{SG} and C_{DG} with and without considering velocity overshoot becomes noticeable. Compared to C_{SG}, the difference in C_{DG} with and without considering velocity overshoot is larger. Specifically at large V_D, considering velocity overshoot C_{DG} degrades more. The trends in C_{DG} and C_{SG} predicted by the analytical model are confirmed by the 2D simulation results.

4. DISCUSSION

The larger decrease in C_{DG} when considering velocity overshoot can be understood by considering C_{DG1}, C_{DG2}, C_{SG1} and C_{SG2}, which in the pre-saturation region are defined as

$$C_{DG1} \equiv -\frac{\partial Q_{D1}}{\partial V_G}\frac{1}{WL}, \quad C_{SG1} \equiv -\frac{\partial Q_{S1}}{\partial V_G}\frac{1}{WL};$$

and in the post-saturation region as

$$C_{DG2} \equiv -\frac{\partial Q_{D2}}{\partial V_G}\frac{1}{WL}, \quad C_{SG2} \equiv -\frac{\partial Q_{S2}}{\partial V_G}\frac{1}{WL}.$$

Note that $C_{DG1} + C_{DG2} = C_{DG}$, $C_{SG1} + C_{SG2} = C_{SG}$.

Figures 3(a) and 3(b) show the normalized value of C_{DG1} and C_{DG2} and C_{SG1} and C_{SG2} vs V_D of the NMOS device, biased at $V_G = 1$ V, based on both analytical models. As shown in Fig. 3(a), when V_D is small, C_{DG1} for the pre-saturation region is much larger than C_{DG2} for the post-saturation region. When V_D becomes large, C_{DG2} for the post-saturation region is much larger than C_{DG1}. In the pre-saturation region, with and without considering velocity overshoot, C_{DG1} is identical. In contrast, in the post-saturation region, considering velocity overshoot, C_{DG2} is smaller when compared to the case without considering it. This is correlated to the results shown in Fig. 2(a). As shown in Fig. 3(b) regardless of V_D C_{SG1} for the presaturation region is always much larger than C_{SG2} for the post-saturation region. In the pre-saturation region, with and without considering

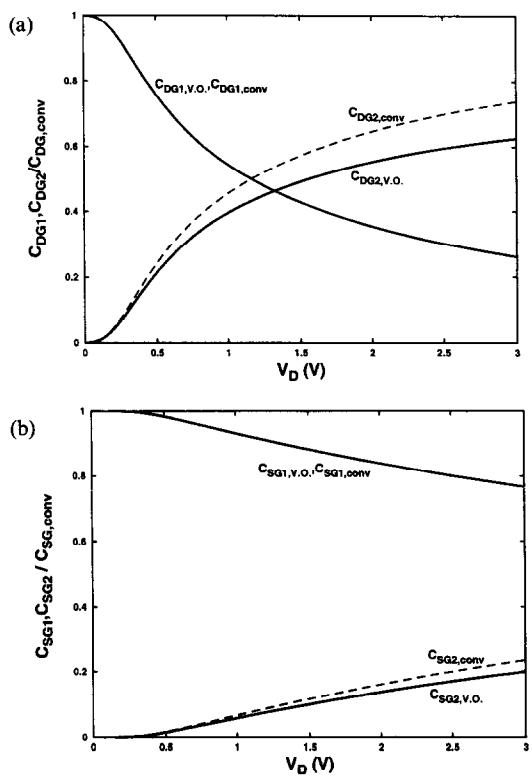

Fig. 3. (a) Normalized C_{DG1} and C_{DG2} and (b) normalized C_{SG1} and C_{SG2} vs V_D of the NMOS device with a channel length of 0.09 μm, biased at $V_G = 1$ V, based on the analytical model considering velocity overshoot and without considering it, respectively.

velocity overshoot, C_{SG1} is identical. In the post-saturation region, considering velocity overshoot C_{SG2} is smaller when compared to the case without considering it. From Figs 3(a) and 3(b), we learn that for C_{SG} the pre-saturation region is more important—C_{SG1} is more important than C_{SG2}. Considering velocity overshoot, in the post-saturation region, when V_D is large, C_{SG2} may become smaller than that without considering it. Since C_{SG1} of the presaturation region always dominates C_{SG}, at large V_D, the decrease in C_{SG2} of the post-saturation region when considering velocity overshoot only makes C_{SG} decrease a little bit. However, for C_{DG}, the post-saturation region can be more important—at large V_D, C_{DG2} is more important than C_{DG1}. Therefore at large V_D the decrease in C_{DG2} of the post-saturation region when considering velocity overshoot makes C_{DG} decrease much more when compared to the C_{SG} case. This explains the larger decrease in C_{DG} when considering velocity overshoot at large V_D when compared to the C_{SG} case. The decrease in C_{DG2} in the post-saturation region when considering velocity overshoot at large V_D is caused by a larger electron drift velocity in the post-saturation region.

5. CONCLUSION

In this article the impact of velocity overshoot on the source-gate and drain-gate capacitance in a 0.1 μm NMOS device has been discussed. As verified by 2D simulation results, based on the analytical capacitance model considering velocity overshoot, since a smaller amount of electrons exists in the channel region C_{SG} and C_{DG} show a smaller value when compared with the conventional model. As compared to the C_{SG} case, the larger decrease in C_{DG} when considering velocity overshoot at high V_D is the result of higher electron velocity in the post-saturation region.

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REFERENCES

1. A. Hori *et al.*, A 0.05 μm-CMOS with ultra shallow source/drain junctions fabricated by 5 keV ion implantation and rapid thermal annealing, *IEDM Tech. Dig.*, pp. 485–488 (1994).
2. Y. G. Chen, S. Y. Ma, J. B. Kuo, Z. Yu and R. W. Dutton, An analytical drain current model considering both electron and lattice temperatures simultaneously for deep submicron ultrathin SOI NMOS devices with self-heating, *IEEE Trans. Electron Devices*, pp. 899–906 (May 1995).
3. S. Y. Ma and J. B. Kuo, Concise analytical model for deep submicron NMOS devices with consideration of energy transport, *Jap. J. Appl. Phys.* **33,** 550–553 (1994).
4. Y. G. Chen, J. B. Kuo, Z. Yu and R. W. Dutton, An analytical drain current model for short-channel fully-depleted ultrathin silicon-on-insulator NMOS devices, *Solid-St. Electron.* (1995).
5. G. Baccarani and M. R. Wordeman, An investigation of steady-state velocity overshoot in silicon, *Solid-St. Electron.* **28,** 407–416 (1985).
6. J. G. Ruch, Electron dynamics in short channel field-effect transistors, *IEEE Trans. Electron Devices.* pp. 652–654 (May 1972).
7. N. G. Einspruch and G. Gildenblat, *Advanced MOS Devices Physics*, Academic Press: New York, Vol. 18, pp. 25–29 (1989).
8. R. S. Huang and P. H. Ladbrooke, The physics of excess electron velocity in submicron-channel FET's, *J. Appl. Phys.* **48,** 4791–4798 (1977).
9. T. Kobayashi and K. Saito, Two-dimensional analysis of velocity overshoot effects in ultrashort-channel Si MOSFET's, *IEEE Trans. Electron Devices* **32,** 788–792 (1985).
10. J. B. Kuo, Y. W. Chang and Y. G. Chen, An analytical velocity overshoot model for 0.1 μm N-channel metal-oxide-silicon (NMOS) devices considering energy transport, *Jap. J. Appl. Phys.* to be published.
11. D. E. Ward and R. W. Dutton, A charge-oriented model for MOS transistor capacitances, *IEEE J. Solid-State Circuits* **13,** 703–707 (1978).
12. T. Smedes and F. M. Klaassen, Effects of the lightly doped drain configuration on capacitance characteristics of submicron MOSFETs, *IEDM Dig.*, pp. 197–200 (1990).
13. H. Iwai, M. R. Pinto, C. S. Rafferty, J. E. Oristian, and R. W. Dutton, Velocity saturation effect on short-channel MOS transistor capacitance, *IEEE Electron Device Lett.* **6,** 120–122 (1985).
14. E. W. Greeneich, An analytical model for the gate capacitance of small-geometry MOS structures, *IEEE Trans. Electron Devices* **30,** 1838–1839 (1983).
15. R. Stratton, Diffusion of hot and cold electrons in semiconductor barriers, *Phys. Rev.* **126,** 2002–2014 (1962).
16. F. M. Klaassen, A MOS model for computer-aided design, *Philips Research Reports* **31,** 71–83 (1976).
17. D. M. Caughey and R. F. Thomas, Carrier mobilities in silicon empirically related to doping and field, *Proc. IEEE* **55,** 2192–2193 (1967).
18. C. Jacoboni, C. Canali, G. Ottaviani and A. A. Quaranta, A review of some charge transport properties of silicon, *Solid-St. Electron.* **20,** 77–89 (1977).
19. Y. G. Chen and J. B. Kuo, A unified triode/saturation closed-form analytical model with a smooth continuity in the output conductance suitable for CAD of VLSI circuits using deep sub-0.1 μm NMOS devices, *IEEE Trans. CAD of IC*, to be published.
20. *MEDICI: Two-Dimensional Semiconductor Device Simulation*, Technology Modeling Associates, Inc.