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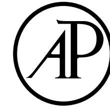

An extremely low offset voltage AlInAs/GaInAs heterostructure-emitter bipolar transistor

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A new $Al_{0.48}In_{0.52}As/Ga_{0.47}In_{0.53}As$ heterostructure-emitter bipolar transistor (HEBT) with a very low offset voltage of 40 mV has been fabricated by molecular beam epitaxy. From the theoretical analysis and experimental results, it is found that a 500-Å thick emitter used in the studied device can effectively eliminate the potential spike at the N–AlInAs/n–GaInAs heterointerface. However, a degenerate current gain of about 25 is obtained, attributed to the increase of recombination current at the neutral-emitter regime. This is caused by the short hole diffusion length of GaInAs, which reduces the emitter injection efficiency. Due to the small surface recombination velocity, the emitter edge-thinning design is not essential to improve the device performance of our proposed AlInAs/GaInAs HEBT.

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Key words: heterostructure-emitter bipolar transistor (HEBT), potential spike, neutral-emitter recombination current.

1. Introduction

Heterojunction bipolar transistors (HBTs) have attracted remarkable interest for microwave and digital circuit applications due to their high-speed and high-current capabilities [1–3]. The basic concept of HBT is that a wide-gap emitter layer is employed to introduce an energy barrier for limiting the injection of holes from base to emitter regime. Therefore, the principle benefit of HBT is not only the ability to achieve high emitter injection efficiency and hence high current gain, but also the freedom to change doping levels in the emitter and base without the significant constraint of an injection efficiency consideration. However, the precise alignment of the compositional junction to the doping junction, which is essential for the high-performance HBTs, is difficult to achieve due to the considerable out-diffusion of p-type dopants. Furthermore, the large collector–emitter (CE) offset voltage ΔV_{CE} resulting from the difference in turn-on voltage between the base-collector (BC) homojunction and the base-emitter (BE) heterojunction is observed which results in undesirable power consumption [4]. In order to overcome these problems, the heterostructure-emitter bipolar transistors (HEBTs) have been proposed and fabricated successfully in [5, 6]. For the HEBTs, the 'effective' BC and BE junctions can be considered as a homojunction. This yields the nearly equal turn-on voltage between these two junctions and the extremely small offset voltage may be obtained.

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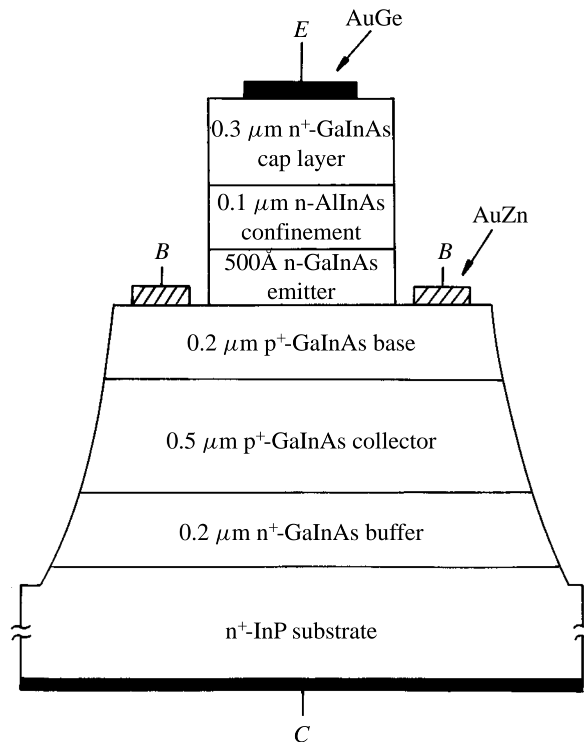

Fig. 1. Schematic cross-section of the studied AlInAs/GaInAs HEBT.

Recently, AlGaAs/GaAs and InGaP/GaAs HEBTs have attracted high-current gain and high-frequency applications [6–9]. Liu and Lour [6] successfully fabricated an AlGaAs/GaAs HEBT with the current gain of 180 and offset voltage of 80 mV. Chen *et al.* [7] reported an AlGaAs/GaAs HEBT with a current gain of 720 and a low offset voltage of 49 mV by using the emitter-edge thinning design. In addition, Yang *et al.* [9] first fabricated and reported the high-performance InGaP/GaAs HEBTs. They demonstrated the significant lower surface recombination current and high current gain at high collector current density with an InGaP passivation layer. These results show a good potential for the practical applications. However, the InP-based AlInAs/GaInAs HEBT has not been reported. In this paper, we will fabricate and demonstrate a new AlInAs/GaInAs HEBT to achieve a very small offset voltage.

2. Experiments

The studied $Al_{0.48}In_{0.52}As/Ga_{0.47}In_{0.53}As$ HEBT was grown by molecular beam epitaxy (MBE) on a (100)-oriented n^+-InP substrate, as shown in Fig. 1. The epitaxial layers consisted of a 0.2-μm thick n^+-GaInAs buffer layer ($n^+ = 5 \times 10^{18}$ cm^{-3}), a 0.5-μm thick n^--GaInAs collector layer ($n^- = 5 \times 10^{16}$ cm^{-3}), a 0.2-μm thick p^--GaInAs base layer ($p^+ = 5 \times 10^{18}$ cm^{-3}), a 500-Å thick n-GaInAs emitter layer ($n = 5 \times 10^{17}$cm^{-3}), a 0.1-μm thick n-AlInAs confinement layer ($n = 5 \times 10^{17}$ cm^{-3}), and a 0.3-μm thick n^+-GaInAs cap layer ($n^+ = 3 \times 10^{18}$ cm^{-3}). The n- and p-type dopants used here were Si and Be. After MBE growth, wet-etching and photolithographic processes were used to define the emitter and base regions. Ohmic contacts were performed by alloying evaporated AuGe and AuZn metals for the n-type emitter, collector, and p-type base, respectively. The emitter and collector areas are 4.9×10^{-5} and 5×10^{-4} cm^{-2}, respectively.

Fig. 2. The conduction current components of the studied structure.

3. Theoretical analysis

For the typical HEBTs, a nearly unit emitter injection efficiency γ is achieved. However, for our studied device, the recombination current in the neutral-emitter regime can not be neglected completely, due to the insertion of the n-GaInAs emitter layer between the N-AlInAs confinement and the p^+-GaInAs base layer. Hence, the variations of varied recombination current components should be investigated.

Figure 2 illustrates the conduction current components of the studied structure without considering the series resistance and high-level injection effect. The hole current consists of the thermal-diffusion current (J_{hd}), the neutral-emitter recombination current (J_{hn}), the space-charge region recombination current J_{SCR}), the base surface recombination current (J_{BS}), and the recombination current in the bulk quasineutral base (J_{Bb}). The total base current J_B is

$$J_B = J_{hd} + J_{hn} + J_{SCR} + J_{Bs} + J_{Bb}. \tag{1}$$

The hole thermal-diffusion current J_{hd} is dominated by:

$$J_{hd} = J_{h1}\left(1 - \frac{W_n^2}{2L_p^2}\right)\exp\left(-\frac{\Delta Ev}{KT}\right) \tag{2}$$

with

$$J_{h1} = \frac{qD_p n_{ie}^2}{Q_E}\exp\left(\frac{-qV_1}{KT}\right)\left[\exp\left(\frac{qV_{BE}}{KT}\right) - 1\right] \tag{3}$$

where W_n, is the neutral-emitter thickness, L_p is the hole diffusion length in the neutral-emitter region and ΔEv is the valence band discontinuity between the confinement and emitter layer emitter. D_p, Q_E, and n_{ie} are the hole diffusion coefficient, emitter Gummel number, and effective emitter intrinsic concentration, respectively. V_1 is the portion of external voltage V_{BE} across the heterojunction only. The neutral-emitter recombination current J_{hn} is

$$J_{hn} = J_{h1}\left(\frac{W_n^2}{2L_p^2}\right). \tag{4}$$

The space-charge region recombination current J_{SCR} can be approximated as

$$J_{SCR} = q\int_{-X1}^{0} U_{SCRE}\,dx + q\int_{0}^{X2} U_{SCRB}\,dx \tag{5}$$

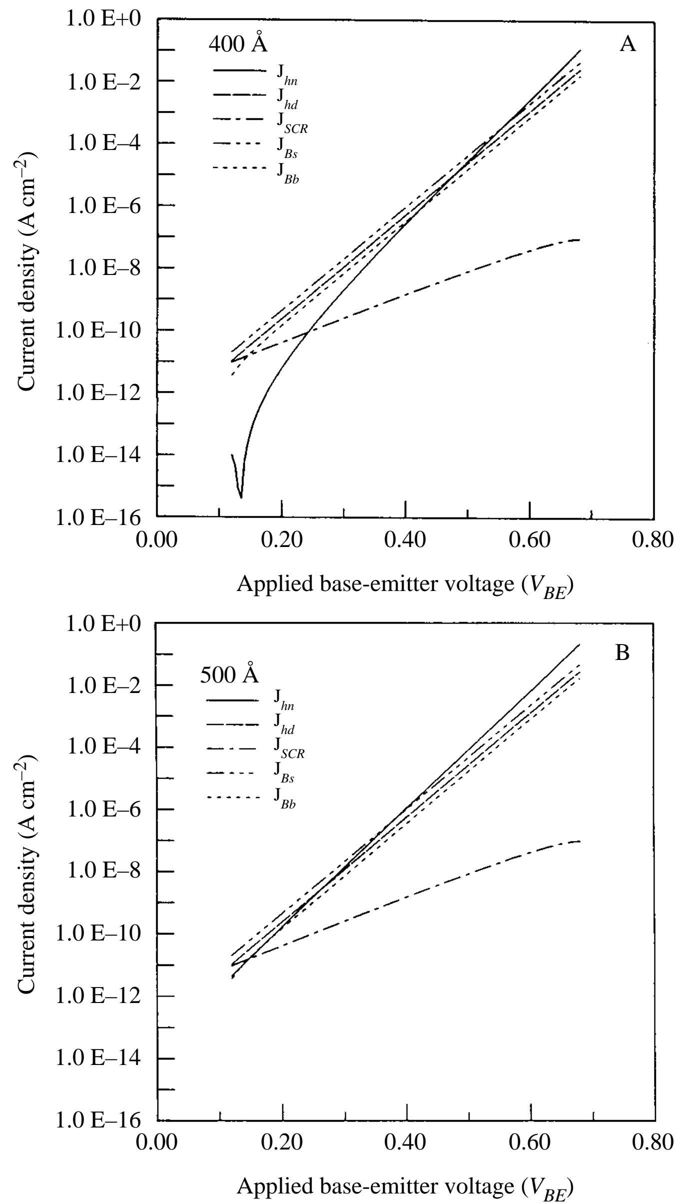

Fig. 3. The calculated base component currents versus V_{BE} voltage for: A, the device LT1 (400 Å); B, device LT2 (500 Å); C, device LT3 (700 Å); D, the device LT4 (1000 Å).

with

$$U_{SCRE} = 0.5\sigma_n V_n N_t n_{ie} \exp\left(\frac{V_{BE}}{2V_T}\right) \tag{6}$$

and

$$U_{SCRB} = 0.5\sigma_n V_n N_t n_{ib} \exp\left(\frac{V_{BE}}{2V_T}\right) \tag{7}$$

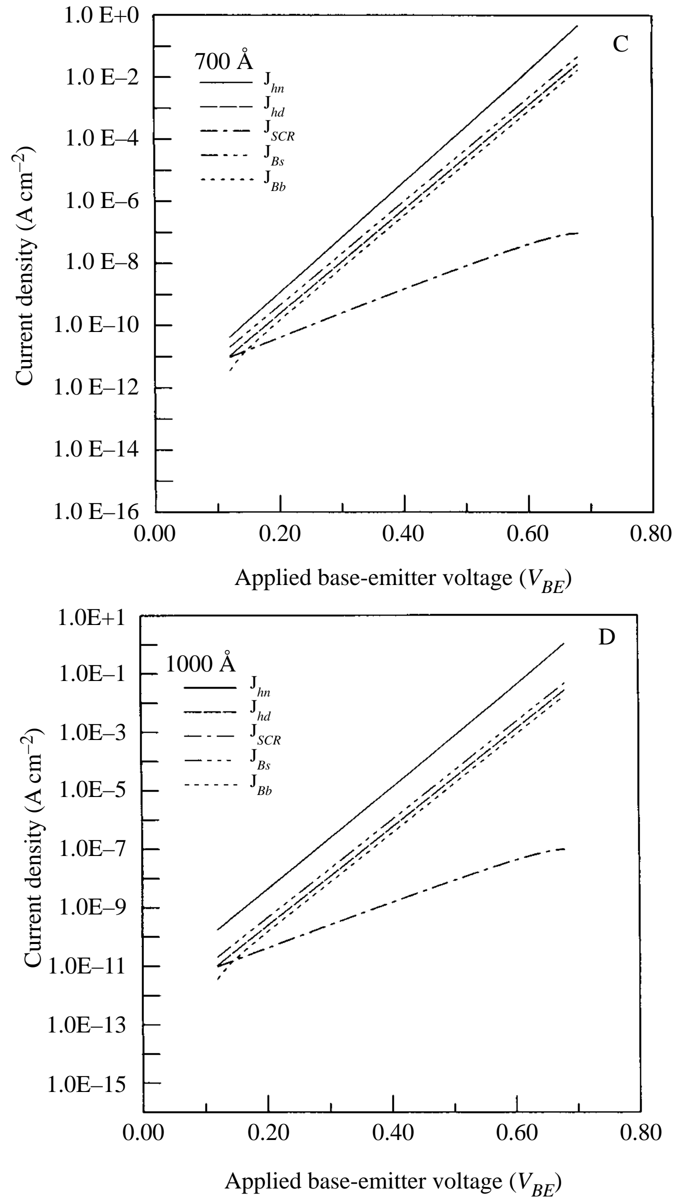

Fig. 3. Continued.

where $X1$ and $X2$ are the depletion thickness at the emitter and base region, respectively. σ_n, V_n, N_t, n_{ie}, and n_{ib} are the capture cross-section, free-carrier thermal velocity, trapping density, emitter effective intrinsic concentration, and base effective intrinsic concentration, respectively. The first and second terms on the right hand side of eqn (5) are the space-charge recombination current at the emitter and base region, respectively.

The base surface recombination current J_{BS} can be expressed as

$$J_{BS} = \frac{I^*}{A_E} \exp\left(\frac{V_{BE}}{V_T}\right) \tag{8}$$

where I^* is an empirical parameter, and A_E is the emitter junction area. The recombination current in the bulk quasineutral base J_{Bb} can be determined by

$$J_{Bb} = J_{nE1} \frac{W_b^2}{2Le^2} \tag{9}$$

where J_{nE1} is the electron current at the base edge of the depletion region. W_B and Le are the neutral-base thickness and electron diffusion length, respectively.

In contrast, the electron current at the base edge of the depletion region can be expressed as

$$J_{en1} = \frac{qD_e n_{ib}^2}{pLe} \left[\exp\left(\frac{q(V_{BE} - V_1)}{KT}\right)\right] \coth \frac{W_B}{L_e} \tag{10}$$

where D_e is the electron diffusion coefficient. The electron current in the collector region J_C is

$$J_C = J_{en1} - J_{Bb} \tag{11}$$

with

$$J_{en1} = J_{EN} - J_{SCR} - J_{BS} - J_{hn} \tag{12}$$

where J_{EN} is the emitter electron current. Then the emitter and collector current can be expressed as

$$I_E = A_e(J_{EN} + J_{hd} + J_{hn}) \tag{13}$$

and

$$I_C = A_E J_C \tag{14}$$

$$I_B = I_E - I_C. \tag{15}$$

The emitter electron injection efficiency γ and the current gain β can be defined as

$$\gamma = \frac{A_E J_{en1}}{I_E} \tag{16}$$

and

$$\beta = \frac{I_C}{I_B}. \tag{17}$$

The collector-emitter offset voltage ΔV_{CE} leading to the power consumption is also an important factor for the transistor performances. The ΔV_{CE} value could be determined as

$$\Delta V_{CE} = I_B R_E + \frac{KT}{q} \ln\left(\frac{A_C}{A_E}\right) + \frac{KT}{q}\left(\frac{J_{CS}}{\alpha_F J_{ES}}\right) \tag{18}$$

where R_E is the emitter series resistance, A_C is the collector area, α_F is the forward common-base current gain, J_{CS} and J_{ES} are the reverse saturation current density of collector and emitter junctions respectively, and

$$J_{ES} = A^* T^2 \exp\left(-\frac{q\phi_{BN} + q\Delta V_E}{KT}\right) \tag{19}$$

where A^* is the Richardson constant, ϕ_{BN} and ΔV_e are the barrier height from Fermi level to conduction band minimum in the base regime and the potential spike located at the EB junction, respectively. By inserting an n-GaInAs emitter layer between the N-AlInAs confinement and the p^+-GaInAs base layer, the potential

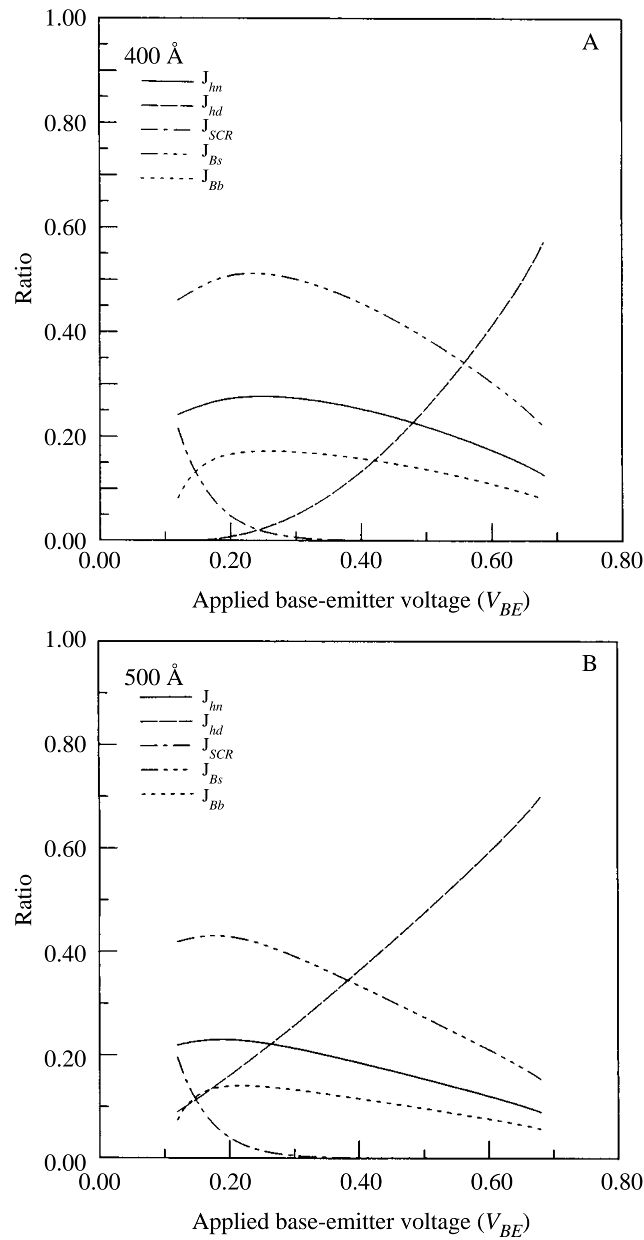

Fig. 4. The ratio of the base component current to the total base current versus V_{BE} voltage. A, the device LT1 (400 Å); B, the device LT2 (500 Å); C, the device LT3 (700 Å); D, the device LT4 (1000 Å).

spike is expected to be removed and the offset voltage may be reduced. A minimum value of emitter layer thickness could be calculated by solving the Poisson equation as

$$a = \sqrt{\frac{2\varepsilon \Delta E_c}{q^2 N_D}\left(\frac{N_A}{N_A + N_D}\right)} \tag{20}$$

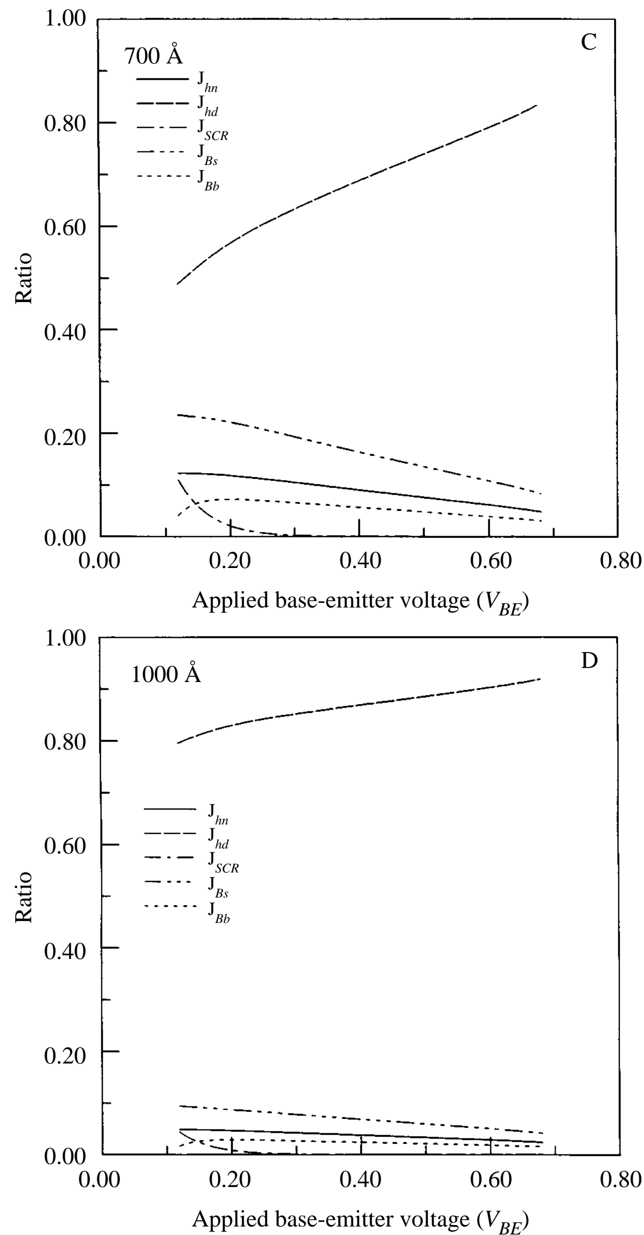

Fig. 4. Continued.

where ΔE_c, N_D, and N_A are the conduction band discontinuity between the confinement and emitter layer, emitter, and base layer concentration, respectively. ε is the permittivity of base layer. From calculation, the value of a is 390 Å for the AlInAs/GaInAs HEBT. So, a 500 Å thick emitter layer is sufficient to eliminate the potential spike at small V_{BE} voltage and reduce the offset voltage for our studied devices.

By considering the influence of the recombination current, the different emitter thicknesses, such as 400 Å

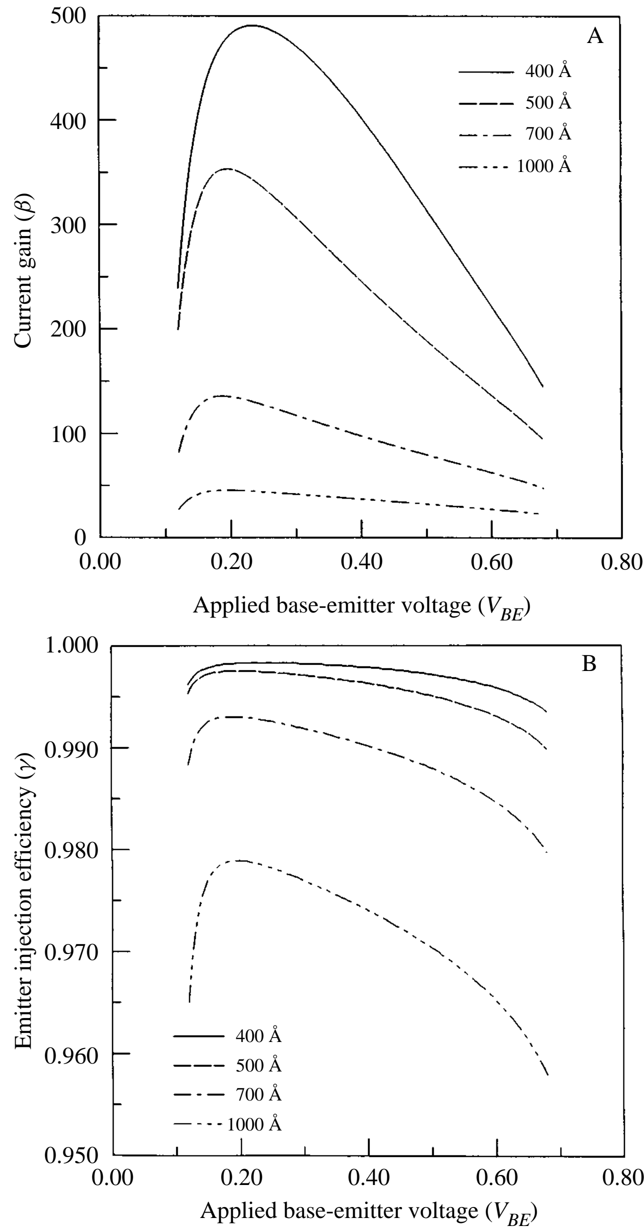

Fig. 5. A, The calculated β versus V_{BE} for the studied device. B, The calculated γ versus V_{BE} for the studied device.

(device LT1), 500 Å (device LT2), 700 Å (device LT3), and 1000 Å (device LT4), are employed in the theoretical analysis. The calculated base component currents versus V_{BE} voltage for the AlInAs/GaInAs HEBTs are shown in Fig. 3. Generally, the base component currents are increased linearly by increasing the V_{BE} voltage. Furthermore, J_{hn} increases with the increase of the emitter thickness, while the other component currents maintain constant. The dependence of V_{BE} voltage on the ratio of the component base current to

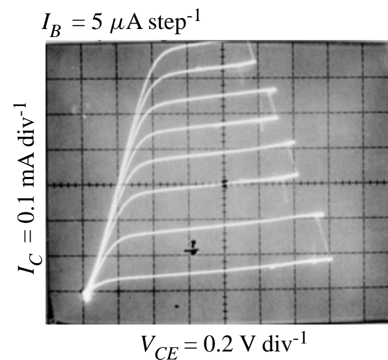

Fig. 6. The common-emitter I–V characteristics of the studied device.

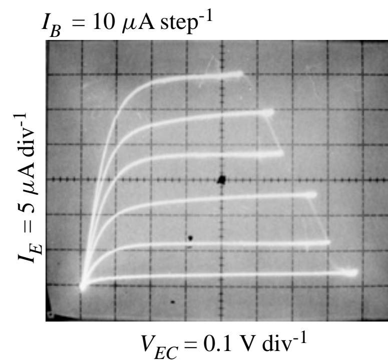

Fig. 7. The experimental I–V characteristics under the inverted operation mode.

the total base current are illustrated in Fig. 4. Similarly, for the devices with large emitter thicknesses, the neutral-emitter recombination current is an important component for determining the base current which could increase the total base current and result in the decrease of collector current. Figure 5 illustrates the calculated β and γ versus V_{BE} for the studied devices. It is clearly found that a maximum current gain of 490 and a large emitter injection efficiency can be obtained for the device LT1 ($W_E = 400$ Å). On the other hand, a maximum current gain of 44 and a low emitter injection efficiency are found for the device LT4 ($W_E = 100$ Å). This is due to the fact that the larger emitter thickness will introduce the more neutral-emitter recombination current. This certainly results in degraded current gain and emitter injection efficiency. Particularly, the phenomenon is obvious for the short hole diffusion length material under the applied large V_{BE} biased condition.

4. Experimental results and discussions

Figure 6 shows the experimental common-emitter current–voltage (I–V) characteristics of the studied device. The maximum current gain of 25 and an extremely low offset voltage of 40 mV are obtained. Note that the current gain of AlInAs/GaInAs HEBT decreases by increasing the base current I_B. It is known that from the above analysis there are a number of holes which are recombined in the neutral-emitter region. On the other hand, due to the low surface recombination velocity of the GaInAs layer, the potential spike is eliminated and the offset voltage ΔV_{CE} can be reduced simultaneously. In addition, the experimental two-terminal I–V

characteristic shows that the turn-on voltage difference between the EB and BC junction is about 40 mV. This value is consistent with the ΔV_{CE} obtained from Fig. 4. Figure 7 shows the output I–V characteristics under the inverted operation mode. The magnitude of reverse current gain, $\beta_r = \Delta I_E/\Delta I_B$ is about 0.42 at $I_B = 10\ \mu$A and $V_{EC} = 0.5$ V. Moreover, the I–V curves are very smooth, i.e. the reach-through effect is not found. The practical potential spike at emitter side ΔV_E may be expressed as

$$\Delta V_{CE} = \Delta V_E + \frac{KT}{q} \ln \frac{1}{\alpha_e \gamma_C} \tag{21}$$

where α_E is the forward base transport and γ_C is the collector injection efficiency. From Fig. 7, the product of $\alpha_E \gamma_C$ is about 0.3. Thus, the potential spike ΔV_E is only of 10 mV. This value can be neglected in the practical application.

From the viewpoint of the transistor performances, the emitter thickness of 500 Å should be reduced to 400 Å or less to achieve a higher current gain for the studied AlInAs/GaInAs HEBT. It is known that the experimental results are in good agreement with the theoretical analysis. Consequently, with an appropriate design on device structure, e.g. the small W_E, a better device performance may be obtained.

5. Conclusions

In summary, a new AlInAs/GaInAs HEBT with an extremely low offset voltage of 40 mV has been fabricated successfully and demonstrated. From the theoretical analysis and experimental results, it is known that a 500 Å thick emitter inserted between the AlInAs confinement layer and the GaInAs base layer can effectively eliminate the potential spike of EB junction. The current gain is degraded due to the large neutral-emitter current effect under large V_{BE} bias. Hence, the emitter thickness should be reduced. Furthermore, owing to the low surface recombination current of the GaInAs layer, the emitter edge-thinning design is not essential to improve the device performances.

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