

A Comprehensive Study of Inversion Current in MOS Tunneling Diodes

C.-H. Lin, B.-C. Hsu, M. H. Lee, and C. W. Liu, *Senior Member, IEEE*

Abstract—The gate current of MOS tunneling diodes biased at inversion region with different substrate doping is investigated. For p-type substrate ($1\text{--}5 \Omega\text{-cm}$) devices, the tunneling diode works in the deep depletion region and the inversion current is dominated by the thermal generation rate of minority electrons via traps at Si/SiO₂ interface and in the deep depletion region. The activation energy is approximately equal to half of the silicon bandgap independent of gate voltage. For devices on p⁺ substrate ($0.01\text{--}0.05 \Omega\text{-cm}$), the band-to-traps tunneling and band-to-band tunneling are the dominating current components at inversion bias, and reveal a strong field dependence and a weak temperature dependence. The band-to-traps and band-to-band current components are even more significant in the devices on the p⁺⁺ substrate ($0.001\text{--}0.0025 \Omega\text{-cm}$). Finally, the effects of temperature and light illumination on inversion current of MOS tunneling diodes will be also discussed.

Index Terms—Inversion current, MOS tunneling diode, ultrathin oxide.

I. INTRODUCTION

FOR future deep-submicron ULSI technology, it is expected that the SiO₂ gate dielectric will be less than 3 nm for a technology node beyond $0.13 \mu\text{m}$ [1]. The gate current becomes significant for MOS diodes with such ultrathin oxide. This gate current has been utilized for many novel applications, such as light-emitting diodes (LEDs) [2], [3], and photodetectors [4], although the significant gate current is a problematic issue in ULSI circuits. Due to the capability of carrier supply from the source and drain, the gate currents biased at accumulation region and at inversion region have similar behaviors in MOS-FETs [5]. While, due to the lack of carrier supply, the inversion current is quite different from the accumulation current for MOS tunneling diode. The mechanisms of accumulation current of the MOS tunneling diodes have been extensively studied [6]–[8]. The mechanism of inversion current is not yet well understood in the MOS diodes, although this inversion current of MOS diodes on heavily doped substrate is similar to gate-induced drain leakage current (GIDL) [9], [10]. Recently, Ghetti

et al. investigated the inversion current of MOS diodes with thick oxide ($\sim 6 \text{ nm}$) based on tunneling mechanisms [11]. A theoretical model including band-to-band tunneling, interface state tunneling, carrier generation through the interface, carrier generation in the depletion region, and diffusion current have been reported [12]. For ultrathin oxide ($< 3 \text{ nm}$), the carrier tunneling rate through oxide is sufficient large, and the carrier generation rate is the bottleneck for current transport. In this paper, we demonstrate that three carrier-generation mechanisms are responsible for the inversion current of NMOS tunneling diodes. The mechanisms are Shockley-Read-Hall (SRH) generation, band-to-band tunneling, and band-to-traps tunneling. The doping level of substrate determined the dominant mechanism.

II. EXPERIMENT

The ultrathin gate oxide of the NMOS diode was grown by rapid thermal oxidation (RTO) on p-type silicon (100) substrate with three different doping levels, $1\text{--}5 \Omega\text{-cm}$ (labeled as “p”), $0.01\text{--}0.05 \Omega\text{-cm}$ (p⁺), and $0.001\text{--}0.0025 \Omega\text{-cm}$ (p⁺⁺). The gas flows were 500 sccm nitrogen and 500 sccm oxygen at reduced pressure. Before the growth of RTO oxide, the sample was cleaned by a HF dip and *in-situ* hydrogen bake at 1000°C for 2 min. After the growth of the ultrathin gate oxide, the sample was *in-situ* annealed in hydrogen and nitrogen for 10 min each at 900°C . The oxide thickness was measured by ellipsometry. NMOS diodes had Al gate electrodes with various circular areas defined by photolithography. The temperature dependence of current-voltage ($I\text{-}V$) characteristic was performed on a low-leakage hot chuck. Device temperature was set using the hot chuck before the $I\text{-}V$ measurements were conducted. The photocurrent and its temperature dependence are also measured by using metal halide lamp and the hot chuck.

III. CARRIER GENERATION MODELS

The inversion tunneling current was simulated by a self-coded program method based on the conventional SRH model, band-to-traps tunneling model, and band-to-band tunneling model. The band profile was determined by conventional Poisson’s equation.

A. Shockley-Read-Hall (SRH) Model

For the MOS devices with oxide thickness less than 3 nm, the tunneling rate of the minority carrier through the oxide is sufficiently effective at large gate bias. Therefore, the current is dominated by the minority carrier generation rate via traps at

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Si/SiO₂ interface and in the deep depletion region. The conventional SRH recombination model, which determines the generation rate of electron-hole pairs, can be described by [13]

$$U = \frac{\sigma_p \sigma_n v_{th} (pn - n_i^2) N_t}{\sigma_n [n + N_c \exp(-\frac{E_c - E_i}{kT})] + \sigma_p [p + N_v \exp(-\frac{E_v - E_i}{kT})]} \quad (1)$$

$$= \frac{(pn - n_i^2)}{\tau_p [n + n_i \exp(-\frac{E_T - E_i}{kT})] + \tau_n [p + n_i \exp(\frac{E_T - E_i}{kT})]} \quad (2)$$

where

v_{th} thermal velocity;

N_c and N_v state densities of the conduction band and the valance band, respectively;

n_i intrinsic carrier density;

E_T trap energy level;

σ_n and σ_p capture cross sections of the traps for electrons and holes, respectively;

n and p electron and hole densities, respectively;

τ_n and τ_p lifetime times of electron and hole, respectively.

The inversion current from SRH mechanism J_{SRH} is determined by the integration of the thermal generation rate over the whole deep depletion region and interface states energy level, which is given by

$$J_{SRH} = q \cdot \int_0^W U dx + q \cdot \int_{E_v}^{E_c} U_{Dit} dE \quad (3)$$

where

W width of the deep depletion region;

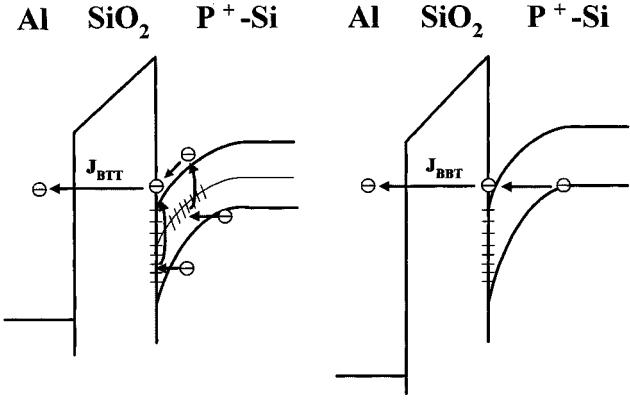
U thermal generation rate of electrons in deep depletion region;

U_{Dit} thermal generation rate of electrons via interface states with the assumption that Dit is uniformly distributed in the bandgap.

Only one trap level is considered in the depletion region during the calculation of the electron generation rate in the depletion region.

B. Band-to-Traps Tunneling Model

For p⁺ and p⁺⁺ substrate devices, owing to high doping concentration, which causes the shrinkage of the depletion region width, the band-to-traps (bulk traps and interface states) tunneling and band-to-band tunneling become the dominated mechanisms of the inversion current. At small gate bias, the band-to-traps tunneling model dominates the tunneling current due to small silicon surface bending (< 1.1 eV), as shown in Fig. 1(a). However, when gate bias is large enough to have surface band bending larger than 1.1 eV, the band-to-band tunneling [Fig. 1(b)] becomes more significant than band-to-traps tunneling. Both the models have voltage dependence on the tunneling current, while the previous SRH model of devices on p substrates has a relatively weak voltage dependence. Hurkx *et al.* have proposed a modified recombination model which includes both hole tunneling and electron tunneling in heavily



(a)

(b)

Fig. 1. Schematic band diagram of current transport mechanisms: (a) band-to-traps (bulk traps and interface states) tunneling and (b) band-to-band tunneling.

doped gated-diodes [14], [15], and the generation rate of electrons via traps $G_{trap}(x)$ is given by

$$G_{trap}(x) = (1 + \Gamma(x))U_{SRH}(x) \quad (4)$$

where $U_{SRH}(x)$ is the conventional SRH generation rate, and $\Gamma(x)$ is given by

$$\Gamma = 2\sqrt{3\pi} \frac{|F|}{F_\Gamma} \exp(F/F_\Gamma)^2 \quad (5)$$

with

$$F_\Gamma = \frac{\sqrt{24m^*(kT)^3}}{q\hbar} \quad (6)$$

where F is the local electric field of silicon, and the m^* is the effective mass of carriers. Some electrons tunnel from valance band to the most active bulk traps in the depletion region (located near the middle of bandgap), jump up to conduction band, and then tunnel to Al electrode. Some electrons near the Si/SiO₂ interface will tunnel from valance band to interface states directly, instead of tunneling to bulk traps. For the weak electric field, i.e., $F \ll 10^5$ V/cm at room temperature, Γ is much less than 1, and (4) will reduce back to the conventional SRH model [13]. Therefore, the band-to-traps tunneling current J_{BTT} is given by

$$J_{BTT} = q \cdot \int_0^W G_{trap}(x) dx + q \cdot \int_{E_v}^{E_c} G_{Dit} dE. \quad (7)$$

On the right-hand side, the first integration term represents the component of band-to-bulk traps tunneling, and the second term represents the component of band-to-interface trap tunneling. There is no position integral in the second term, since there is one-to-one correspondence between interface trap energy and the position from which the electrons tunnel.

C. Band-to-Band Tunneling Model

As gate bias larger than 2 V, the band-to-band tunneling starts to dominate the inversion tunneling current. In MOS tunneling diodes with heavily doped substrate, the carrier transport

TABLE I
LIST OF THE PARAMETERS USED IN SIMULATION

		p substrate	p ⁺ substrate	p ⁺⁺ substrate
Device parameters	Doping Concentration (1/cm ³)	1x10 ¹⁶	2.4x10 ¹⁸	1x10 ²⁰
	Oxide Thickness (nm)	1.8	1.7	1.3
	Device Area (1/cm ²)	3x10 ⁻⁴	3x10 ⁻⁴	3x10 ⁻⁴
SRH	Lifetime, τ _n =τ _p (sec)	1.2x10 ⁻⁶		
	Interface states,Dit (1/cm ² ·eV)	10 ¹¹		
Band-to-traps tunneling	effective mass m* (kg)	0.19 m ₀ (m ₀ =0.911x10 ⁻³⁰ kg)		
Band-to-band tunneling	effective mass m* (kg)	0.19 m ₀ (m ₀ =0.911x10 ⁻³⁰ kg)		

mechanism is similar to that of GIDL in MOSFET, which is attributed to band-to-band tunneling near the gate-to-drain overlap region. Wu *et al.* have proposed a new quasi-two-dimensional (quasi-2-D) model for band-to-band tunneling current [16]. Neglecting the lateral electric field effect, the band-to-band tunneling current J_{BBT} can be attained by integrating the tunneling rate $P(E_{si})$ through the whole depletion region, and is given by

$$J_{BBT} = q \cdot \int_0^W P(E_{si}) dx \\ = q \cdot \int_{E1}^{E2} P(E_{si}) \cdot \frac{dx}{dE_{si}} \cdot dE_{si} \quad (8)$$

where tunneling rate $P(E_{si})$ can be described as

$$P(E_{si}) = \frac{q^2 m^{1/2} E_{si}^2}{18\pi\hbar^2 E_g^{1/2}} \cdot \exp\left(-\frac{\pi m^{1/2} E_g^{3/2}}{2\hbar q E_{si}}\right) \quad (9)$$

where

- E_g silicon bandgap;
- E_{si} electric field in the depletion region;
- m electron effective mass.

Therefore, the band-to-band tunneling current is strongly dependent on electric field. The bandgap dependence on temperature is used to simulate the temperature dependence of band-to-band tunneling current. The silicon bandgap is given by [17]

$$E_g(T) = E_g(0) - \frac{\alpha \cdot T^2}{(T + \beta)} \quad (10)$$

where

- $E_g(0) = 1.17$;
- $\alpha = 4.74 \times 10^{-4}$;
- $\beta = 636$ for silicon.

Silicon bandgap decreases at high temperature, and thus, the band-to-band tunneling current increases as temperature increases.

The parameters of SRH, band-to-traps tunneling, and band-to-band tunneling models used in the simulation are listed in Table I.

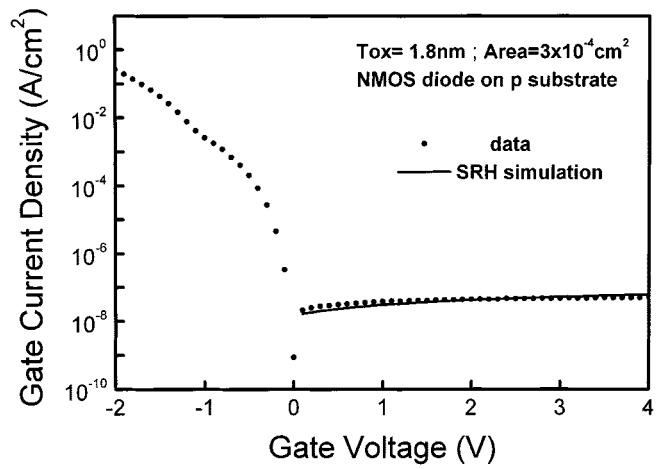


Fig. 2. $I-V$ curve of an NMOS diode on p substrate with SRH simulation results.

IV. COMPARISON OF SIMULATIONS AND EXPERIMENTAL RESULTS

Fig. 2 shows the $I-V$ curve of an Al/1.8 nm oxide/p-Si diode with an area of 3×10^{-4} cm². The simulated inversion tunneling current based on SRH model agrees well with the measured curve, and the inversion current is relatively constant in log scale. For ultrathin oxide device, the tunneling rate is controlled by the oxide voltage, which causes the direct tunneling of electrons from silicon to Al electrode. In NMOS tunneling diode, as positive gate bias increases, the oxide voltage increases very slightly, and most gate voltage drops on silicon with the formation of deep depletion region [4]. Therefore, the tunneling current is limited by the thermal generation rate of electrons in deep depletion region and at Si/SiO₂ interface, and can be simulated by conventional SRH generation/recombination model.

The $I-V$ curve of an Al/1.7 nm oxide/p⁺-Si diode with an area of 3×10^{-4} cm² is shown in Fig. 3. There is an enormous disparity with the previous device on p substrate. The tunneling current reveals strong field dependence and a kink around 1.7 V, indicating the transition between band-to-traps tunneling and band-to-band

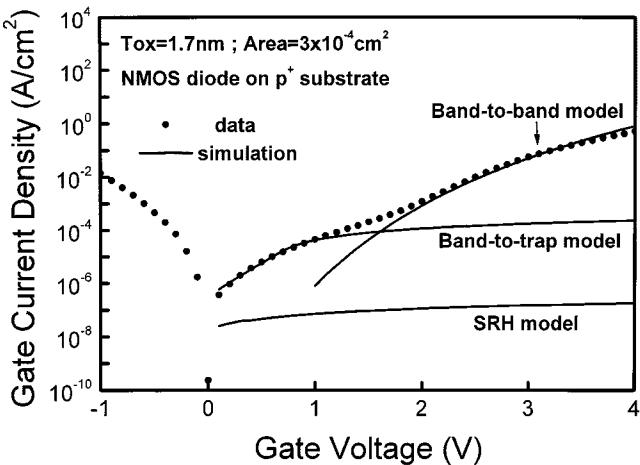


Fig. 3. $I-V$ curve of an NMOS diode on p^+ substrate with SRH, band-to-traps tunneling, and band-to-band tunneling simulation results.

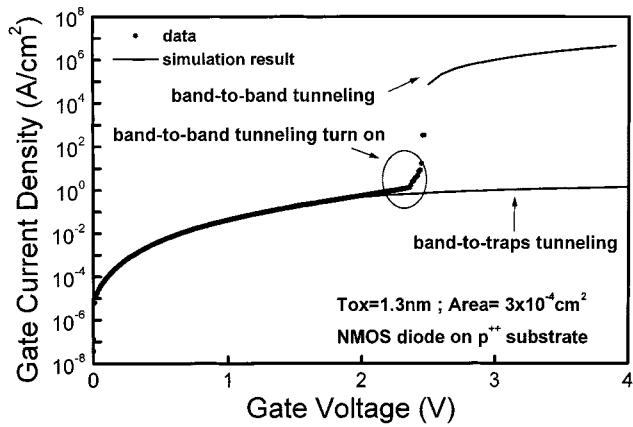


Fig. 4. $I-V$ curve of an NMOS diode on p^{++} substrate with simulation results.

tunneling. At positive gate bias smaller than 1.7 V, the generation rate of electrons is dominated by electrons tunneling from valance band to traps (bulk traps and interface traps), and then jumping up to conduction band. However, when gate bias is larger than 1.7 V (the surface band bending is larger than the bandgap), the generation of electrons is mainly due to electron tunneling from valance band to conduction band directly. The simulation results of band-to-traps tunneling and band-to-band tunneling give an excellent fit to the experimental data. For comparison, the SRH component is also shown in Fig. 3 and is negligible, as compared to the other two components.

Fig. 4 shows the $I-V$ curve of an Al/1.3 nm oxide/p⁺⁺-Si diode with an area of $3 \times 10^{-4}\text{ cm}^2$. The gate tunneling current increases abruptly at $V_g \sim 2.4\text{ V}$, which is due to the turn-on of band-to-band tunneling mechanism (surface bending $> 1.12\text{ eV}$). The larger inversion tunneling current level than that of the device on p⁺ substrate is the result of large electric field in the device on p⁺⁺ substrate. The higher substrate doping concentration, which makes tunneling rate $P(E_{\text{Si}})$ larger, leads to larger band-to-band tunneling current. The simulation results are also shown in Fig. 4. Due to the measurement limit ($< 100\text{ mA}$), the experimental data points with current larger than 100 mA are not

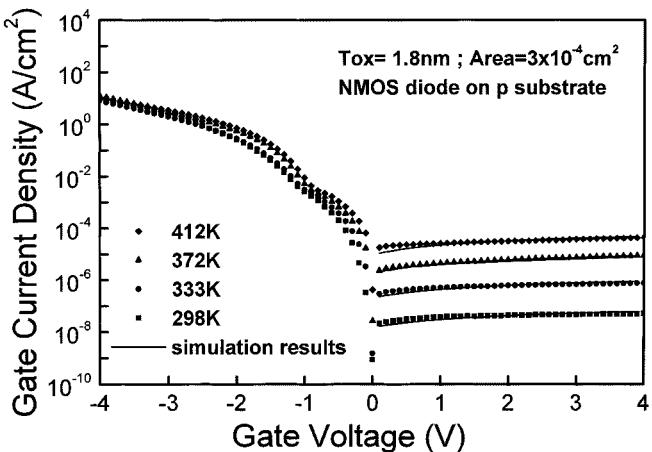


Fig. 5. $I-V$ curves of an NMOS diode on p substrate at different temperatures with SRH simulation results.

shown in Fig. 4. The heavy doping magnifies the band-to-traps and band-to-band tunneling.

V. TEMPERATURE AND ILLUMINATION EFFECT ON INVERSION CURRENT

A. Temperature Effect

Fig. 5 shows the $I-V$ curves of an Al/1.8 nm oxide/p-Si diode with an area of $3 \times 10^{-4}\text{ cm}^2$ at different temperatures (room temperature to 412 K). At positive gate bias, the gate current is relatively constant in log scale and reveals strong temperature dependence with activation energies of $\sim 640\text{ meV}$ at bias voltage from $0.5\text{~}\sim\text{~}3\text{ V}$. This confirms that the gate tunneling current is limited by the thermal generation rate of electron-hole pairs via defect at Si/SiO₂ interface and in the deep depletion region. The temperature dependence of gate current is different from previous work, reported by Yassine *et al.* [18], where the gate inversion current shows weaker temperature effect at high gate voltage on thicker oxide (3.7 nm). Note that at the low negative gate bias ($-1\text{ V} < V_g < 0\text{ V}$), however, the gate tunneling current exhibit weaker temperature dependence with activation energy of 155 meV at -0.5 V (not shown in Fig. 7), which may be caused by electron tunneling from Al gate electrode to silicon through interface states [19].

The $I-V$ curves of an Al/1.7 nm oxide/p⁺-Si diode with an area of $3 \times 10^{-4}\text{ cm}^2$ from room temperature to 410 K are shown in Fig. 6. The inversion current of the device with heavily doped p⁺ substrate exhibits strong field dependence at all measurement temperatures. The band-to-traps tunneling current has stronger temperature dependence as compared to the band-to-band tunneling current. This is due to temperature dependence of the SRH function in the band-to-traps transport equation.

The activation energies of the devices on p and p⁺ substrates at different gate voltages are extracted from Figs. 5 and 6 and are given in Fig. 7. For the devices on p-type substrate, the activation energy reveals no field dependence and its value is approximately equal to half of the silicon bandgap, since the most active traps are located in the middle of the bandgap. The SRH model can also describe the thermal generation rate of electron-hole pairs in the deep depletion and at Si/SiO₂ interface at elevated temperature.

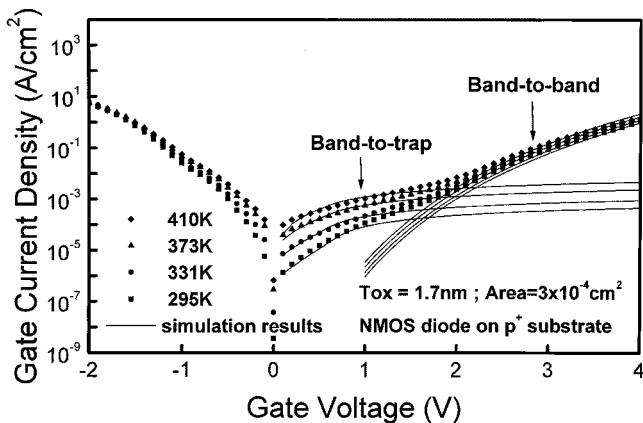


Fig. 6. $I-V$ curves of an NMOS diode on p^+ substrate at different temperatures with simulation results.

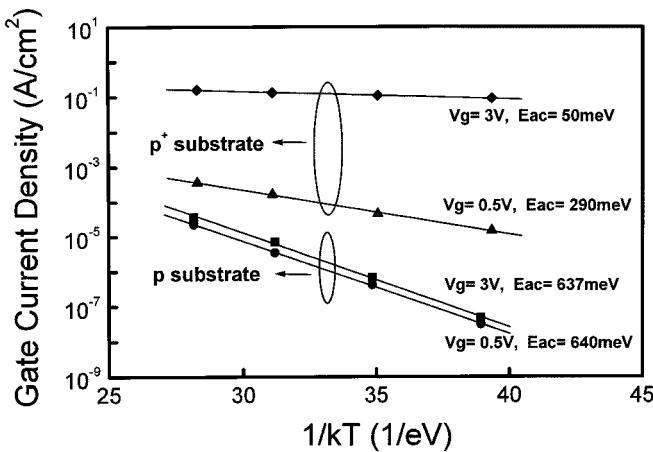


Fig. 7. Extraction of the activation energy at various gate voltage for p and p^+ substrate devices.

On the contrary, for the devices on p^+ substrate, the activation energy exhibits strong field dependence. At high gate bias ($V_g = 3$ V), the band-to-band tunneling current shows very small temperature dependence with an activation energy of 50 meV. At low gate bias ($V_g = 0.5$ V), the band-to-traps tunneling current has the activation energy of 290 meV.

B. Illumination Effect

Fig. 8 shows the dark current and photocurrent of an Al/2.3 nm oxide/p-Si tunneling diode at different illumination densities, and the device area is 3×10^{-4} cm². The photocurrent was excited by metal halide lamp with a spectrum similar to sun. The dark and photocurrent are relatively constant in log scale for positive gate bias larger than 0.2 V. For p⁺ substrate device, however, due to compete with the band-to-band tunneling current, the photocurrent can only be observed significantly at small gate bias ($V_g < 2$ V) under the applied light intensity (Fig. 9). Photo excitation generates much more electrons than thermal generation alone, and therefore the SRH and band-to-traps regimes have a measurable increase in tunneling current. However, even with photo excitation, the band-to-band tunneling current is still dominant under high band bending conditions, and independent of the light intensity.

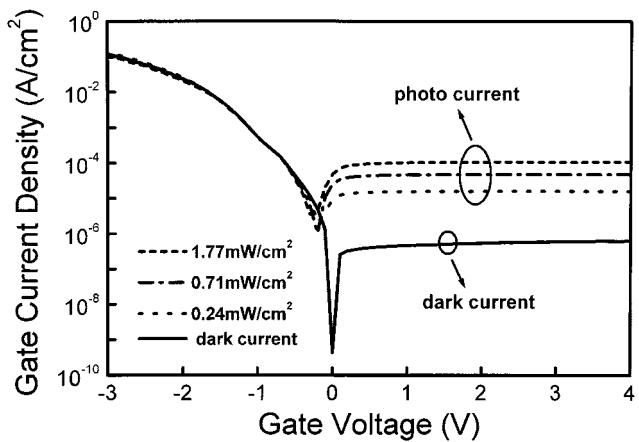


Fig. 8. Dark and photo currents of an NMOS tunneling diode on p substrate.

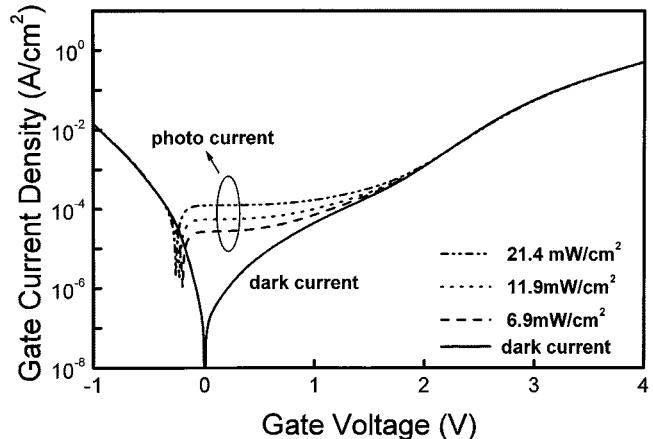


Fig. 9. Dark and photo currents of an NMOS tunneling diode on p^+ substrate.

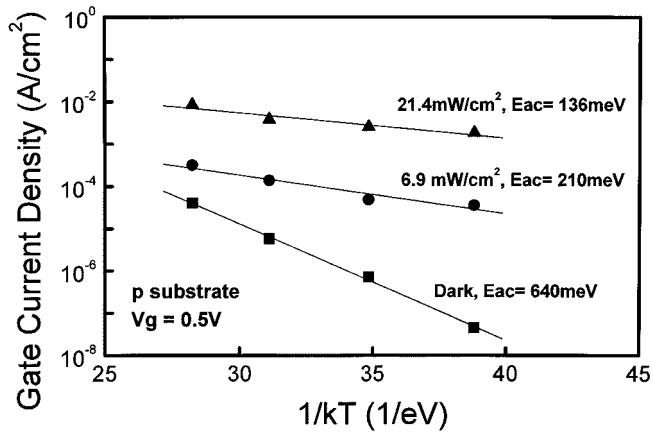


Fig. 10. Activation energies of an NMOS diode on p substrate at different illumination densities.

Fig. 10 shows the illumination density dependence of the activation energy in p-type substrate devices biased at low gate voltage (0.5 V) extracted from the $I-V$ measurement at different temperatures and light exposure density (not shown here). Under the illumination, most excess electrons are generated in conduction band by the photo excitation, which is independent of temperature. The inversion current consists of the thermal-

generated current due to temperature as well as the photo-generated current due to the photo illumination. The photo-generated current is dependent on the illumination intensity and has no temperature dependence. Therefore, the temperature dependence becomes less significant when the illumination intensity increases. This is shown in Fig. 10 and the activation energies of inversion current with no light exposure, 6.9 mW/cm^2 exposure, and 21.4 mW/cm^2 exposure are 640 meV, 210 meV, and 136 meV, respectively. However, the detailed modeling, which can predict the activation energy under the photo excitation using the SHR model, is still under investigation.

VI. CONCLUSION

In conclusion, the comprehensive study of gate inversion current in MOS tunneling diodes with different substrate doping is investigated. For p-type substrate devices, the inversion tunneling current is dominated by the thermal generation rate of electron-hole pairs via interface traps and the traps in the deep depletion region. The inversion current is relatively constant in log scale and shows strong temperature and illumination density dependence. The value of activation energy is approximately equal to half of the silicon bandgap, since the most active traps are located near the middle of the bandgap. On the contrary, for p⁺ and p⁺⁺ substrate devices, the gate current is dominated by band-to-band tunneling at high gate bias and by band-to-traps tunneling at low gate bias. The gate current of the device on p⁺ substrate biased at inversion region exhibits stronger field dependence and weaker temperature dependence than devices on p substrate.

REFERENCES

- [1] *International Technology Roadmap for Semiconductors*, 1999.
- [2] C. W. Liu, M. H. Lee, M.-J. Chen, I. C. Lin, and C.-F. Lin, "Room-temperature electroluminescence from electron-hole plasmas in the metal oxide silicon tunneling diodes," *Appl. Phys. Lett.*, vol. 76, no. 12, pp. 1516–1518, 2000.
- [3] C. W. Liu, M. H. Lee, M. J. Chen, C.-F. Lin, and M. Y. Chern, "Roughness-enhanced electroluminescence from metal oxide silicon tunneling diodes," *IEEE Electron Device Lett.*, vol. 21, pp. 601–603, Dec. 2000.
- [4] C. W. Liu, W. T. Liu, M. H. Lee, W. S. Kuo, and B. C. Hsu, "A novel photodetector using MOS tunneling structures," *IEEE Electron Device Lett.*, vol. 21, pp. 307–309, June 2000.
- [5] K. F. Schuegraf and C. Hu, "Low injection SiO₂ breakdown model for very low voltage lifetime extrapolation," *IEEE Trans. Electron Devices*, vol. 41, pp. 761–767, May 1994.
- [6] A. Schenk and G. Heiser, "Modeling and simulation of tunneling through ultrathin dielectrics," *J. Appl. Phys.*, vol. 81, no. 12, pp. 7900–7908, 1997.
- [7] N. Yang, W. K. Henson, J. R. Hauser, and J. J. Wortman, "Modeling study of ultrathin gate oxides using direct tunneling current and capacitance-voltage measurements in MOS devices," *IEEE Trans. Electron Devices*, vol. 46, pp. 1464–1471, July 1999.
- [8] L. F. Register, E. Rosenbaum, and K. Yang, "Analytic model for direct tunneling current in polycrystalline silicon-gate metal-oxide-semiconductor devices," *Appl. Phys. Lett.*, vol. 74, no. 3, pp. 457–459, 1999.
- [9] T.-E. Chang, C. Huang, and T. Wang, "Mechanisms of interface trap-induced drain leakage current in off-state n-MOSFET's," *IEEE Trans. Electron Devices*, vol. 42, pp. 738–743, Apr. 1995.
- [10] M. Rosar, B. Leroy, and G. O. Schweeger, "A new model for the description of gate voltage and temperature dependence of gate induced drain leakage (GIDL) in the low electric field region," *IEEE Trans. Electron Devices*, vol. 47, pp. 154–159, Jan. 2000.
- [11] A. Ghetti, C.-T. Liu, M. Mastrapasqua, and E. Sangiorgi, "Characterization of tunneling current in ultrathin gate oxide," *Solid-State Electron.*, vol. 44, pp. 1523–1531, 2000.
- [12] M. Y. Doghish and F. D. Ho, "A comprehensive analytical model for metal-insulator-semiconductor (MIS) devices," *IEEE Trans. Electron Devices*, vol. 39, pp. 2771–2780, Dec. 1992.
- [13] A. S. Grove, *Physics and Technology of Semiconductor Devices*. New York: Wiley, 1967.
- [14] G. A. M. Hurkx, D. B. M. Klaassen, and M. P. G. Knuvers, "A new recombination for devices simulation including tunneling," *IEEE Trans. Electron Devices*, vol. 39, pp. 331–338, Feb. 1992.
- [15] G. A. M. Hurkx, H. C. de Graaff, W. J. Kloosterman, and M. P. G. Knuvers, "A new analytical diode model including tunneling and avalanche breakdown," *IEEE Trans. Electron Devices*, vol. 39, pp. 2090–2098, Sept. 1992.
- [16] K.-F. You and C.-Y. Wu, "A new quasi-2-D model for hot-carrier band-to-band tunneling current," *IEEE Trans. Electron Devices*, vol. 46, pp. 1174–1179, June 1999.
- [17] S. M. Sze, *Physics of Semiconductor Devices*, 2nd ed. New York: Wiley, 1981.
- [18] A. Yassine and R. Hijab, "Temperature dependence of gate current in ultrathin SiO₂ in direct-tunneling regime," Integrated Reliability Workshop Final Rep., pp. 56–61, 1997.
- [19] A. Ghetti, E. Sangiorgi, J. Bude, T. W. Scorsch, and G. Weber, "Low voltage tunneling in ultrathin oxides: A monitor for interface states and degradation," in *IEDM Tech. Dig.*, 1999, pp. 731–734.



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From 1994 to 1996, he was an Associate Professor at National Chunghsin University, Taichun, Taiwan. Now he is an Associate Professor at NTU. His current research interests include CMOS optoelectronics, optical interconnects, SiGe high-speed devices, and rapid thermal process. He invented the first MOS tunneling light-emitting diode and photodetector. He owns two patents on photodetectors.