Mechanically Strained Strained-Si NMOSFETs

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***Abstract*—The drain-current enhancement of the mechanically strained strained-Si NMOSFET device is investigated for the first time. The improvements of the drain current are found to be $\sim 3.4\%$ and $\sim 6.5\%$ for the strained-Si and control Si devices, respectively, with the channel length of 25 μm at the external biaxial tensile strain of 0.037%, while the drain-current enhancements are $\sim 2.0\%$ and $\sim 4.5\%$ for strained-Si and control Si devices, respectively, with the channel length of 0.6 μm. Beside the strain caused by lattice mismatch, the mechanical strain can further enhance the current drive of the strained-Si NMOSFET. The strain distribution due to the mechanical stress has different effect on the current enhancement depending on the strain magnitude and channel direction. The smaller current enhancement for strained-Si device as compared to the control device can be explained by the saturation of mobility enhancement at large strain.**

***Index Terms*—Drain-current enhancement, mechanical strain, strained-Si nMOSFET.**

I. Introduction

RECENTLY, the strained-Si MOSFETs have become attractive for high-speed, complementary metal–oxide-semiconductor (CMOS) device applications [1], [2]. Biaxial tensile strain in the pseudomorphic-Si layer, epitaxially grown on relaxed SiGe, splits the degeneracy in conduction and valence bands of bulk Si, and leads to the light effective mass of carriers and reduces intervalley scattering. The electron mobility enhancement in strained-Si NMOSFETs is due to the strain induced band structure modification. The electron mobility can be further enhanced by externally applied mechanical stress (strain) on strained-Si NMOSFETs. To investigate the individual device characteristics with longitudinal and transverse mechanical stress (strain), the Si MOSFET has been studied by a conventional four-point bending method [3]–[8], but the effect of biaxial mechanical strain on the device characteristics of Si and strained-Si has not yet been reported. In this letter, we have demonstrated a new mechanical setup to control the mechanical strain on the Si substrate and thus to enhance the performance of strained-Si NMOSFET characteristics. The setup can produce biaxial mechanical strain similar to the strain produced by relaxed SiGe layers, and allows the circuit layout with device channels at different directions. Note that uni-axial bending is not practical for the circuit layout, since most circuits have device channels at different directions.

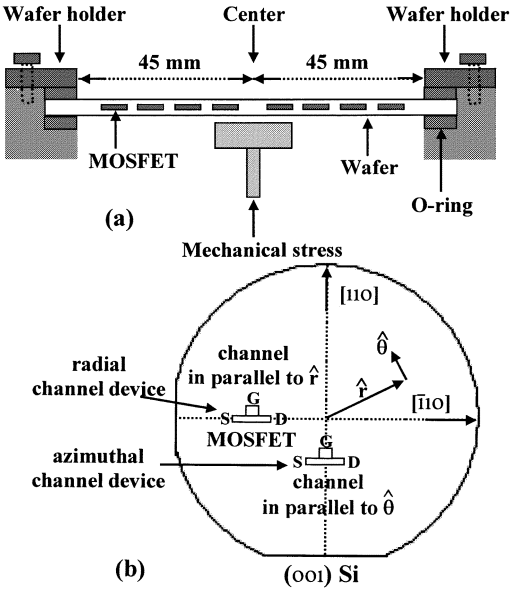

Fig. 1. (a) Schematic diagram of the externally applied mechanical stress on the Si (100) wafer, and (b) the devices with the channel along the azimuthal direction (θ) on the 11O direction, and the devices with the channel along the radial direction (r) on the $\bar{1}1$O direction.

II. Experiment

The relaxed $Si_{0.8}$ $Ge_{0.2}$ layers (1 μm thick) with a uniform Ge content (20%) were grown by ultrahigh vacuum chemical vapor deposition (UHVCVD) on an epitaxial-graded Si_{1-x} Ge_x layers (1-μm-thick) with the Ge content from 0 to 20% at 600 °C using silane (SiH_4) and germane (GeH_4) precursors. Then, the 20-nm-thick undoped strained-Si layers were grown on the relaxed $Si_{0.8}$ $Ge_{0.2}$ virtual substrate. The Raman spectrum shows that strain in the strained-Si device is $\sim 0.64\%$. The control Si and strained-Si NMOSFETs were fabricated at the same time by a conventional process. To reduce the thermal budget, the gate oxide tetraethylorthosilicate (TEOS) with a thickness of $\sim$30 nm was deposited at 700 °C. The doping concentrations are $\sim 1 \times 10^{15}$ cm^{-3} and $\sim 1 \times 10^{16}$ cm^{-3} for control Si and strained-Si devices, respectively.

In this letter, we have applied externally a uniform mechanical stress at the center with the diameter of 13-mm on 100-mm wafers for both the strained-Si and control Si devices with the displacement of ~ 0.9 mm as shown in Fig. 1(a). The mechanical strain at the center of the wafer during the external applied stress is $\sim 0.037\%$. The schematic diagram of the setup to apply stress, and the orientation of devices on the wafers are shown in Fig. 1(a) and (b), respectively. According to the device layout,

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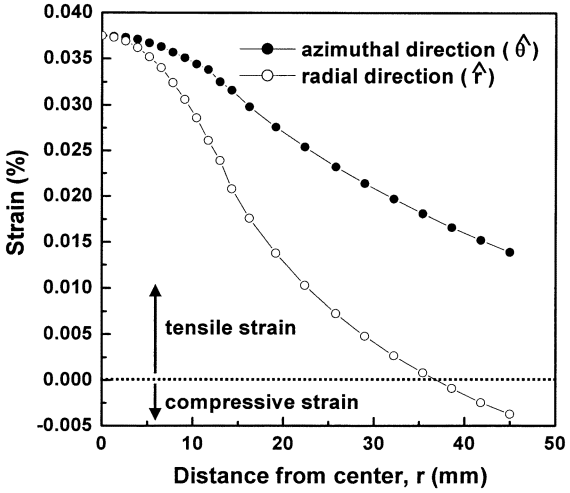

Fig. 2. Strain field is simulated by ANSYS. The strain is higher in azimuthal direction as compared to the radial direction. Most of the area have tensile strain and only a slightly compressive strain is identified at near to the edge of the wafer.

the devices with the channel directions parallel to the azimuthal and radial directions are placed along 11O and $\bar{1}$1O, respectively. The devices have both gate lengths of 25 and 0.6 μm with a same gate width of 25 μm.

III. Results and Discussion

To investigate the strain distribution along the azimuthal and radial directions on the 100-mm wafer, finite element simulation by ANSYS has been performed as shown in Fig. 2. The biaxial strain is observed at center area of the wafer, but the strain along the azimuthal direction is higher than that along the radial direction. This simulation also shows a compressive radial strain at the wafer edge. The strain gradually decreases from the center to edge of the wafer.

Fig. 3 shows the typical drain current (I_{ds}) versus drain voltage (V_{ds}) characteristics with and without mechanical stress at V_{gs}–V_t =1, 2, and 3 V near the center of the wafer, where the external biaxial strain is maximum ($\sim$0.037%). The threshold voltages (V_t) of control Si and strained-Si devices are found to be 0.025 and 0.01 V, respectively, using the $\sqrt{I_{ds}}$ versus V_{gs} (gate voltage) at the saturation region. The smaller V_t of the strained-Si device is due to the lower conduction edge of strained-Si than that of control Si. The threshold voltages of both the strained-Si and control Si devices do not change after the mechanical stress as compared to the mechanical stress-free condition. This result is similar to the [5]. The peak mobility enhancement factor of the strained-Si device with respect to the control device is $\sim$1.7, obtained from the split capacitance—voltage (*C–V*) measurement, while the drain-current enhancement factor, $(I_{ds})_{\text{strained-Si}}/(I_{ds})_{\text{control Si}}$, is $\sim$2 due to the lower series resistance of the strained-Si device as compared to the control device. In our devices, the contact resistance is dominant in the series resistance. Due to the smaller bandgap of strained-Si, the strained-Si device has a lower contact resistance ($\sim$19 Ω-μm^2 for strained-Si device and $\sim$36 Ω-μm^2 for control Si devices).

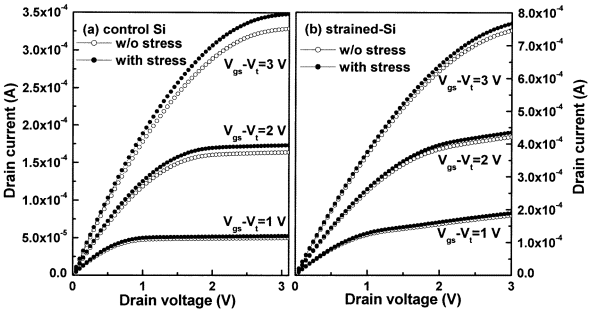

Fig. 3. Drain current versus drain voltage for (a) a control Si and (b) a strained-Si device ($W \times L = 25 \times 25$ μm^2) with and without mechanical strain.

The drain-current enhancements are found to be $\sim$3.4% and $\sim$6.5% for strained-Si and control Si devices ($W \times L = 25 \times 25$ μm^2), respectively, with the external strain of 0.037% at $V_{ds} = 1$ V and V_{gs}–$V_t = 3$ V. This indicates that the strained-Si device has a $\sim$90% current enhancement per percent of strain at $I_{ds} = 362.5$ μA and control Si device has a $\sim$175% current enhancement per percent of strain at $I_{ds} = 177.5$ μA. For the channel length of 0.6 μm, the drain-current enhancements are found to be $\sim$2.0% and $\sim$4.5% for strained-Si and control Si devices, respectively. The drain-current enhancement decreases with decreasing the channel length due to the velocity overshoot effect [7]. The improvement of the drain current is due to the mobility enhancement at the presence of tensile strain. It is noted that the drain-current enhancement of control Si devices due to the mechanical stress are almost 2 times higher than that of the strained-Si devices. This phenomenon can be explained by investigating the electron mobility enhancement factor of Si under biaxial tensile strain [9]. It is observed that the slope of the electron mobility enhancement factor at low tensile strain ($<$0.1%) is almost 2.5 times higher than that at high strain (0.64%) due to the saturation of mobility enhancement. Note that the 0.64% is the strain in the strained-Si device.

To clarify the channel orientation effect on the drain-current enhancements due to the mechanical strain distribution on the wafer, we have studied the NMOSFETs located along 11O and $\bar{1}$1O direction on the wafer [Fig. 1(b)]. The devices along the $\bar{1}$1O direction have channels along the radial direction (radial channel device) and the devices along the 11O direction have channels along the azimuthal direction (azimuthal channel device). Fig. 4 shows the drain-current enhancement versus distance from center of the wafer for both the control Si and strained-Si devices with the channel length of 25 and 0.6 μm. It is known [6] that the strain parallel to the channel can enhance more current than that of the strain perpendicular to the channel for NMOS devices. The I_{ds} enhancement of the azimuthal channel devices is higher than that of the radial channel devices due to the higher azimuthal strain than radial strain during mechanical stress (Fig. 2). The enhancement is in a good agreement with the reported result for Si device [6]. The current enhancement decreases gradually from the center toward the edge of the wafer for both strained-Si and control devices with the gate lengths of 25 μm and 0.6 μm, due to the higher mechanical strain at the center region than the edge of the wafer. This result is corroborating with the simulated strain

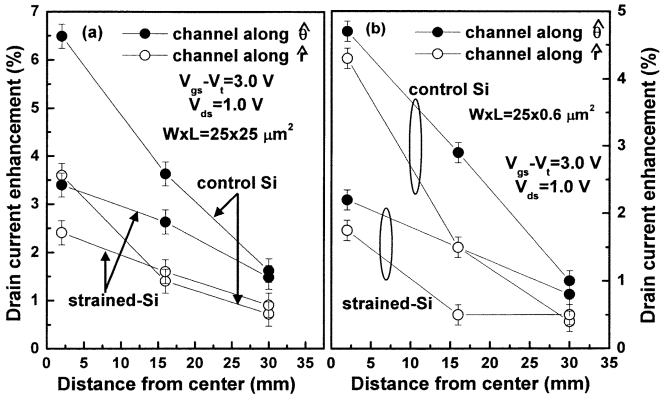

Fig. 4. Drain-current enhancement versus the distance from the center of the wafer for both the mechanically strained strained-Si and control Si devices with (a) $L = 25\ \mu$m and (b) $L = 0.6\ \mu$m. Note that the error bar of the measurement is $\sim 1.0\%$, and therefore the difference of the small current enhancement in strained-Si and control Si devices can not be distinguished at the same data points.

distribution on the wafer as shown in Fig. 2. A compressive strain is observed at the wafer edge, but no device is placed at that position. The distribution of current enhancement reflects out the strain field distribution, and the strain field is determined by the mechanical setup.

IV. Conclusion

We have investigated the drain-current enhancements for both strained-Si and control Si NMOSFETs using a new mechanical setup. The maximum drain current improvements are found to be $\sim 3.4\%$ and $\sim 6.5\%$ for the mechanically strained strained-Si and control Si devices, respectively, with the gate length of 25 μm at a maximum external strain $(\sim 0.037\%)$. The drain-current enhancement decreases with shrinking the channel length. The strain field obtained by finite element simulation is consistent with the current enhancement distribution for both strained-Si and control devices. According to the measured output device characteristics and the simulation of the strain distribution on the wafer, it paves a new way to improve the device characteristics of the strained-Si and control Si devices for CMOS applications.

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