行政院國家科學委員會專題研究計畫　期中進度報告

兼具偵測多波段紅外線及可見光的偵測器陣列模組之研發

(1/3)

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一、中文摘要

本計畫預期完成兼具偵測多波段紅外線及可見光的偵測器陣列模組。其主要工作內容包含三部分：單一偵測器的設計與製作、偵測器陣列的設計與製作、讀出電路的設計與製作，最後是偵測器陣列與讀出電路的整合。

在單一偵測器方面，我們所要完成的偵測器，不但具有偵測不同紅外線波段輻射強度的能力，而且能遙測物體溫度。該偵測器的基本結構是：兩種不同的超晶格結構，而其中夾著一寬能障。兩超晶格具有不同的電子躍遷能階，故能偵測不同波段的紅外線。而中間的寬能障，可作為電子能量的高通過濾器，具有調變偵測器響應的功能。利用二種不同的偵測器響應，我們可求出光電流的比值，由此遙測出輻射物體的溫度。

在偵測器陣列方面，我們針對超晶格偵測器的特性，設計出可正面入射的像素(pixel) 。其中每一像素的表面，均有 V 型的凹槽，以解決該偵測器正向入射的問題；另在像素 mesa 的側面，均覆蓋著絕緣體及金屬層，這是為了反射光線及防止表面漏電流而設計的。如此的陣列設計，可增加捕光的能力，又能防止像素間的串訊，另具防止表面漏電流等多重功能。本計畫的陣列是以一維的線性陣列為重心。

在讀出電路方面，我們針對紅外線陣列的需要，設計出相配的讀出電路。其中以 correlated doubled sampling circuitry 來減除重置雜訊。並以差動放大器將亮訊號減去暗訊號，以增加讀出電路的零敏度。在製作讀出電路的同時，我們也將利用 CMOS 技術製作可見光偵測器，以期使整個模組兼具偵測多波段紅外線及可見光的能力。

我們長期的目標在於完成熱影像攝影系統。而本計畫則以線性陣列模組為近期的工作項目，預計以三年的時間完成。

二、本年度計畫緣由與目的

For thermal imaging, 1-D or 2-D (Focal Plane) staring arrays would be used instead of one single detector. Hence, uniformity of each detector cannot be too emphasized. The uniformity of the detector array primarily depends on the accuracy and precision of the Molecular Beam Epitaxy (MBE) or Metal-organic Chemical Vapor Deposition (MOCVD). In the following sections, we will describe history of thermal imaging by infrared photodetector arrays and the fabrication formerly used to achieve light coupling. Then, we will introduce our new method to fabricate the 1-D linear detector array, which has several merits over the formerly fabricated detector array. This fabrication method had been recorded in our patent for which we had applied. Finally, the uniformity of this 1-D linear infrared photodetector array may be calculated by measuring the I-V characteristics of several pixels in one array at temperature of 78 K.

三、執行進度

As shown in Fig. 1 is the 3-D solid view of a 1×N linear IR detector array. One of the main goals of this 1-D detector array is to eliminate the crosstalk between two neighboring IR detection pixels with an optical isolation structure, which was achieved by applying the trench technology among the neighboring detection pixels. A fabricating instance of this linear array is shown in Fig. 2, which corresponds to the vertical (AA' direction) and transverse (BB' direction) cross-section of the array bulk in Fig. 1, respectively. In this instance, the same part shown in different sub-figures was labeled with an identical number.

Refer to Fig. 2(a), according to this instance, the IR detector array use a semi-insulating (S-I) GaAs wafer as substrate (201). Then we grow an epi-layer (202) above the substrate. This epi layer contains upwards an n-type bottom-contact layer (202a), an active layer (202b) made of multiquantum wells or superlattices, and an n-type top-contact layer (202c). The epi-layer 202 is the main structure of the IR detection pixel.

Refer to Fig. 2(b), we first transfer the pattern on the surface of the epi-layer by lithography. The pattern to be defined consists of the region protected by the PR or

not. Then the naked region is etched by reactive ion etching (RIE). The etched region contains the mesh-like trench (206) and the common ground region (207), while the unetched region contains top-contact region (205), MIS mesas (204) and numbers of detection pixels (203). Each detector array has two MIS mesas, one is at the front end, and the other is at the rear end. Besides, the angle between the trench and cleaved edge ($[01\bar{1}]$ or [011]) of wafer should be 45° so that the vertical sidewalls of the trench are natural cleavage planes. Next, the wafer is soaked in the etching solution for several seconds so that roughness and defects on the surface of the trench can be reduced and hence further prevent surface leakage current. Besides, what should be kept an eye on is that the mesh-like trenches and the common ground regions must reach to the bottom contact layer (202a), so that external electric field can be dropped upon the active layer (202b) of detection pixels and electrical isolation among pixels can be achieved.

Refer to Fig. 2(c), an insulating layer of Si_3N_4 (1^{st} insulating layer 208) is deposited on the surface of the wafer by PECVD. By fabricating this insulator layer the short problem between the top and bottom of the IR detector pixel or between the different IR detector pixel could be eliminated. Then a reflecting metal layer (209) of aluminum (Al) is coated on the 1^{st} insulating layer by sputtering. Afterward we flat the wafer by refilling a layer (2^{nd} insulating layer 210) of SOG (Spin On Glass) into the mesh-like trench. The aforementioned SOG could be replaced by polyimide. Next, we removed the 1^{st} insulating layer and the reflecting metal layer from the wafer except those on the MIS mesas and trenches.

Refer to Fig. 2(d), to achieve light coupling we construct numbers of rectangular grooves (211) on the surface of each individual detection pixel by wet etching. The longer side of each rectangular groove must be parallel to the $[01\bar{1}]$ direction. The anisotropic etching solution is made of H_2SO_4、H_2O_2 and DI water with specific ratio, as demonstrated by the Electrochemical Society. The groove looks like a boat, whose transverse cross-section is V-shaped and the longitudinal cross-section looks like a dovetail, as the label 211a and 211b show in Fig. 2(d).

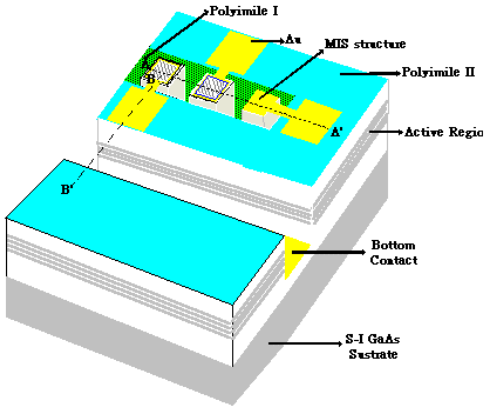
Refer to Fig. 2(e), before forming the metal lines and contacts on each detection pixel, we coat the surface of the top-contact region (205) with a field-passivation layer (212) to achieve electrical passivation. The field-passivation layer is made of either SOG or polyimide or any other insulators. Next, we deposit in turn an alloy layer of Au/Ge/Ni and a layer of Au onto the surface of wafer by evaporation. Then we remove the excess metal by lift-off method or wet etching to form the metal electrode (213). These metal electrodes can be classified as pixel electrodes (213a), MIS electrodes (213b), and common-ground electrodes (213c). Finally, ohmic contacts are formed by rapid thermal annealing (RTA) these metal electrodes.

The fabricated wafer is then sliced into pieces of detector arrays. As shown in Fig. 3, each pixel uses v-groove structures as the manner for light coupling. When the external IR radiation is normally incident into the detection pixel, it will be refracted and hence result in effective photoelectric interaction. Moreover, a SiN layer followed by a metal layer is deposit on the sidewall surface of the pixel. Because metal tends to reflect light, as the IR radiation enter the pixel it would be trapped in the same pixel and hence prevents crosstalk from occurring. In addition, the metal (Al) layer (209) and the insulating layer (208) on the sidewalls of trench are connected intimately with those on the MIS mesas (204), as shown in Fig. 2(e) and the insert of Fig. 3. Because electrodes on these MIS mesas are independent of those on detection pixels and common ground, by applying a reverse bias to electrode on the MIS mesa, carriers of the surface of the trench would be depleted and the surface leakage currents due to surface states could be reduced.

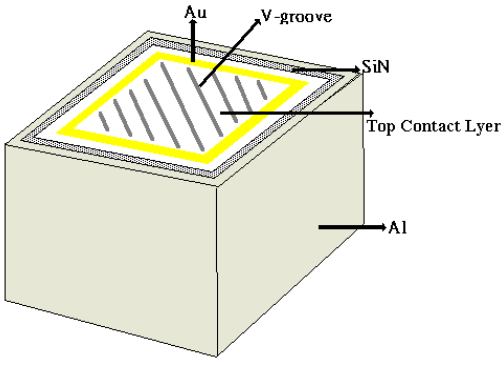
四、總結

From description above, we are sure that this invention possesses many advantages such as being a practical and simple process to fabricate linear array and enhancing the detecting efficiency of quantum well and superlattice IR photodetectors. Moreover, the structure of the 1-D detector array has several advantages such as the ability to diffract the normal incident rays to the device and thus achieve effective photoelectric effect, and the ability to confine the incident radiation into the individual pixel. Certainly, for the linear array can be used extensively for thermal imaging, each detection pixel should be in background limited performance (BLIP) up to 78K and uniformity of each detection pixel in the array should be emphasized critically.

五、圖表及註解



(a)



(b)

Figure 1 The schematic 3-D solid view of a 1×N linear IR detector array (a) and one of its detection pixels.

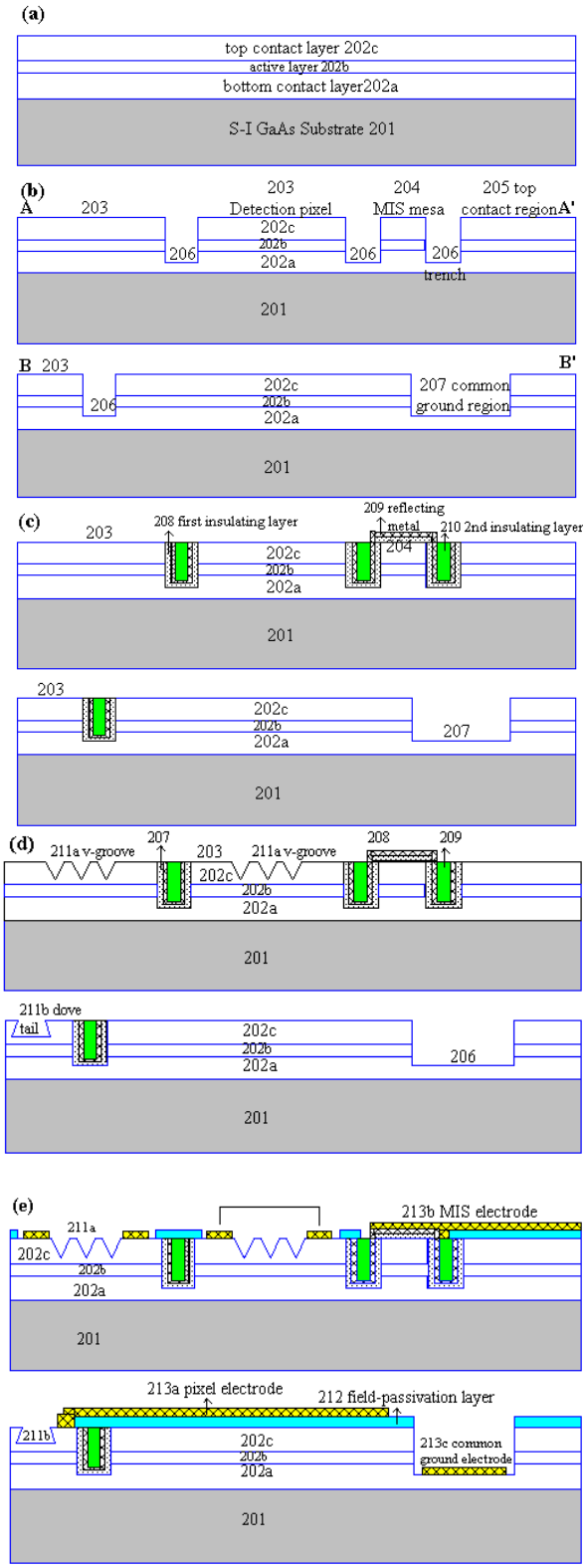


Figure 2 The schematic process flow of the 1-D linear array, which corresponds to the vertical (AA' direction) and transverse (BB' direction) cross-section of the array bulk in Fig. 1, respectively

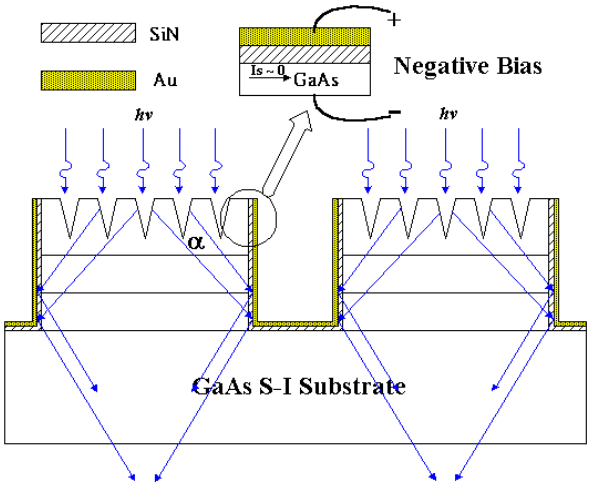


Figure 3 The schematic profile of the 1-D linear array. In this figure, optical coupling, light trapping and MIS structure are shown

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