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A Compact Threshold Voltage Model for Gate Misalignment Effect of DG FD SOI nMOS Devices Considering Fringing Electric Field Effects

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***Abstract*—This paper reports an analysis of gate misalignment effect on the threshold voltage of double-gate ultrathin fully depleted silicon-on-insulator nMOS devices using a compact model considering the fringing electric field effect, biased at zero-bias V_{DS}. Using the conformal mapping transformation approach, a closed-form compact model considering the fringing electric field effect in the nongate overlap region has been derived to provide an accurate prediction of the threshold voltage behavior as verified by the two-dimensional simulation results.**

***Index Terms*—Device modeling, MOS, silicon-on-insulator (SOI).**

I. Introduction

DOUBLE-GATE (DG), silicon-on-insulator (SOI) technology has been regarded as another mainstream technology for sub-100-nm CMOS very large-scale integration (VLSI) owing to its advantages in reduced second-order effects[1], [2]. Many aspects of DG SOI devices have been studied [3]–[6]. For DG SOI CMOS devices, the gate misalignment has a large effect on device performance [7]. Fig. 1 shows the two-dimensional (2-D) electric field contours in a DG SOI nMOS device with a gate oxide thickness of 70 Å, a thin film of 600 Å doped with a p-type density of 4×10^{17} cm^{-3}, and a gate misalignment of 0.04 μm, biased at $V_G = V_{th}$, and $V_D = 50$ mV. As shown in the figure, the fringing electric field from the right edge of the bottom gate to the thin film of the nongate overlap region is substantial, which could have a nonnegligible influence on device performance. Several models for DG SOI devices have been reported [8]–[10]. However, until no analytical model for the gate misalignment effect has been reported. In this paper, an analysis of the gate misalignment effect on the threshold voltage of DG ultrathin FD SOI nMOS devices is reported, using a compact model that considers the fringing field effect. It is shown that by using the conformal mapping transformation approach, such a closed-form model, which is reported for the first time, can provide an accurate predication of the threshold voltage behavior as verified by the 2-D simulation results. In the following sections, derivation of the analytical model is described, followed by model verification and discussion.

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II. Model Derivation

In this section, a compact zero-biased threshold voltage considering the fringing electric field effect is derived. In order to concentrate on the fringing electric field effects from gate misalignment, a DG SOI nMOS device with a channel length of 0.2 μm and a gate misalignment u_s as shown in Fig. 2(a), biased at its threshold voltage $V_G = V_{th}$ and $V_D = 50$ mV for the zero-bias V_{DS} condition, is considered. Define the origin of the coordinates at the tangent to the left edge of the top gate on the back surface. The Y-axis is along the back surface in the drain direction. The X-axis is in the vertical direction tangent to the left edge of the top gate. In the thin film, 2-D Poisson's equation is

$$\frac{\partial^2\Psi(x,y)}{\partial x^2}+\frac{\partial^2\Psi(x,y)}{\partial y^2}=\frac{qN_A}{\epsilon_{si}} \tag{1}$$

where N_A is the p-type doping density of the thin film, ϵ_{si} is silicon permittivity, and q is electronic charge. In order to simplify the analysis, polysilicon depletion effect [11], [12] and quantum effects [13], [14] are not considered. In the following derivation, the thin film is divided into (I) gate overlap region and (II) nongate overlap region.

A. Gate Overlap Region (I)

In the gate overlap region (I), a 2-D parabolic approximation [10] has been used to solve 2-D Poisson's equation

$$\Psi_1(x,y)=P_{01}(y)+P_{11}(y)x+P_{21}(y)x^2. \tag{2}$$

The boundary conditions for the gate overlap region (I) are that at top and bottom thin-film interfaces, the displacements are continuous

$$\begin{aligned}-\frac{\partial\Psi_1(x,y)}{\partial x}\Big|_{x=t}&=\frac{C_{ox2}}{\epsilon_{si}}[V_G+\phi_{f2}-\Psi_{b1}(y)]\\ -\frac{\partial\Psi_1(x,y)}{\partial x}\Big|_{x=0}&=\frac{C_{ox1}}{\epsilon_{si}}[\Psi_{s1}(y)-V_G-\phi_{f1}]\end{aligned} \tag{3}$$

where $C_{ox1/2}$ is the unit-area top/bottom gate oxide capacitance, V_G is the gate voltage, $\phi_{f1/2}=(kT/q)\ln(N_{poly}/n_i)$ is the Fermi voltage of the top/bottom gate, $\Psi_{b1}(y)$ is the back surface potential [$\Psi_{b1}(y)=\Psi_1(0,y)$], and $\Psi_{s1}(y)$ is the front surface potential [$\Psi_{s1}(y)=\Psi_2(t_{si},y)$]. Solving 2-D Poisson's equation

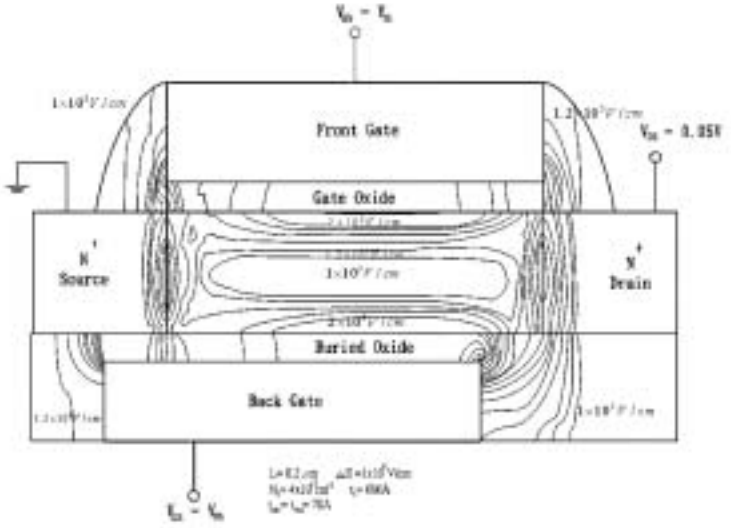

Fig. 1. Two-dimensional electric field contours in a DG SOI nMOS device with n^+ polysilicon top and bottom gates, a gate oxide of 70 Å, a thin film of 600 Å doped with a p-type density of 4×10^{17} cm^{-3}, and a gate misalignment of 0.04 μm, biased at $V_G = V_{th}$ and $V_D = 10$ mV.

with the boundary conditions, the coefficients are shown in (4) at the bottom of the page. In addition, a relationship between front and back surface potentials has been obtained

$$\Psi_{s1}(y) = \Psi_{b1}(y) - \frac{C_{ox2}}{\epsilon_{si}}[V_G + \phi_{f2} - \Psi_{b1}(y)]t_i + P_{21}(y)t_i^2. \tag{5}$$

Since the thin film is very thin, we may assume that [10]

$$\frac{\partial^2 \Psi_1(y)}{\partial y^2} \cong \frac{1}{\kappa_s}\frac{\partial^2 \Psi_{b1}(y)}{\partial y^2}. \tag{6}$$

From (1), (2), (4) and (6), a differential equation in terms of the back surface potential is

$$\frac{\partial^2 \Psi_{b1}(y)}{\partial y^2} - \kappa_s \frac{\left(1 + \frac{C_{ox1}}{C_s} + \frac{C_{ox2}}{C_{ox1}}\right)}{\frac{1}{2}t_i^2\left(1 + \frac{2C_s}{C_{ox1}}\right)}\Psi_{b1}(y) = \kappa_s\left[\frac{qN_A}{\epsilon_{si}} - \frac{\left(1 + \frac{C_{ox1}}{C_s} + \frac{C_{ox2}}{C_{ox1}}\right)V_G + \left(\frac{C_{ox1}}{C_s} + \frac{C_{ox2}}{C_{ox1}}\right)\phi_{f2} + \phi_{f1}}{\frac{1}{2}t_i^2\left(1 + \frac{2C_s}{C_{ox1}}\right)}\right]. \tag{7}$$

Solving this differential equation, the back surface potential is

$$\Psi_{b1}(y) = C_1 \exp\left(\sqrt{A_0}y\right) + C_2 \exp\left(-\sqrt{A_0}y\right) - \frac{A_1}{A_0}$$

$$A_0 = \kappa_s\left[\frac{\left(1 + \frac{C_{ox1}}{C_s} + \frac{C_{ox2}}{C_{ox1}}\right)}{\frac{1}{2}t_i^2\left(1 + \frac{2C_s}{C_{ox1}}\right)}\right]$$

$$A_1 = \kappa_s\left[\frac{qN_A}{\epsilon_{si}} - \frac{\left(1 + \frac{C_{ox1}}{C_s} + \frac{C_{ox2}}{C_{ox1}}\right)V_G + \left(\frac{C_{ox1}}{C_s} + \frac{C_{ox2}}{C_{ox1}}\right)\phi_{f2} + \phi_{f1}}{\frac{1}{2}t_i^2\left(1 + \frac{2C_s}{C_{ox1}}\right)}\right]. \tag{8}$$

B. Nonoverlap Gate Region (II)

In the nongate overlap region (II), the electrostatic potential is approximated as

$$\Psi_2(x, y) = P_{02}(y) + P_{12}(y)x + P_{22}(y)x^2. \tag{9}$$

$$P_{01}(y) = \Psi_{b1}(y)$$

$$P_{11}(y) = -\frac{C_{ox2}}{\epsilon_{si}}[V_G + \phi_{f2} - \Psi_{b1}(y)]$$

$$P_{21}(y) = \frac{-\left[1 + \frac{C_{ox1}}{C_s} + \frac{C_{ox2}}{C_{ox1}}\right]\Psi_{b1}(y) + \left[1 + \frac{C_{ox1}}{C_s} + \frac{C_{ox2}}{C_{ox1}}\right]V_G + \left[\frac{C_{ox1}}{C_s} + \frac{C_{ox2}}{C_{ox1}}\right]\phi_{f2} + \phi_{f1}}{t_i^2\left(1 + \frac{2C_s}{C_{ox1}}\right)}. \tag{4}$$

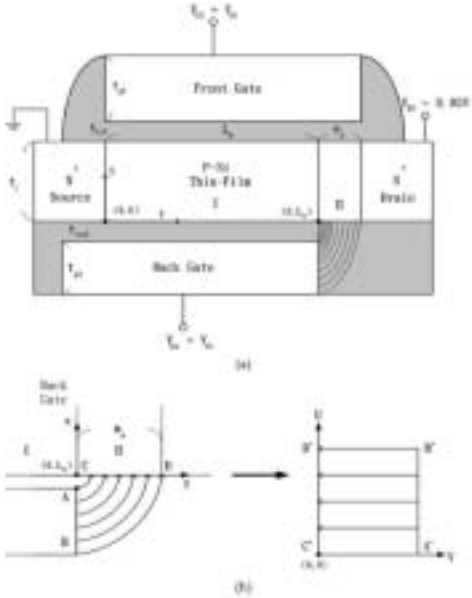

Fig. 2. (a) Cross section of the DG SOI nMOS device with a gate misalignment and (b) the boundary of the sidewall oxide region next to the right edge of the bottom gate before and after conformal mapping for model derivation.

The boundary conditions at top and bottom interfaces become

$$-\frac{\partial\Psi_2(x,y)}{\partial x}|_{x=0}=\frac{\epsilon_{ox}}{\epsilon_{si}t(y)}[V_G+\phi_{f2}-\Psi_{b2}(y)]$$
$$-\frac{\partial\Psi_2(x,y)}{\partial x}|_{x=t_i}=\frac{C_{ox1}}{\epsilon_{si}}[\Psi_{s2}(y)-V_G-\phi_{f1}] \quad (10)$$

where $\Psi_{b2}(y)=\Psi_2(0,y)$ and $\Psi_{s2}=\Psi_2(t_i,y)$ are back and front surface potentials, respectively. $t(y)$ is the distance from the right edge of the bottom gate to the back surface channel. Due to the fringing electric field, $t(y)$ is not a fixed value. From (9) and (10), the coefficients are shown in (11) at the bottom of the page. In addition, a relationship between front and back surface potential is

$$\Psi_{s2}(y)=\Psi_{b2}(y)-\frac{\epsilon_{ox}}{\epsilon_{si}t(y)}[V_G+\phi_{f2}-\Psi_{b2}(y)]t_i+\Gamma_{b2}(y)t_i^2. \quad (12)$$

Using a similar approximation approach as for the gate overlap region ($\Gamma_{b}\equiv(\partial^2\Psi_2(y)/\partial y^2)\cong(1/\epsilon_s)(\partial^2\Psi_{b2}(y)/\partial y^2)$, from (9) and (1), one obtains

$$\frac{\partial^2\Psi_{b2}(y)}{\partial y^2}=\kappa_s\left[\frac{\partial^2\Psi_2(y)}{\partial y^2}\right]=\kappa_s\left[\frac{qN_A}{\epsilon_{si}}-2\Gamma_{b2}(y)\right] \quad (13)$$

which is a differential equation in terms of the back surface potential. Due to the fringing electric field from the right edge of the bottom gate via the oxide to the thin-film interface, the above equation is difficult to calculate. In order to simplify the analysis, a conformal mapping transformation technique [15] has been used to transform the original $x\vec{X}+y\vec{Y}$ space in terms of the $\vec{X}$ and $\vec{Y}$ axes as shown in Fig. 2 to the $u\vec{U}+v\vec{V}$ space in terms of $\vec{U}$ and $\vec{V}$ axes based on the following transfer function:

$$(y-L_{m1})\vec{Y}+ux\vec{X}=k\sinh(u\vec{U}+v\vec{V})$$
$$L_{m1}=L_c-m_a$$
$$u=\frac{m_a}{t_{ox2}\sinh\left[\cosh^{-1}\left(\frac{t_{ox2}+t_{si2}}{t_{ox2}}\right)\right]}$$
$$k=\frac{m_a}{\sinh\left[\cosh^{-1}\left(\frac{t_{ox2}+t_{si2}}{t_{ox2}}\right)\right]}. \quad (14)$$

From the above formula, ABCD in the $x\vec{X}+y\vec{Y}$ coordinates is transformed into A'B'C'D' in the $u\vec{U}+v\vec{V}$ coordinates. As a result, the arc-shaped electric field contour in the oxide next to the right edge of the bottom gate in the $x\vec{X}+y\vec{Y}$ coordinates has become straight-line-shaped in the $u\vec{U}+v\vec{V}$ coordinates. Based on the transformation, the distance between the bottom gate electrode and the bottom thin-film/oxide interface $t(y)$, which is not a fixed value, has been transformed into $m\pi/2$, which is the distance between points A' and C' in the new coordinates under the condition $\sinh(m\pi/2)=1$. Therefore, after conformal mapping transformation ($t(y)\rightarrow m\pi/2$, $\Psi_{b2}(y)\rightarrow\Psi_v(v)$, $y-L_{m1}=k\sinh v$), a differential equation in terms of back surface potential Ψ_v in the $u\vec{U}+v\vec{V}$ coordinates has been obtained

$$\frac{\partial^2\Psi_v(v)}{\partial y^2}=\kappa_s\left[\frac{qN_A}{\epsilon_{si}}-2\alpha_0\Psi_v(v)-2\beta_0\right]$$
$$\alpha_0=-\frac{\left(1+\frac{2t_{ox1}}{m\pi k}+\frac{2t_{ox}}{m\pi kC_s}\right)}{t_i^2\left(1+\frac{2C_s}{C_{ox1}}\right)}$$
$$\beta_0=\frac{\left[1+\frac{2t_{ox1}}{m\pi k}+\frac{2t_{ox}}{m\pi kC_s}\right]V_G+\left[\frac{2t_{ox1}}{m\pi k}+\frac{2t_{ox}}{m\pi kC_s}\right]\phi_{f2}+\phi_{f1}}{t_i^2\left(1+\frac{2C_s}{C_{ox1}}\right)}. \quad (15)$$

$$\Gamma_{b2}(y)=\Psi_{b2}(y)$$
$$\Gamma_{12}(y)=-\frac{\epsilon_{ox}}{\epsilon_{si}t(y)}[V_G+\phi_{f2}-\Psi_{b2}(y)]$$
$$\Gamma_{22}(y)=\frac{-\left[1+\frac{2t_{ox1}}{t(y)k}+\frac{2t_{ox}}{t(y)kC_s}\right]\Psi_{b2}(y)+\left[1+\frac{2t_{ox1}}{t(y)k}+\frac{2t_{ox}}{t(y)kC_s}\right]V_G+\left[\frac{2t_{ox1}}{t(y)k}+\frac{2t_{ox}}{t(y)kC_s}\right]\phi_{f2}+\phi_{f1}}{t_i^2\left(1+\frac{2C_s}{C_{ox1}}\right)}. \quad (11)$$

In addition, after transformation, the coefficients become

$$\begin{aligned} F_{02}(v) &= \Psi_s(v) \\ F_{12}(v) &= -\frac{2\kappa_{ox}}{m\pi t_{ox}}[V_G + \phi_{fg} - \Psi_s(v)] \\ F_{22}(v) &= \alpha_0 \Psi_s(v) + \beta_0. \end{aligned} \tag{16}$$

Since

$$\begin{aligned} \frac{\partial^2 \Psi_s(v)}{\partial y^2} &= \frac{\partial}{\partial y}\left(\frac{\partial v}{\partial y}\frac{\partial \Psi_s(v)}{\partial v}\right) \\ &= \left(\frac{\partial v}{\partial y}\right)^2 \frac{\partial^2 \Psi_s(v)}{\partial v^2} + \left(\frac{\partial^2 v}{\partial y^2}\right)\frac{\partial \Psi_s(v)}{\partial v} \end{aligned}$$

the differential (15) could be rewritten as

$$\begin{aligned} \frac{\partial^2 \Psi_s(v)}{\partial v^2} - \tanh v \frac{\partial \Psi_s(v)}{\partial v} + 2\alpha_0 \kappa_s k^2 \cosh^2 v \Psi_s(v) \\ = \kappa_s k^2 \cosh^2 v \left[\frac{qN_A}{\epsilon_{si}} - 2\beta_0\right]. \end{aligned} \tag{17}$$

Equation (17) is a nonlinear differential equation, which is difficult to solve. In order to simplify the situation, one may assume that $a = \sinh v$ and thus, $(\partial \Psi_s/\partial a) = (\partial \Psi_s/\partial v)\cosh v$, and

$$\frac{\partial^2 \Psi_s}{\partial v^2} = \left(\frac{\partial^2 \Psi_s}{\partial a^2}\right)\cosh^2 v + \left(\frac{\partial \Psi_s}{\partial a}\right)\sinh v.$$

Via this, (17) is further simplified as a linear differential equation

$$\begin{aligned} \frac{\partial^2 \Psi_s}{\partial a^2} + B_0 \Psi_s &= B_1 \\ B_0 &= 2\kappa_s k^2 \alpha_0 \\ B_1 &= \kappa_s k^2 \left[\frac{qN_A}{\epsilon_{si}} - 2\beta_0\right]. \end{aligned} \tag{18}$$

Solving (18), one obtains the back surface potential in the $u\vec{U} + v\vec{V}$ coordinates as

$$\begin{aligned} \Psi_s &= g_1 \exp(\gamma a) + g_2 \exp(-\gamma a) + \frac{B_1}{B_0} \\ \gamma &= \sqrt{-B_0}. \end{aligned} \tag{19}$$

Using $\sinh v = y - L_m/k$ to transform back to the $x\vec{X} + y\vec{Y}$ coordinates, the back surface potential is

$$\Psi_{b2}(y) = g_1 \exp\left[\frac{\gamma}{k}(y - L_m)\right] + g_2 \exp\left[-\frac{\gamma}{k}(y - L_m)\right] + \frac{B_1}{B_0}. \tag{20}$$

C. Boundary Conditions

In this subsection, boundary conditions for back and front surface potentials are described.

1) Back Surface Potentials ($\psi_{b1}(y)$, $\psi_{b2}(y)$): For the back surface potentials in the gate overlap and the nongate overlap regions ($\Psi_{b1}(y)$, $\Psi_{b2}(y)$), the boundary conditions are that at the left ($y = 0$) and the right ($y = L_{ov}$) sides, they are determined by the source and the drain potentials

$$\begin{aligned} \Psi_{b1}(0) &= \phi_{fn} + V_S \\ \Psi_{b2}(L_{ov}) &= \phi_{fn} + V_D, \end{aligned} \tag{21}$$

where $\phi_{fn} = (kT/q)\ln(N_D/n_i)$, N_D is the source/drain doping density. At the boundary ($y = L_m$) between the gate overlap and the nongate overlap regions, the potential and the electric field are continuous. Thus

$$\begin{aligned} \Psi_{b1}(L_m) &= \Psi_{b2}(L_m) \\ \frac{\partial \Psi_{b1}}{\partial y}|_{y=L_m} &= \frac{\partial \Psi_{b2}}{\partial y}|_{y=L_m}. \end{aligned} \tag{22}$$

From $\Psi_{b1}(y)$, (8), and $\Psi_{b2}(y)$, (20), with four boundary conditions, (21) and (22), the coefficients are shown in (23) at the bottom of the page.

2) Front Surface Potential ($\psi_{s1}(y)$, $\psi_{s2}(y)$): From (11) and (12), a relationship between the front surface potential Ψ_{s2} and the back surface potential Ψ_{b2} in the nongate overlap region could be found as

$$\Psi_{s2}(y) = \frac{\sigma_2\left[\frac{2C_{ox}}{C_{ox1}} + \frac{t_{ox1}}{t(y)}\right]\Psi_{b2}(y) + \left[1 - \frac{t_{ox1}}{t(y)}\right]V_G - \left[\frac{t_{ox1}}{t(y)}\right]\phi_{fg} + \phi_{fj}}{1 + \frac{2C_{ox}}{C_{ox1}}} \tag{24}$$

where $\sigma_2 = 0.51 + 4m_a \times 10^4$ is an empirical correction factor to account for the nonsymmetric structure in the nongate overlap region. Note that m_a is the gate misalignment in centimeter.

$$C_1 = \frac{\left(\phi_{fn} + V_S + \frac{qN_A}{\beta_0}\right)\exp\left(-\sqrt{\beta_0}L_m\right)\left[\cosh\left(\frac{\gamma}{k}m_a\right) - \sinh\left(\frac{\gamma}{k}m_a\right)\frac{\sqrt{\beta_0}\alpha_0}{\gamma}\right] - \phi_{fn} - V_D + \frac{B_1}{B_0} - \left(\frac{qN_A}{\beta_0} + \frac{B_1}{B_0}\right)\cosh\left(\frac{\gamma}{k}m_a\right)}{-2\left[\sinh\left(\sqrt{\beta_0}L_m\right)\cosh\left(\frac{\gamma}{k}m_a\right) + \cosh\left(\sqrt{\beta_0}L_m\right)\sinh\left(\frac{\gamma}{k}m_a\right)\frac{\sqrt{\beta_0}\alpha_0}{\gamma}\right]}$$

$$C_2 = \frac{\left(\phi_{fn} + V_S + \frac{qN_A}{\beta_0}\right)\exp\left(\sqrt{\beta_0}L_m\right)\left[\cosh\left(\frac{\gamma}{k}m_a\right) + \sinh\left(\frac{\gamma}{k}m_a\right)\frac{\sqrt{\beta_0}\alpha_0}{\gamma}\right] - \phi_{fn} - V_D + \frac{B_1}{B_0} - \left(\frac{qN_A}{\beta_0} + \frac{B_1}{B_0}\right)\cosh\left(\frac{\gamma}{k}m_a\right)}{2\left[\sinh\left(\sqrt{\beta_0}L_m\right)\cosh\left(\frac{\gamma}{k}m_a\right) + \cosh\left(\sqrt{\beta_0}L_m\right)\sinh\left(\frac{\gamma}{k}m_a\right)\frac{\sqrt{\beta_0}\alpha_0}{\gamma}\right]}$$

$$g_1 = \frac{\left(\phi_{fn} + V_D - \frac{B_1}{B_0}\right)\left[\cosh\left(\sqrt{\beta_0}L_m\right) + \sinh\left(\sqrt{\beta_0}L_m\right)\frac{\gamma}{k\sqrt{\beta_0}}\right] + \left[\left(\frac{qN_A}{\beta_0} + \frac{B_1}{B_0}\right)\cosh\left(\sqrt{\beta_0}L_m\right) - \phi_{fn} - V_S - \frac{qN_A}{\beta_0}\right]\exp\left(-\frac{\gamma}{k}m_a\right)}{2\left[\cosh\left(\sqrt{\beta_0}L_m\right)\sinh\left(\frac{\gamma}{k}m_a\right) + \sinh\left(\sqrt{\beta_0}L_m\right)\cosh\left(\frac{\gamma}{k}m_a\right)\frac{\gamma}{k\sqrt{\beta_0}}\right]}$$

$$g_2 = \frac{\left(\phi_{fn} + V_D - \frac{B_1}{B_0}\right)\left[\cosh\left(\sqrt{\beta_0}L_m\right) - \sinh\left(\sqrt{\beta_0}L_m\right)\frac{\gamma}{k\sqrt{\beta_0}}\right] - \left[\left(\frac{qN_A}{\beta_0} + \frac{B_1}{B_0}\right)\cosh\left(\sqrt{\beta_0}L_m\right) + \phi_{fn} + V_S + \frac{qN_A}{\beta_0}\right]\exp\left(\frac{\gamma}{k}m_a\right)}{-2\left[\cosh\left(\sqrt{\beta_0}L_m\right)\sinh\left(\frac{\gamma}{k}m_a\right) + \sinh\left(\sqrt{\beta_0}L_m\right)\cosh\left(\frac{\gamma}{k}m_a\right)\frac{\gamma}{k\sqrt{\beta_0}}\right]}$$

(23)

From (4) and (5), a relationship between the front surface potential Ψ_{s1} and the back surface potential Ψ_{b1} in the gate overlap region has been found as

$$\Psi_{s1}(y)=\frac{\sigma_1\left[\frac{2C_o}{C_{ox1}}+\frac{C_{dep}}{C_{ox1}}\right]\Psi_{b1}(y)+\left[1-\frac{C_{dep}}{C_{ox1}}\right]V_G-\left[\frac{C_{dep}}{C_{ox1}}\right]\phi_{f2}+\phi_{f1}}{1+\frac{2C_o}{C_{ox1}}} \tag{25}$$

where $\sigma_1=0.09-2m_a\times10^5$ is an empirical correction factor.

From (20) and (24) and (8) and (25), the front surface potentials are

$$\begin{aligned}\Psi_{s1}(y)&=C_3\exp\left(\sqrt{A_0}y\right)+C_4\exp\left(-\sqrt{A_0}y\right)-D_1\\ \Psi_{s2}(y)&=g_2\exp\left[\frac{\gamma}{k}(y-L_{ov})\right]+g_1\exp\left[-\frac{\gamma}{k}(y-L_{ov})\right]+D_2\\ D_1&=\frac{\sigma_1\left[\frac{2C_o}{C_{ox1}}+\frac{C_{dep}}{C_{ox1}}\right]\frac{A_1}{A_0}+\left[\frac{C_{dep}}{C_{ox1}}-1\right]V_G+\left[\frac{C_{dep}}{C_{ox1}}\right]\phi_{f2}-\phi_{f1}}{1+\frac{2C_o}{C_{ox1}}}\\ D_2&=\frac{\sigma_2\left[\frac{2C_o}{C_{ox2}}+\frac{L_{ov}}{\theta(y)}\right]\frac{B_1}{B_0}+\left[1-\frac{L_{ov}}{\theta(y)}\right]V_G-\left[\frac{L_{ov}}{\theta(y)}\right]\phi_{f2}+\phi_{f1}}{1+\frac{2C_o}{C_{ox2}}},\end{aligned} \tag{26}$$

For the front surface potentials in the gate overlap and the nongate overlap regions ($\Psi_{s1}(y)$, $\Psi_{s2}(y)$), the boundary conditions are that at the left ($y=0$) and the right($y=L_{ch}$) sides, they are determined by the source and the drain potentials:

$$\begin{aligned}\Psi_{s1}(0)&=\phi_{fn}+V_S\\ \Psi_{s2}(L_{ch})&=\phi_{fn}+V_D.\end{aligned} \tag{27}$$

At the boundary ($y=L_{ov}$) between the gate overlap and the nongate overlap regions, the potential and the electric field are continuous. Thus

$$\begin{aligned}\Psi_{s1}(L_{ov})&=\Psi_{s2}(L_{ov})\\ \frac{\partial\Psi_{s1}}{\partial y}|_{y=L_{ov}}&=\frac{\partial\Psi_{s2}}{\partial y}|_{y=L_{ov}}.\end{aligned} \tag{28}$$

Using the boundary conditions (26)–(28), the coefficients in the front surface potentials in the gate overlap and the nongate overlap regions [(26)] are shown in (29) at the bottom of the page.

3) Threshold Voltage: The threshold voltage of the device is defined as the gate voltage when the sum of the electron densities at the locations in the front and the back surface channels with their respective minimum potentials equal to the doping density of the thin film

$$N_A=n_i\exp\left(\frac{\Psi_{s\min}}{V_T}\right)+n_i\exp\left(\frac{\Psi_{b\min}}{V_T}\right), \tag{30}$$

where $\Psi_{s\min}$ and $\Psi_{b\min}$ are the minimum front and back surface potentials, respectively. Note that (30) is not applicable for the thin film with a zero or very light doping density, where N_A should be replaced by $J/q\mu_n E$ (J is the predefined current density, μ_n is the electron mobility, and E is the lateral electric field). In the gate overlap region, from $\partial\Psi_{b1}/\partial y=0$, the minimum back surface potential is $\Psi_{b1\min}=2\sqrt{C_3C_4}-A_1/A_0$ at $y_{b1\min}=-(1/2\sqrt{A_0})\ln(C_3/C_4)$. In the nongate overlap region, from $\partial\Psi_{b2}/\partial y=0$, the minimum back surface potential is $\Psi_{b2\min}=2\sqrt{g_1g_2}+B_1/B_0$ at $y_{b2\min}=L_{ov}-(k/2\gamma)\ln(g_1/g_2)$. From $\Psi_{b1\min}$ and $\Psi_{b2\min}$, $\Psi_{b\min}$ could be determined. Similarly, the minimum front surface potential in the gate overlap region is $\Psi_{s1\min}=2\sqrt{C_3C_4}-D_1$, $y_{s1\min}=-(1/2\sqrt{A_0})\ln(C_3/C_4)$. The minimum front surface potential in the nongate overlap region is: $\Psi_{s2\min}=2\sqrt{g_1g_4}+D_2$, $y_{s2\min}=L_{ov}-(k/2\gamma)\ln(g_2/g_4)$. From $\Psi_{s1\min}$ and $\Psi_{s2\min}$, $\Psi_{s\min}$ could be found. As shown in Fig. 5(a), the minimum front surface potential ($\Psi_{s\min}$) is higher than the minimum back surface potential($\Psi_{b\min}$). Therefore, the second term in (30) can be neglected. If the minimum front surface potential occurs in the nongate overlap region, $\Psi_{s\min}=\Psi_{s2\min}$ and $y_{s2\min}=L_{ov}-(k/2\gamma)\ln(g_2/g_1)>L_{ov}$, hence $g_1<g_4$, which can be reorganized as

$$\begin{aligned}&(\phi_{fn}+V_D-D_2)\cosh\left(\sqrt{A_0}L_{ov}\right)+\left[\phi_{fn}+V_s+D_1\right.\\ &\qquad\left.-(D_1+D_2)\cosh\left(\sqrt{A_0}L_{ov}\right)\right]\sinh\left(\frac{\gamma}{k}m_a\right)<0\end{aligned}$$

using (29). Under this situation, from (30), the threshold voltage is

$$V_{th}=\frac{-Z_2-\sqrt{Z_2^2-4Z_1Z_3}}{2Z_1} \tag{31}$$

$$\begin{aligned}C_3&=\frac{(\phi_{fn}+V_S+D_1)\exp\left(-\sqrt{A_0}L_{ov}\right)\left[\cosh\left(\frac{\gamma}{k}m_a\right)-\sinh\left(\frac{\gamma}{k}m_a\right)\frac{\sqrt{A_0}k}{\gamma}\right]-\phi_{fn}-V_D+D_2-(D_1+D_2)\cosh\left(\frac{\gamma}{k}m_a\right)}{-2\left[\sinh(\sqrt{A_0}L_{ov})\cosh(\frac{\gamma}{k}m_a)+\cosh(\sqrt{A_0}L_{ov})\sinh(\frac{\gamma}{k}m_a)\frac{\sqrt{A_0}k}{\gamma}\right]}\\ C_4&=\frac{(\phi_{fn}+V_S+D_1)\exp\left(\sqrt{A_0}L_{ov}\right)\left[\cosh(\frac{\gamma}{k}m_a)+\sinh(\frac{\gamma}{k}m_a)\frac{\sqrt{A_0}k}{\gamma}\right]-\phi_{fn}-V_D+D_2-(D_1+D_2)\cosh\left(\frac{\gamma}{k}m_a\right)}{2\left[\sinh\left(\sqrt{A_0}L_{ov}\right)\cosh\left(\frac{\gamma}{k}m_a\right)+\cosh\left(\sqrt{A_0}L_{ov}\right)\sinh\left(\frac{\gamma}{k}m_a\right)\frac{\sqrt{A_0}k}{\gamma}\right]}\\ g_1&=\frac{(\phi_{fn}+V_D-D_2)\left[\cosh\left(\sqrt{A_0}L_{ov}\right)+\sinh\left(\sqrt{A_0}L_{ov}\right)\frac{\gamma}{k\sqrt{A_0}}\right]+\left[(D_1+D_2)\cosh\left(\sqrt{A_0}L_{ov}\right)-\phi_{fn}-V_S-D_1\right]\exp\left(-\frac{\gamma}{k}m_a\right)}{2\left[\cosh\left(\sqrt{A_0}L_{ov}\right)\sinh\left(\frac{\gamma}{k}m_a\right)+\sinh\left(\sqrt{A_0}L_{ov}\right)\cosh\left(\frac{\gamma}{k}m_a\right)\frac{\gamma}{k\sqrt{A_0}}\right]}\\ g_2&=\frac{(\phi_{fn}+V_D-D_2)\left[\cosh(\sqrt{A_0}L_{ov})-\sinh(\sqrt{A_0}L_{ov})\frac{\gamma}{k\sqrt{A_0}}\right]-\left[(D_1+D_2)\cosh\left(\sqrt{A_0}L_{ov}\right)+\phi_{fn}+V_S+D_1\right]\exp\left(\frac{\gamma}{k}m_a\right)}{-2\left[\cosh\left(\sqrt{A_0}L_{ov}\right)\sinh\left(\frac{\gamma}{k}m_a\right)+\sinh\left(\sqrt{A_0}L_{ov}\right)\cosh\left(\frac{\gamma}{k}m_a\right)\frac{\gamma}{k\sqrt{A_0}}\right]}.\end{aligned} \tag{29}$$

$$Z_1 = K_1^2 + \frac{d_2 d_4}{f_0^2}$$
$$Z_2 = 2E_3\left(E_4 - \frac{kT}{q}\ln\left(\frac{N_A}{n_i}\right)\right) + \frac{d_1 d_4 + d_2 d_3}{f_0^2}$$
$$Z_3 = \left(E_4 - \frac{kT}{q}\ln\left(\frac{N_A}{n_i}\right)\right)^2 + \frac{d_3 d_3}{f_0^2} \tag{32}$$

$$d_1 = (\phi_{fs} + V_D - E_4)\left[\cosh\left(\sqrt{A_0}L_{ss}\right) + \sinh\left(\sqrt{A_0}L_{ss}\right)\frac{\gamma}{k\sqrt{A_0}}\right] + \left[-\phi_{fs} - V_S - E_2 + (E_2 + E_4)\cosh\left(\sqrt{A_0}L_{ss}\right)\right]\exp\left(-\frac{\gamma}{k}m_s\right)$$
$$d_2 = -E_3\left[\cosh\left(\sqrt{A_0}L_{ss}\right) + \sinh\left(\sqrt{A_0}L_{ss}\right)\frac{\gamma}{k\sqrt{A_0}}\right] + \left[-E_1 + (E_1 + E_3)\cosh\left(\sqrt{A_0}L_{ss}\right)\right]\exp\left(-\frac{\gamma}{k}m_s\right)$$
$$d_3 = (\phi_{fs} + V_D - E_4)\left[\cosh\left(\sqrt{A_0}L_{ss}\right) - \sinh\left(\sqrt{A_0}L_{ss}\right)\frac{\gamma}{k\sqrt{A_0}}\right] + \left[-\phi_{fs} - V_S - E_2 + (E_2 + E_4)\cosh\left(\sqrt{A_0}L_{ss}\right)\right]\exp\left(\frac{\gamma}{k}m_s\right)$$
$$d_4 = -E_3\left[\cosh\left(\sqrt{A_0}L_{ss}\right) - \sinh\left(\sqrt{A_0}L_{ss}\right)\frac{\gamma}{k\sqrt{A_0}}\right] + \left[-E_1 + (E_1 + E_3)\cosh\left(\sqrt{A_0}L_{ss}\right)\right]\exp\left(\frac{\gamma}{k}m_s\right) \tag{33}$$

$$E_1 = \frac{C_{ox2} - C_{ox1} - \sigma_1(2C_s + C_{ox2})}{C_{ox1} + 2C_s}$$
$$E_2 = \frac{C_{ox2}\phi_{f2} - C_{ox1}\phi_{f1} + \sigma_1(2C_s + C_{ox2})A_2}{C_{ox1} + 2C_s}$$
$$E_3 = \frac{C_{ox1} - \frac{\varepsilon_{ox}}{t(y)} + \sigma_2\left(2C_s + \frac{\varepsilon_{ox}}{t(y)}\right)}{C_{ox2} + 2C_s}$$
$$E_4 = \frac{C_{ox1}\phi_{f1} - \frac{\varepsilon_{ox}}{t(y)}\phi_{f2} + \sigma_2\left(2C_s + \frac{\varepsilon_{ox}}{t(y)}\right)B_2}{C_{ox1} + 2C_s} \tag{34}$$

$$A_2 = \frac{\frac{1}{2}qN_A t_s^2\left(1 + \frac{2C_s}{C_{ox1}}\right) - \epsilon_{si}\left(\frac{C_{ox2}}{C_s} + \frac{C_{ox2}}{C_{ox1}}\right)\phi_{f2} - \epsilon_{si}\phi_{f1}}{\epsilon_{si}\left(1 + \frac{C_{ox2}}{C_s} + \frac{C_{ox2}}{C_{ox1}}\right)}$$
$$B_2 = \frac{-qN_A t_s^2\left(1 + \frac{2C_s}{C_{ox1}}\right) + \epsilon_{si}\left(\frac{2\epsilon_{si}}{t_{ox2}} + \frac{2\epsilon_{ox}}{t_{ox2}C_s}\right)\phi_{f2} + \epsilon_{si}\phi_{f1}}{\epsilon_{si}\left(1 + \frac{2\epsilon_{si}}{t_{ox2}} + \frac{2\epsilon_{ox}}{t_{ox2}C_s}\right)} \tag{35}$$

$$p_0 = \cosh\left(\sqrt{A_0}L_{ss}\right)\sinh\left(\frac{\gamma}{k}m_s\right) + \sinh\left(\sqrt{A_0}L_{ss}\right)\cosh\left(\frac{\gamma}{k}m_s\right)\frac{\gamma}{k\sqrt{A_0}}. \tag{36}$$

On the other hand, when

$$(\phi_{fs} + V_D - D_2)\cosh\left(\sqrt{A_0}L_{ss}\right) + [\phi_{fs} + V_s + D_1 - (D_1 + D_2)\cosh\left(\sqrt{A_0}L_{ss}\right)]\sinh\left(\frac{\gamma}{k}m_s\right) > 0$$

($g_3 > g_1$) the minimum front surface potential occure in the gate overlap region, which means $\Psi_{s\,min} = \Psi_{s1\,side}$. Thus, the threshold voltage becomes

$$V_{th} = \frac{-X_2 - \sqrt{X_2^2 - 4X_1X_3}}{2X_1} \tag{37}$$

$$X_1 = K_1^2 + \frac{b_2 b_4}{f_0^2}$$
$$X_2 = 2E_3\left(E_2 + \frac{kT}{q}\ln\left(\frac{N_A}{n_i}\right)\right) + \frac{b_1 b_4 + b_2 b_3}{f_0^2}$$
$$X_3 = \left(E_2 + \frac{kT}{q}\ln\left(\frac{N_A}{n_i}\right)\right)^2 + \frac{b_3 b_3}{f_0^2} \tag{38}$$

$$b_1 = (\phi_{fs} + V_S + E_2)\exp\left(-\sqrt{A_0}L_{ss}\right)\cdot\left[\cosh\left(\frac{\gamma}{k}m_s\right) - \sinh\left(\frac{\gamma}{k}m_s\right)\frac{\sqrt{A_0}k}{\gamma}\right] - \phi_{fs} - V_D + E_1 - (E_2 + E_4)\cosh\left(\frac{\gamma}{k}m_s\right)$$
$$b_2 = E_1\exp\left(-\sqrt{A_0}L_{ss}\right)\left[\cosh\left(\frac{\gamma}{k}m_s\right) - \sinh\left(\frac{\gamma}{k}m_s\right)\frac{\sqrt{A_0}k}{\gamma}\right] + E_3 - (E_1 + E_3)\cosh\left(\frac{\gamma}{k}m_s\right)$$
$$b_3 = (\phi_{fs} + V_S + E_2)\exp\left(\sqrt{A_0}L_{ss}\right)\cdot\left[\cosh\left(\frac{\gamma}{k}m_s\right) + \sinh\left(\frac{\gamma}{k}m_s\right)\frac{\sqrt{A_0}k}{\gamma}\right] - \phi_{fs} - V_D + E_4 - (E_2 + E_4)\cosh\left(\frac{\gamma}{k}m_s\right)$$
$$b_4 = E_1\exp\left(\sqrt{A_0}L_{ss}\right)\left[\cosh\left(\frac{\gamma}{k}m_s\right) + \sinh\left(\frac{\gamma}{k}m_s\right)\frac{\sqrt{A_0}k}{\gamma}\right] + E_3 - (E_1 + E_3)\cosh\left(\frac{\gamma}{k}m_s\right) \tag{39}$$
$$f_0 = \sinh\left(\sqrt{A_0}L_{ss}\right)\cosh\left(\frac{\gamma}{k}m_s\right) + \cosh\left(\sqrt{A_0}L_{ss}\right)\sinh\left(\frac{\gamma}{k}m_s\right)\frac{\sqrt{A_0}k}{\gamma}. \tag{40}$$

Note that the threshold voltage formula as shown in (31) and (37) is a function of the physical parameters of the DG SOI device as shown in related equations.

4) Without Considering the Fringing Effect: If the fringing electric field effect from the right edge of the bottom gate is not considered ($\partial\Psi_2(x,y)/\partial x|_{x=0} = 0$), from (10), one obtains $P_{12} = 0$, $P_{02} = \Psi_{b2}$, and $P_{22} = (-\Psi_{s2} + V_G + \phi_{f1})/((1/2)t_s^2(1 + 2C_s/C_{ox2}))$. From (13), the differential equation in terms of the back surface potential is

$$\frac{\partial^2\Psi_{s2}}{\partial y^2} - \frac{2\kappa_s}{t_s^2\left(1 + \frac{2C_{ox}}{C_{ox2}}\right)}\Psi_{s2} = \kappa_s\left[\frac{qN_a}{\epsilon_{si}} - \frac{2(V_G + \phi_{f1})}{t_s^2\left(1 + \frac{2C_{ox}}{C_{ox2}}\right)}\right]. \tag{41}$$

Thus, (20) is still applicable except that B_1/B_0 and γ/k are replaced by $B_1/B_0 = V_G + \phi_{f1} - (2\gamma_s^2 N_a/\epsilon_{si})t_s^2(1 + 2C_s/C_{ox1})$ and $\gamma/k = \sqrt{2\kappa_s/t_s^2(1 + 2C_s/C_{ox1})}$.

III. Model Evaluation

In order to assess the effectiveness of the analytical model for the gate misalignment effect of the DG SOI nMOS devices, the model results have been compared with the 2-D simulation results. Fig. 3 shows (a) back and (b) front surface potential distributions of the DG SOI nMOS device with a channel length of 0.2 μm, n^+ polysilicon top and bottom gates, a gate oxide of 70 Å, a thin film of 600 Å, doped with a p-type density of 4×10^{17} cm^{-3}, and various gate misalignments biased at $V_G =$

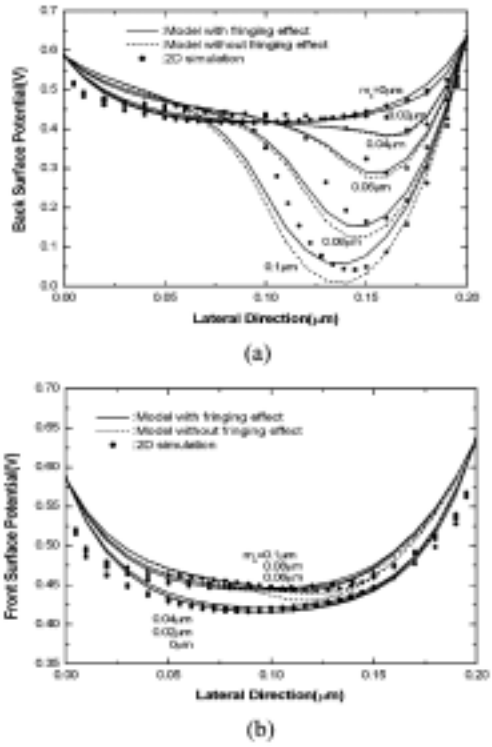

Fig. 3. (a) Back and (b) front surface potential distributions of the DG SOI nMOS device with a channel length of 0.2 μm, n^+ polysilicon top and bottom gates, a gate oxide of 70 Å, a thin film of 600 Å doped with a p-type density of 4×10^{17} cm^{-3}, and various gate misalignments biased at $V_G = V_{th}$ and $V_D = 50$ mV, based on the analytical model with and without considering fringing electric field effect, and 2-D simulation results.

V_{th} and $V_D = 50$ mV, based on the analytical model with and without considering the fringing electric field effect, and the 2-D simulation results.

As shown in the Fig. 3(a), when the gate misalignment increases, the back surface potential is lowered in the nongate overlap region. Considering the fringing electric field effect due to gate misalignment, the dip in the back surface potential becomes smaller as compared to the case without considering it. In addition, when the gate misalignment becomes larger, the fringing electric field effect becomes more important. As shown in Fig. 3(b), when the gate misalignment becomes larger, the fringing electric field effect on the front surface potential becomes more noticeable. In addition, a larger gate misalignment leads to a lower minimum front surface potential, which is also due to the fringing electric field effect. As shown in Fig. 3(a) and (b), the analytical model considering the fringing electric field effect could predict front and back surface potential distributions consistently as verified by the 2-D simulation results.

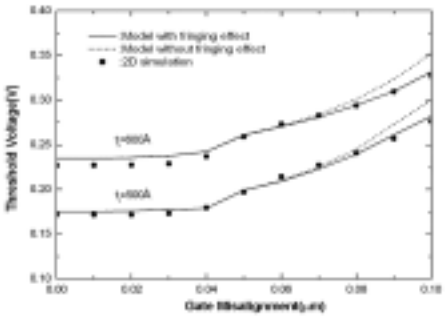

Fig. 4. Threshold voltage versus gate misalignment of the DG SOI nMOS device with a channel length of 0.2 μm, n^+ polysilicon top and bottom gates, a gate oxide of 70 Å, and a thin film of 500 Å and 600 Å doped with a p-type density of 4×10^{17} cm^{-3}, based on the analytical model with and without considering fringing electric field effect and 2-D simulation results.

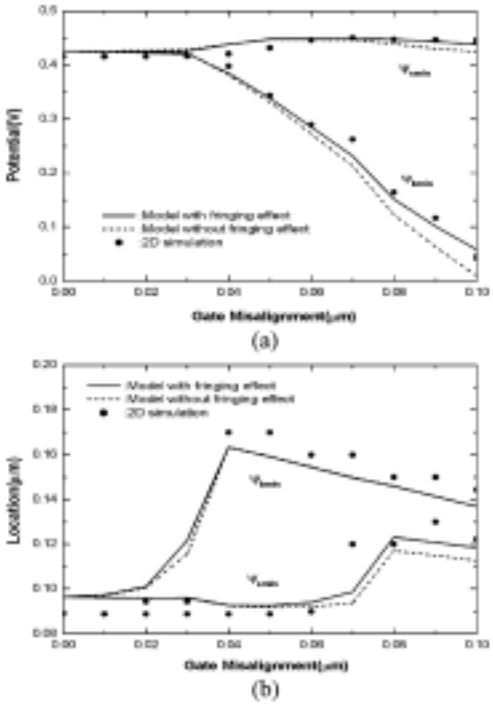

Fig. 5. (a) Minimum front and back surface potentials and (b) their locations versus gate misalignment of the DG SOI nMOS device with a channel length of 0.2 μm, n^+ polysilicon top and bottom gates, a gate oxide of 70 Å, and a thin film of 600 Å doped with a p-type density of 4×10^{17} cm^{-3}, biased at $V_G = V_{th}$ and $V_D = 50$ mV.

Fig. 4 shows the threshold voltage versus the gate misalignment of the DG SOI nMOS device with a channel length of 0.2 μm, n^+ polysilicon top and bottom gates, a gate oxide of

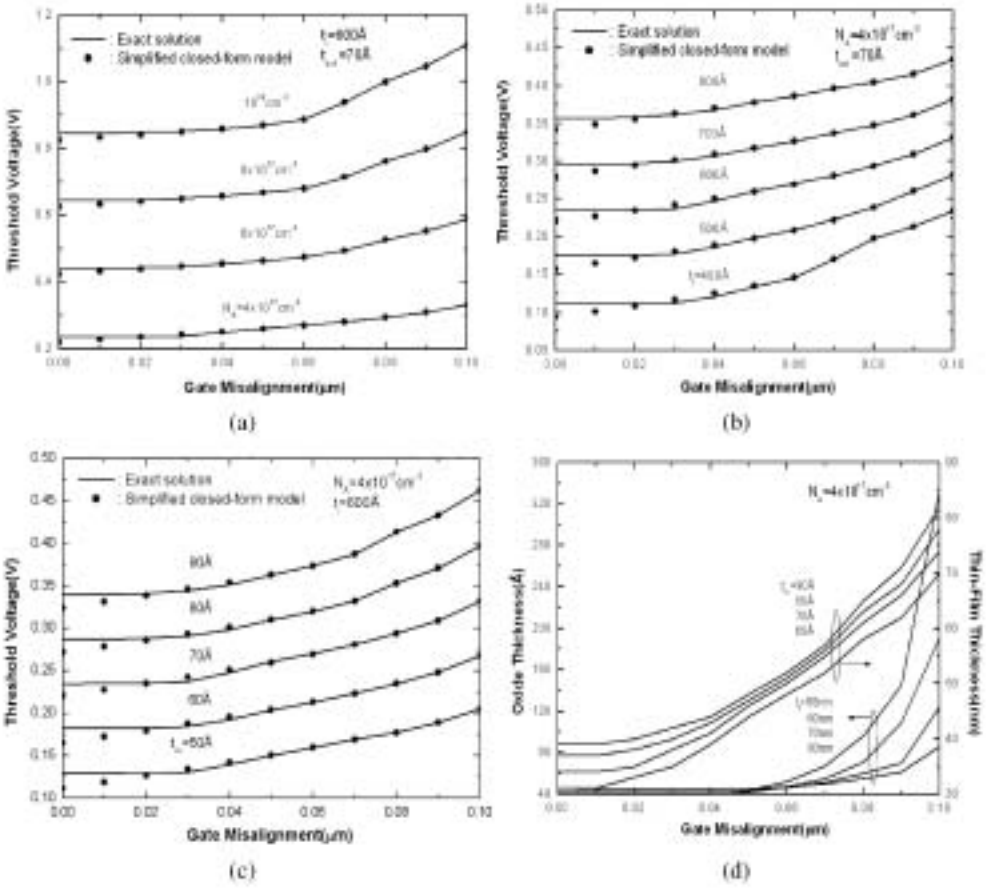

Fig. 6. Threshold voltage versus the gate misalignment of the DG SOI nMOS device with various (a) thin-film doping densities, (b) thin-film thicknesses, and (c) gate oxide thicknesses, using the exact solution from (30) and the simplified closed-form model [(31)–(40)]. (d) Criterion for selecting (31)–(36) or (37)–(40) for the threshold voltage.

70 Å, and a thin film of 500 and 600 Å doped with a p-type density of 4×10^{17} cm^{-3}, based on the analytical model with and without considering the fringing electric field effect and the 2-D simulation results. As shown in the figure, for both cases with a thin film of 500 and 600 Å, the fringing electric field effect coming from the gate misalignment is important in determining the threshold voltage. Without considering the fringing electric field effect, the threshold voltage is over-estimated, which is more noticeable when the gate misalignment becomes larger. At a gate misalignment of 0.1 μm, the fringing electric field effect causes a reduction in threshold voltage about 0.022 V (6%) for the thin film of 600 Å and 0.028 V (7%) for 500 Å. As shown in the figure, and verified by the 2-D simulation results, the analytical model considering the fringing electric field effect could provide an accurate prediction of the threshold voltage.

IV. Discussion

Fig. 5 shows (a) minimum front and back surface potentials and (b) their locations versus gate misalignment of the DG SOI nMOS device with a channel length of 0.2 μm, n^+ polysilicon top and bottom gates, a gate oxide of 70 Å, and a thin film of 600 Å doped with a p-type density of 4×10^{17} cm^{-3}, biased at $V_G = V_{th}$ and $V_D = 50$ mV. As shown in Fig. 5(a) and (b), when the gate misalignment is smaller than 0.03 μm, the minimum front and back surface potentials are about equal, located in the gate overlap region. As the gate misalignment increases, the location of the minimum back surface potential moves toward the drain. At a gate misalignment of 0.04 μm, the minimum is located in the nongate overlap region. A further increase in the gate misalignment leads to a situation in which the

location of the minimum back surface potential moves toward the source slightly. A similar situation exists for the front surface, but its transition point is located at a gate misalignment of 0.08 μm. When the gate misalignment is greater than 0.08 μm, the location of the minimum front surface potential moves into the nongate overlap region. As shown in the figure, as verified by the 2-D simulation results, the analytical model considering the fringing electric field effect predicts the behavior closely.

The closed-form analytical model developed in this paper is useful for providing insightful understanding while doing device design of DG SOI devices. Fig. 6 shows the threshold voltage versus the gate misalignment of the DG SOI nMOS device with various (a) thin-film doping densities, (b) thin-film thicknesses, and (c) gate oxide thicknesses, using the exact solution from (30) and the simplified closed-form model [(31)–(40)] and (d) the criterion for selecting (31)–(36) or (37)–(40) for the threshold voltage. As shown in Fig. 6(a)–(c), as the gate misalignment increases, the threshold voltage increases. When the thin-film doping density is raised, the threshold voltage becomes more sensitive to the gate misalignment [Fig. 6(a)]. At a doping density of 4×10^{17} cm^{-3}, with a gate misalignment of 0.1 μm, the threshold voltage is increased by 0.1 V, while at a doping density of 10^{16} cm^{-3}, it is increased by 0.27 V. As shown in Fig. 6(b), when the thickness of the thin film is reduced, the threshold voltage becomes more sensitive to the gate misalignment. With a thin film of 800 Å, at a gate misalignment of 0.1 μm, its threshold voltage becomes larger by 0.077 V, while with a thin film of 400 Å, it is increased by 0.124 V. As shown in Fig. 6(c), as the gate oxide thickness becomes smaller, the sensitivity of the gate misalignment effect becomes smaller. At a gate oxide of 90 Å, with a gate misalignment of 0.1 μm, the threshold voltage is increased by 0.123 V, while at 50 Å, it is increased by 0.076 V. Therefore, to minimize the gate misalignment effect, the thin film should not be too thin and its doping density should not be too high. In addition, the gate oxide thickness should be reduced to minimize the gate misalignment effect. From Fig. 6(a)–(c), as confirmed by the exact solution results using (30), the simplified closed-form model [(31)–(40)] could provide an accurate prediction of the gate misalignment effect. As described in the model derivation section, while deriving the threshold voltage, the minimum front surface potential in either the gate overlap ($\Psi_{s1\min}$) or the gate nonoverlap ($\Psi_{s2\min}$) region has been used depending on its location. As described before, when

$$(\phi_{fn}+V_D-D_2)\cosh\left(\sqrt{A_0}L_{ov}\right)+[\phi_{fn}+V_s+D_1 -(D_1+D_2)\cosh\left(\sqrt{A_0}L_{ov}\right)]\sinh\left(\frac{\gamma}{R}m_a\right)<0$$

which implies $g_3 < g_4$, the minimum front surface potential occurs in the gate nonoverlap region—$\Psi_{s\min} = \Psi_{s2\min}$ and (31)–(36) should be used. Otherwise, (37)–(40) should be used. The above equation is a function of the gate oxide thickness, and the thickness and the doping density of the thin film. Based on this reasoning, Fig. 6(d) shows the selection criterion for various gate oxide and thin-film thicknesses. As shown in the figure, for each case, to the right of the curve, $\Psi_{s2\min}$ should be used in the threshold voltage formula [(31)–(36)] since the gate nonoverlap region dominates. To the left of the curve, $\Psi_{s1\min}$ should be used since the gate overlap region is more important. When the gate oxide becomes thinner, the curve moves toward the right direction, which indicates that the possibility of the dominance of $\Psi_{s2\min}$ in the gate nonoverlap region becomes smaller. When the thin film becomes thinner, the curve moves toward the left direction, which implies the increased chance of the dominance of $\Psi_{s2\min}$.

V. Conclusion

In this paper, an analysis of the gate misalignment effect on the threshold voltage of DG FD SOI nMOS devices using a compact model considering the fringing electric field effect has been described. Using the conformal mapping transformation approach, a closed-form compact model considering the fringing electric field effect above the nongate overlap region has been derived, in order to provide an accurate prediction of the threshold voltage behavior, as verified by the 2-D simulation results.

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附件

出席國際會議心得報告及發表論文

報告者 台大電機郭正邦

本人於 2003 年十一月出席於美國佛羅里達舉行的 IEEE International Conference on Electron Devices for Microwave and Optoelectronic Applications. 發表了論文 Analysis of Gate Misalignment Effect on the Threshold Voltage of Double-Gate (DG) Ultrathin FD SOI NMOS Devices Using a Compact Model Considering Fringing Electric Field Effect. 此論為此研究計畫的結晶 由於需上課 來去匆匆在佛羅里達只停留兩天一夜

Analysis of Gate Misalignment Effect on the Threshold Voltage of Double-Gate (DG) Ultrathin Fully-Depleted (FD) Silicon-On-Insulator (SOI) NMOS Devices Using a Compact Model Considering Fringing Electric Field Effect

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Abstract

This paper reports an analysis of gate misalignment effect on the threshold voltage of double-gate ultrathin fully-depleted (FD) silicon-on-insulator (SOI) NMOS devices using a compact model considering fringing electric field effect. Using the conformal mapping transformation approach, a closed-form compact model considering the fringing electric field effect above the non-gate overlap region has been derived to provide an accurate prediction of the threshold voltage behavior as verified by the 2D simulation results.

1. Introduction

SOI technology has been regarded as another mainstream technology for CMOS VLSI[1]. DG SOI technology has demonstrated its advantages for realizing sub-100nm CMOS devices[2]-[4]. For DG SOI CMOS devices, the gate misalignment effects have a deep impact on device performance[5]. Fig. 1 shows the 2D electric field contours in a DG SOI NMOS device with a gate oxide thickness of 70Å, a thin-film of 600Å doped with a p-type density of $4 \times 10^{17}cm^{-3}$, and a gate misalignment of 0.04μm, biased at $V_{GS} = V_{th}$, and $V_{DS} = 50mV$. As shown in the figure, the fringing electric field from the right edge of the bottom gate to the thin-film of the non-gate overlap region is substantial, which could cause non-negligible influence in device performance. In this paper, an analysis of gate misalignment effect on the threshold voltage of DG ultrathin FD SOI NMOS devices using a compact model considering fringing electric field effect is reported. It will be shown that using the conformal mapping transformation approach, this closed-form compact model considering the fringing electric field effect in the non-gate overlap region could provide an accurate prediction of the threshold voltage behavior as verified by the 2D simulation results. In the following sections, derivation of the analytical model is described, followed by model verification and discussion.

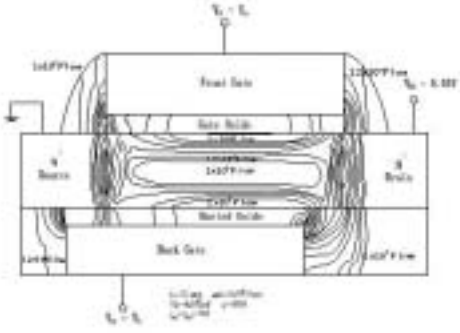


Figure 1: 2D electric field contours in a DG SOI NMOS device with n^+ polysilicon top and bottom gates, a gate oxide of 70Å, a thin-film of 600Å doped with a p-type density of $4 \times 10^{17}cm^{-3}$, and a gate misalignment of 0.04μm, biased at $V_{GS} = V_{th}$ and $V_{DS} = 50mV$.

2. Analytical Model

Fig. 2(a) shows the cross section of the DG SOI NMOS device with a gate misalignment. 2D Poisson's equation $\frac{\partial^2\Psi(x,y)}{\partial x^2} + \frac{\partial^2\Psi(x,y)}{\partial y^2} = \frac{qN_A}{\varepsilon_{si}}$ has been used for solving the electrostatic potential in the thin-film region, which is divided into (I) gate overlap and (II) non-gate overlap regions. In the gate overlap region, a conventional approach [6] has been used to solve the 2D Poisson's equation. In the non-gate overlap region, its electrostatic potential could be approximated as: $\Psi_2(x,y) = P_{02}(y) + P_{12}(y)x + P_{22}(y)x^2$. From Gauss Law at bottom and top oxide/thin-film interfaces, the boundary condi-

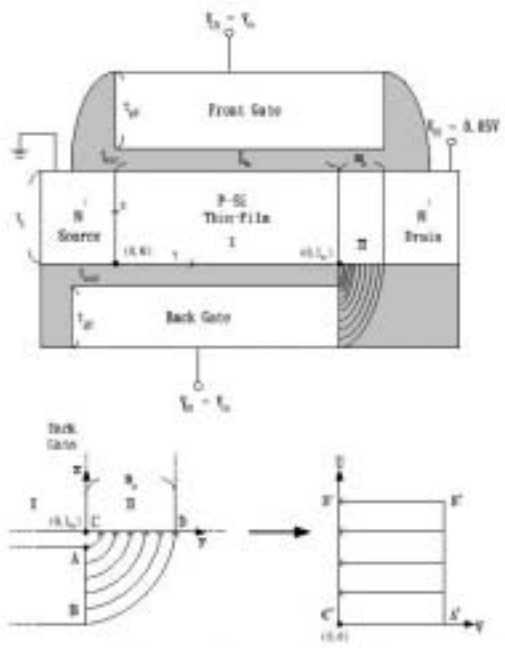


Figure 2: (a) Cross section of the DG SOI NMOS device with a gate misalignment and (b) the boundary of the sidewall oxide region next to the right edge of the bottom gate before and after conformal mapping for model derivation.

tions are: $-\frac{\partial\Psi_2(x,y)}{\partial x}|_{x=0} = \frac{\varepsilon_{ox}}{\varepsilon_{si}t(y)}[V_g + \Phi_{f2(poly)} - \Psi_{b2}(y)]$, $-\frac{\partial\Psi_2(x,y)}{\partial x}|_{x=t_{si}} = \frac{C_{ox1}}{\varepsilon_{si}}[\Psi_{s2}(y) - V_g - \Phi_{f1(poly)}]$. Using a decoupled approach ($\frac{\partial^2\Psi_2(y)}{\partial y^2} \cong \frac{1}{\varepsilon_{si}}\frac{\partial^2\Psi_{b2}(y)}{\partial y^2}$), one could obtain a differential equation in terms of the electrostatic potential at the bottom interface (Ψ_{b2}) as: $\frac{\partial^2\Psi_{b2}(y)}{\partial y^2} = \kappa_i(\frac{qN_A}{\varepsilon_{si}} - 2(\frac{-[1+\frac{t_{ox2}}{t(y)}+\frac{\varepsilon_{si}t_{ox}}{t(y)\varepsilon_{ox}}]\Psi_{b2}(y)+[1+\frac{t_{ox2}}{t(y)}+\frac{\varepsilon_{si}t_{ox}}{t(y)\varepsilon_{ox}}]V_g+[\frac{t_{ox2}}{t(y)}+\frac{\varepsilon_{si}t_{ox}}{t(y)\varepsilon_{ox}}]\Phi_{f2}+\Phi_{gs}}{\frac{\varepsilon_{si}}{C_{ox1}}(1+2\frac{\varepsilon_{si}}{\varepsilon_{ox}t_{ox1}})}$

Due to the fringing electric field from the right edge of the bottom gate via the oxide to the thin-film interface, the above equation is difficult to calculate. In order to simplify the analysis, a conformal mapping transformation technique [7] has been used to transform the original $x\vec{X} + y\vec{Y}$ space in terms of the $\vec{X}$ and $\vec{Y}$ as shown in Fig. 2 to the $u\vec{U} + v\vec{V}$ space in terms of $\vec{U}$ and $\vec{V}$ axes based on the following transfer function: $(y - L_m)\vec{Y} + nx\vec{X} = k\sinh(u\vec{U} + v\vec{V})$, where $L_m = L_c - m_s$, $n = \frac{m_s}{t_{ox2}\sinh|\cosh^{-1}(\frac{t_{ox2}+t_{si2}}{t_{ox2}})|}$, and $k = \frac{m_s}{\sinh|\cosh^{-1}(\frac{t_{ox2}+t_{si2}}{t_{ox2}})|}$. Based on the above formula, ABCD in the $x\vec{X} + y\vec{Y}$ coordinates is transformed into A'B'C'D' in the $u\vec{U} + v\vec{V}$ coordinates. As a result, the arc-shaped electric field contour in the oxide next to the right edge of the bottom gate in the $x\vec{X} + y\vec{Y}$ has become straight-line-shaped in the $u\vec{U} + v\vec{V}$ coordinates. Based on the transformation, the distance between the bottom gate electrode and the bottom thin-film/oxide interface t(y), which is a not a fixed value, has been transformed into $\frac{m\pi}{2}$, which is the distance between points A' and C' in the new coordinates under the condition $sinh(\frac{m\pi}{2}) = 1$. Therefore, a differential equation in terms of back surface potential Ψ_{b2} in the $u\vec{U} + v\vec{V}$ coordinates has been obtained. After solving it, the electrostatic potentials at bottom and top interfaces (Ψ_{b2}, Ψ_{s2}) are

$$\Psi_{b2}(y) = g_1\exp[\frac{\gamma}{k}(y - L_m)] + g_2\exp[-\frac{\gamma}{k}(y - L_m)] + \frac{B_1}{B_0}$$

$$\Psi_{s2}(y) = \frac{\sigma_2[\frac{2C_s}{C_{ox1}} + \frac{t_{si1}}{t(y)}]\Psi_{b2}(y) + [1 - \frac{t_{si1}}{t(y)}]V_g - [\frac{t_{si1}}{t(y)}]\Phi_{f2} +}{1 + \frac{2C_s}{C_{ox1}}}$$

where coefficients could be determined from boundary conditions. The threshold voltage is defined as the gate voltage when the sum of the electron densities at the locations with the minimum front and back surface potentials reaches the doping density of the thin-film:

$$N_A = n_i\exp(\frac{\Psi_{s(min)}}{V_T}) + n_i\exp(\frac{\Psi_{b(min)}}{V_T}).$$

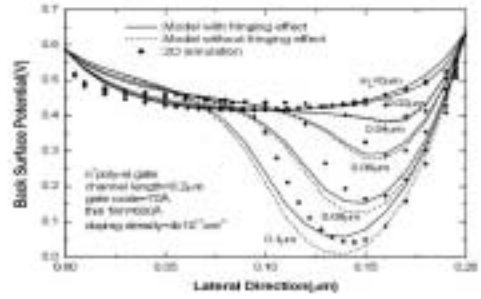
Using the above condition with another condition from the solution of the minimum front and back surface potentials:

$$V_{th} = \frac{[C_{ox1} + 2C_s]\Psi_{s(min)} - [C_{ox2} + 2C_s]\Psi_{b(min)} + C_{ox2}\Phi_{f2} -}{C_{ox1} - C_{ox2}} \quad (1)$$

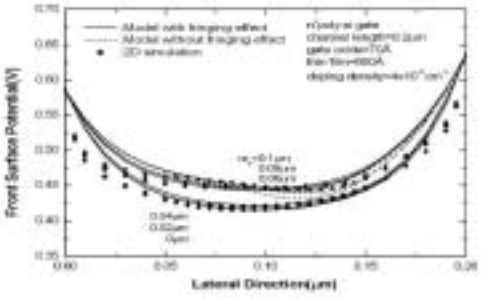
the threshold voltage of the DG SOI NMOS device with a gate misalignment has been obtained.

3. Model Verification

In order to assess the effectiveness of the analytical model for the gate misalignment effect of the DG SOI NMOS devices, the model results have been compared with the 2D simulation results. Fig. 3 shows (a) back and (b) front surface potential distributions of the DG SOI NMOS device with a channel length of 0.2μm, n^+ polysilicon top and bottom gates, a gate oxide of 70Å, a thin-film of 600Å doped with a p-type density of $4 \times 10^{17}cm^{-3}$, and various gate misalignments biased at $V_{GS} = V_{th}$ and $V_{DS} = 50mV$, based on the analytical model with and without considering fringing electric field effects, and 2D simulation results. As shown in the Fig. 3(a), when the gate misalignment increases, the back surface potential is lowered in the non-gate overlap region. Considering the fringing electric field effect due to gate misalignment, the dip in the back surface potential becomes smaller as compared to the case without considering it. In addition, when the gate misalignment becomes larger, the fringing electric field effect becomes more



(a)



(b)

Figure 3: (a) Back and (b) front surface potential distributions of the DG SOI NMOS device with a channel length of 0.2μm, n^+ polysilicon top and bottom gates, a gate oxide of 70Å, a thin-film of 600Å doped with a p-type density of $4 \times 10^{17}cm^{-3}$, and various gate misalignments biased at $V_{GS} = V_{th}$ and $V_{DS} = 50mV$, based on the analytical model with and without considering fringing electric field effects, and 2D simulation results.

important. As shown in Fig. 3(b), when the gate misalignment becomes larger, the fringing electric field effect on the front surface potential becomes more noticeable. In addition, a larger gate misalignment leads to a lower minimum front surface potential, which is also due to the fringing electric field effects. As shown in Figs.3(a)&(b), the analytical model considering the fringing electric field affect could predict front and back surface potential distributions consistently as verified by the 2D simulation results.

Fig. 4 shows the threshold voltage versus the gate misalignment of the DG SOI NMOS device with a channel length of 0.2μm, n^+ polysilicon top and bottom gates, a gate oxide of 70Å, and a thin-film of 500Å and 600Å doped with a p-type density of $4 \times 10^{17}cm^{-3}$, based on the analytical model with and without considering fringing electric field effects and 2D simulation results. As shown in the figure, for both cases with a thin-film of 500Å an 600Å, the

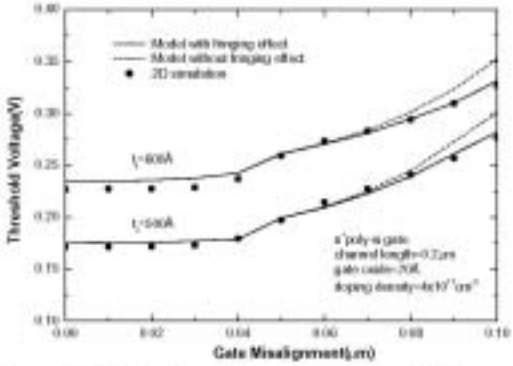


Figure 4: Threshold voltage versus gate misalignment of the DG SOI NMOS device with a channel length of 0.2μm, n^+ polysilicon top and bottom gates, a gate oxide of 70Å, and a thin-film of 500Å and 600Å doped with a p-type density of $4 \times 10^{17}cm^{-3}$, based on the analytical model with and without considering fringing electric field effects and 2D simulation results.

fringing electric field effect coming from gate misalignment is important in determining the threshold voltage. Without considering the fringing electric field effect, the threshold voltage is over-estimated, which is more noticeable when the gate misalignment becomes larger. At a gate misalignment of 0.1μm, the fringing electric field effect causes a reduction in threshold voltage about 0.022V (6%) for the thin-film of 600Å and 0.028V (7%) for 500Å. As shown the in the figure, as verified by the 2D simulation result, the analytical model considering the fringing electric field effect could provide an accurate prediction of the threshold voltage.

4. Discussion

Fig. 5 shows (a) minimum front and back surface potentials and (b) their locations versus gate misalignment of the DG SOI NMOS device with a channel length of 0.2μm, n^+ polysilicon top and bottom gates, a gate oxide of 70Å, and a thin-film of 600Å doped with a p-type density of $4 \times 10^{17}cm^{-3}$, biased at $V_{GS} = V_{th}$ and $V_{DS} = 50mV$. As shown in Fig. 5(a)&(b), when the gate misalignment is smaller than 0.03μm, the minimum front and back surface potentials are about equal, located in the gate overlap region. When the gate misalignment increases, the location with the minimum back surface potential moves toward the drain direction. At the gate misalignment of 0.04μm, it is located in the non-gate overlap region. A further increase in the gate misalignment leads to the situation that the location with the minimum back surface potential moves toward the source direction mildly. A similar situation

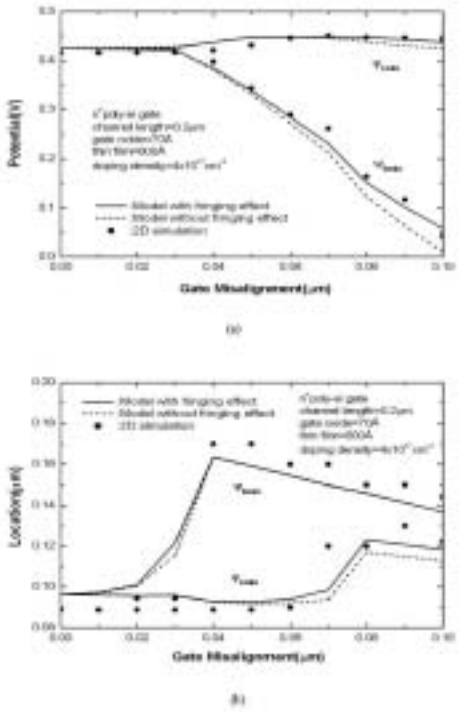


Figure 5: (a) Minimum front and back surface potentials and (b) their locations versus gate misalignment of the DG SOI NMOS device with a channel length of 0.2μm, n^+ polysilicon top and bottom gates, a gate oxide of 70Å, and a thin-film of 600Å doped with a p-type density of $4 \times 10^{17}\text{cm}^{-3}$, biased at $V_{GS} = V_{th}$ and $V_{DS} = 50\text{mV}$.

exists for the front surface potential but its transition point is located at the gate misalignment of 0.08μm. When the gate misalignment is greater than 0.08μm, the location with the minimum front surface potential moves to the non-gate overlap region. As shown in the figure, as verified by the 2D simulation results, the analytical model considering the fringing electric field effect predicts the behavior closely.

5. Conclusion

In this paper, an analysis of gate misalignment effect on the threshold voltage of DG FD SOI NMOS devices using a compact model considering fringing electric field effect has been described. Using the conformal mapping transformation approach, a closed-form compact model considering the fringing electric field effect above the non-gate overlap region has been derived to provide an accurate prediction of the threshold voltage behavior as verified by the 2D simulation results.

6. Acknowledgments

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